Yongtae Kim

List of Publications by Year in descending order

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32	396	1040056	996975
papers	citations	9	15
		h-index	g-index

32	32	32	361
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	An energy efficient approximate adder with carry skip for error resilient neuromorphic VLSI systems. , 2013, , .		76
2	A Reconfigurable Digital Neuromorphic Processor with Memristive Synaptic Crossbar for Cognitive Computing. ACM Journal on Emerging Technologies in Computing Systems, 2015, 11, 1-25.	2.3	54
3	A digital neuromorphic VLSI architecture with memristor crossbar synaptic array for machine learning. , 2012, , .		52
4	Energy Efficient Approximate Arithmetic for Error Resilient Neuromorphic Computing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2733-2737.	3.1	31
5	Design and Analysis of an Approximate Adder with Hybrid Error Reduction. Electronics (Switzerland), 2020, 9, 471.	3.1	29
6	A Novel Approximate Adder Design Using Error Reduced Carry Prediction and Constant Truncation. IEEE Access, 2021, 9, 119939-119953.	4.2	21
7	A 0.38 V near/subâ€•V T digitally controlled lowâ€dropout regulator with enhanced power supply noise rejection in 90 nm CMOS process. IET Circuits, Devices and Systems, 2013, 7, 31-41.	1.4	18
8	Recent Trend of Neuromorphic Computing Hardware: Intel's Neuromorphic System Perspective. , 2020, , .		15
9	An ultra-low voltage digitally controlled low-dropout regulator with digital background calibration. , 2012, , .		11
10	A Parallel Digital VLSI Architecture for Integrated Support Vector Machine Training and Classification. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1471-1484.	3.1	11
11	An Accuracy Enhanced Error Tolerant Adder with Carry Prediction for Approximate Computing. IEIE Transactions on Smart Processing and Computing, 2019, 8, 324-330.	0.4	10
12	Approximate adder design with simplified lower-part approximation. IEICE Electronics Express, 2020, 17, 20200218-20200218.	0.8	9
13	A Novel Approximate Adder with Enhanced Low-cost Carry Prediction for Error Tolerant Computing. IEIE Transactions on Smart Processing and Computing, 2019, 8, 506-510.	0.4	9
14	COREA: Delay- and Energy-Efficient Approximate Adder Using Effective Carry Speculation. Electronics (Switzerland), 2021, 10, 2234.	3.1	8
15	An Energy-Efficient Imprecise Adder with a Lower-part Constant Approximation. , 2020, , .		7
16	Bit-Shuffle Coding for Flicker Mitigation in Visible Light Communication. IEEE Access, 2019, 7, 150271-150279.	4.2	5
17	Approximate Digital Leaky Integrate-and-fire Neurons for Energy Efficient Spiking Neural Networks. IEIE Transactions on Smart Processing and Computing, 2020, 9, 252-259.	0.4	5
18	Training Spiking Neural Networks with an Adaptive Leaky Integrate-and-Fire Neuron. , 2020, , .		5

#	Article	IF	Citations
19	A 0.003-mm2, 0.35-V, 82-pJ/conversion ultra-low power CMOS all digital temperature sensor for on-die thermal management. Analog Integrated Circuits and Signal Processing, 2013, 75, 147-156.	1.4	3
20	A 9 Gb/s/ch Transceiver With Reference-Less Data-Embedded Pseudo-Differential Clock Signaling for Graphics Memory Interfaces. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1982-1986.	3.0	3
21	Resource-Optimized Design of Bit-Shuffle Block Coding for MIMO-VLC. IEEE Access, 2021, 9, 97675-97685.	4.2	3
22	Design of a Low-Cost Approximate Adder with a Zero Truncation. , 2020, , .		3
23	A low-power programmable DLL-based clock generator with wide-range anti-harmonic lock. , 2009, , .		2
24	Training and Inference using Approximate Floating-Point Arithmetic for Energy Efficient Spiking Neural Network Processors. , 2021, , .		2
25	Precision Exploration of Floating-Point Arithmetic for Spiking Neural Networks. , 2021, , .		2
26	Low-Power Cross-Layer Error Management Using MIMO-LDPC Iterative Decoding for Video Processing. IEEE Access, 2021, 9, 133062-133075.	4.2	1
27	DCPA: approximate adder design exploiting dual carry prediction. IEICE Electronics Express, 2021, 18, 20210431-20210431.	0.8	1
28	A New Approximate Adder with Duplicate-Constant Scheme for Energy Efficient Applications. , 2020, , .		0
29	A Novel ReRAM-Based Architecture of Field Sequential Color Driver for High-Resolution LCoS Displays. IEEE Access, 2020, 8, 223385-223395.	4.2	0
30	Design of an Accuracy Enhanced Imprecise Adder with Half Adder-based Approximation. , 2021, , .		0
31	Exploiting Data Compression for Adaptive Block Placement in Hybrid Caches. Electronics (Switzerland), 2022, 11, 240.	3.1	0
32	Design of a Light-Weight Key Scheduler for AES using LFSR for IoT Applications. , 2021, , .		0