Saibal Mukhopadhyay

List of Publications by Year
in descending order

144 papers	2,186 citations	279798 23 h-index	330143 37 g-index
144 all docs	144 docs citations	144 times ranked	1862 citing authors

#	Article	IF	Citations
1	Robust Processing-In-Memory With Multibit ReRAM Using Hessian-Driven Mixed-Precision Computation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1006-1019.	2.7	7
2	Task-Driven RGB-Lidar Fusion for Object Tracking in Resource-Efficient Autonomous System. IEEE Transactions on Intelligent Vehicles, 2022, 7, 102-112.	12.7	24
3	MONETA: A Processing-In-Memory-Based Hardware Platform for the Hybrid Convolutional Spiking Neural Network With Online Learning. Frontiers in Neuroscience, 2022, 16, 775457.	2.8	3
4	Unravelled multilevel transformation networks for predicting sparsely observed spatio-temporal dynamics. Philosophical Transactions Series A, Mathematical, Physical, and Engineering Sciences, 2022, 380, .	3.4	1
5	Securing IoT Devices Using Dynamic Power Management: Machine Learning Approach. IEEE Internet of Things Journal, 2021, 8, 16379-16394.	8.7	3
6	MAHASIM: Machine-Learning Hardware Acceleration Using a Software-Defined Intelligent Memory System. Journal of Signal Processing Systems, 2021, 93, 659-675.	2.1	1
7	Chiplet/Interposer Co-Design for Power Delivery Network Optimization in Heterogeneous 2.5-D ICs. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2021, 11, 2148-2157.	2.5	5
8	Reliable Edge Intelligence in Unreliable Environment. , 2021, , .		4
9	Anisotropic Scatterer Models for Representing RCS of Complex Objects. , 2021, , .		4
10	Adaptive Camera Platform Using Deep Learning-Based Early Warning of Task Failures. IEEE Sensors Journal, 2021, 21, 13794-13804.	4.7	2
11	Characterization of Drain Current Variations in FeFETs for PIM-based DNN Accelerators. , 2021, , .		6
12	Neural Identification for Control. IEEE Robotics and Automation Letters, 2021, 6, 4648-4655.	5.1	3
13	Impact of HKMG and FDSOI FeFET drain current variation in processing-in-memory architectures. Journal of Materials Research, 2021, 36, 4379-4393.	2.6	0
14	SPEED: Spiking Neural Network With Event-Driven Unsupervised Learning and Near-Real-Time Inference for Event-Based Vision. IEEE Sensors Journal, 2021, 21, 20578-20588.	4.7	3
15	ScieNet: Deep learning with spike-assisted contextual information extraction. Pattern Recognition, 2021, 118, 108002.	8.1	5
16	Physics-incorporated convolutional recurrent neural networks for source identification and forecasting of dynamical systems. Neural Networks, 2021, 144, 359-371.	5.9	13
17	Machine Learning in Wavelet Domain for Electromagnetic Emission Based Malware Analysis. IEEE Transactions on Information Forensics and Security, 2021, 16, 3426-3441.	6.9	12
18	A Deep Learning Approach for Predicting Spatiotemporal Dynamics From Sparsely Observed Data. IEEE Access, 2021, 9, 64200-64210.	4.2	3

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19	Characterization of Generalizability of Spike Timing Dependent Plasticity Trained Spiking Neural Networks. Frontiers in Neuroscience, 2021, 15, 695357.	2.8	6
20	A quantum Hopfield associative memory implemented on an actual quantum processor. Scientific Reports, 2021, 11, 23391.	3.3	7
21	A Digital Low-Dropout Regulator With Autotuned PID Compensator and Dynamic Gain Control for Improved Transient Performance Under Process Variations and Aging. IEEE Transactions on Power Electronics, 2020, 35, 3242-3253.	7.9	16
22	SAFE-DNN: A Deep Neural Network With Spike Assisted Feature Extraction For Noise Robust Inference. , 2020, , .		3
23	Processing-In-Memory-Based On-Chip Learning With Spike-Time-Dependent Plasticity in 65-nm CMOS. IEEE Solid-State Circuits Letters, 2020, 3, 278-281.	2.0	9
24	Flex-PIM: A Ferroelectric FET based Vector Matrix Multiplication Engine with Dynamical Bitwidth and Floating Point Precision. , 2020, , .		4
25	WarningNet: A Deep Learning Platform for Early Warning of Task Failures under Input Perturbation for Reliable Autonomous Platforms. , 2020, , .		2
26	A Flexible Precision Multi-Format In-Memory Vector Matrix Multiplication Engine in 65 nm CMOS With RF Machine Learning Support. IEEE Solid-State Circuits Letters, 2020, 3, 450-453.	2.0	2
27	Attention-Based Activation Pruning to Reduce Data Movement in Real-Time AI: A Case-Study on Local Motion Planning in Autonomous Vehicles. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2020, 10, 306-319.	3.6	11
28	Architecture, Chip, and Package Codesign Flow for Interposer-Based 2.5-D Chiplet Integration Enabling Heterogeneous IP Reuse. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2424-2437.	3.1	32
29	Design Flow for Active Interposer-Based 2.5-D ICs and Study of RISC-V Architecture With Secure NoC. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2020, 10, 2047-2060.	2.5	7
30	Uncertainty Characterization in Active Sensor Systems with DNN-based Feedback Control. , 2020, , .		3
31	Effect of Process Variations in Digital Pixel Circuits on the Accuracy of DNN based Smart Sensor. , 2020, , .		3
32	An Inductive Voltage Regulator With Overdrive Tracking Across Input Voltage in Cascoded Power Stage. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3083-3087.	3.0	0
33	Aging Challenges in On-chip Voltage Regulator Design. , 2020, , .		0
34	Multispectral Information Fusion With Reinforcement Learning for Object Tracking in IoT Edge Devices. IEEE Sensors Journal, 2020, 20, 4333-4344.	4.7	13
35	A Configurable Dual-Mode PRINCE Cipher with Security Aware Pipelining in 65nm for High Throughput Applications. , 2020, , .		1
36	A Fully Synthesized Integrated Buck Regulator with Auto-generated GDS-II in 65nm CMOS Process. , 2020, , .		2

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37	An Authentication IC with Visible Light Based Interrogation in 65nm CMOS. , 2020, , .		1
38	A Heterogeneous Spiking Neural Network for Unsupervised Learning of Spatiotemporal Patterns. Frontiers in Neuroscience, 2020, 14, 615756.	2.8	13
39	Algorithm-Circuit Cross-layer Control for Digital Pixel Image Sensors. , 2020, , .		3
40	Multigated Carbon Nanotube Field Effect Transistors-Based Physically Unclonable Functions As Security Keys. IEEE Internet of Things Journal, 2019, 6, 325-334.	8.7	14
41	Energy Efficient and Side-Channel Secure Cryptographic Hardware for IoT-Edge Nodes. IEEE Internet of Things Journal, 2019, 6, 421-434.	8.7	38
42	CAMEL: An Adaptive Camera With Embedded Machine Learning-Based Sensor Parameter Control. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 498-508.	3.6	13
43	On the Effect of NBTI Induced Aging of Power Stage on the Transient Performance of On-Chip Voltage Regulators. , 2019, , .		1
44	A Ferroelectric FET-Based Processing-in-Memory Architecture for DNN Acceleration. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2019, 5, 113-122.	1.5	40
45	Application Inference using Machine Learning based Side Channel Analysis. , 2019, , .		14
46	Mixture of Pre-processing Experts Model for Noise Robust Deep Learning on Resource Constrained Platforms. , 2019, , .		9
47	Design of Reliable DNN Accelerator with Un-reliable ReRAM. , 2019, , .		88
48	Automatic GDSII Generator for On-Chip Voltage Regulator for Easy Integration in Digital SoCs. , 2019, , .		1
49	RTL-to-GDS Tool Flow and Design-for-Test Solutions for Monolithic 3D ICs. , 2019, , .		8
50	Fast and Low-Precision Learning in GPU-Accelerated Spiking Neural Network. , 2019, , .		14
51	Autotuning of Integrated Inductive Voltage Regulator Using On-Chip Delay Sensor to Tolerate Process and Passive Variations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1768-1778.	3.1	3
52	Improving Robustness of ReRAM-based Spiking Neural Network Accelerator with Stochastic Spike-timing-dependent-plasticity. , 2019, , .		11
53	Improved Power/EM Side-Channel Attack Resistance of 128-Bit AES Engines With Random Fast Voltage Dithering. IEEE Journal of Solid-State Circuits, 2019, 54, 569-583.	5.4	47
54	Design and Analysis of a Neural Network Inference Engine Based on Adaptive Weight Compression. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 109-121.	2.7	12

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55	Exploiting on-chip power management for side-channel security. , 2018, , .		4
56	3-D Stacked Image Sensor With Deep Neural Network Computation. IEEE Sensors Journal, 2018, 18, 4187-4199.	4.7	30
57	3D Stacked High Throughput Pixel Parallel Image Sensor with Integrated ReRAM Based Neural Accelerator. , 2018, , .		8
58	An Image Sensor SOC with Energy Harvesting Mixed-Vth Pixel Generating 5.8Î¼W/mm2 Power Density and 0.77 Frames/second Self-Powered Frame Rate. , 2018, , .		0
59	A ferroelectric FET based power-efficient architecture for data-intensive computing. , 2018, , .		18
60	An Unsupervised Anomalous Event Detection Framework with Class Aware Source Separation. , 2018, , .		6
61	An Energy-Quality Scalable Wireless Image Sensor Node for Object-Based Video Surveillance. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 591-602.	3.6	7
62	Reducing Power Side-Channel Information Leakage of AES Engines Using Fully Integrated Inductive Voltage Regulator. IEEE Journal of Solid-State Circuits, 2018, 53, 2399-2414.	5.4	45
63	Accelerating biophysical neural network simulation with region of interest based approximation. , 2018, , .		2
64	Performance based tuning of an inductive integrated voltage regulator driving a digital core against process and passive variations. , 2018, , .		3
65	ReRAM-Based Processing-in-Memory Architecture for Recurrent Neural Network Acceleration. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2781-2794.	3.1	81
66	DeepTrain: A Programmable Embedded Platform for Training Deep Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2360-2370.	2.7	21
67	Reverse Power Delivery Network for Wireless Power Transfer. IEEE Microwave and Wireless Components Letters, 2018, 28, 624-626.	3.2	4
68	A Power-Aware Digital Multilayer Perceptron Accelerator with On-Chip Training Based on Approximate Computing. IEEE Transactions on Emerging Topics in Computing, 2017, 5, 164-178.	4.6	33
69	Adaptive weight compression for memory-efficient neural networks. , 2017, , .		23
70	An All-Digital Fully Integrated Inductive Buck Regulator With A 250-MHz Multi-Sampled Compensator and a Lightweight Auto-Tuner in 130-nm CMOS. IEEE Journal of Solid-State Circuits, 2017, 52, 1825-1835.	5.4	36
71	Active Fluidic Cooling on Energy Constrained System-on-Chip Systems. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2017, 7, 1813-1822.	2.5	8
72	Clock Data Compensation Aware Digital Circuits Design for Voltage Margin Reduction. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2401-2413.	5.4	1

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73	A Single-Chip Image Sensor Node With Energy Harvesting From a CMOS Pixel Array. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2295-2307.	5.4	11
74	Reliability-performance tradeoffs between 2.5D and 3D-stacked DRAM processors. , 2016, , .		2
75	Neurocube: A Programmable Digital Neuromorphic Architecture with High-Density 3D Memory. , 2016, , .		97
76	ReRAM Crossbar based Recurrent Neural Network for human activity detection. , 2016, , .		19
77	Reconfigurable 96Ã—128 active pixel sensor with 2.1ÂµW/mm² power generation and regulated multi-domain power delivery for self-powered imaging. , 2016, , .		1
78	Design, Characterization, and Application of a Field-Programmable Thermal Emulation Platform. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2016, 6, 1330-1339.	2.5	1
79	Amdahl's law for lifetime reliability scaling in heterogeneous multicore processors. , 2016, , .		6
80	Impact of Heterogeneous Technology Integration on the Power, Performance, and Quality of a 3D Image Sensor. IEEE Transactions on Multi-Scale Computing Systems, 2016, 2, 61-67.	2.4	6
81	(Invited paper) energy delivery for self-powered IoT devices. , 2016, , .		2
82	Thermally Adaptive Cache Access Mechanisms for 3D Many-Core Architectures. IEEE Computer Architecture Letters, 2016, 15, 129-132.	1.5	3
83	Partitioning Methods for Interface Circuit of Heterogeneous 3-D-ICs Under Process Variation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1626-1635.	3.1	2
84	A 190 nA Bias Current 10 mV Input Multistage Boost Regulator With Intermediate-Node Control to Supply RF Blocks in Self-Powered Wireless Sensors. IEEE Transactions on Power Electronics, 2016, 31, 1322-1333.	7.9	10
85	Neurocube. Computer Architecture News, 2016, 44, 380-392.	2.5	207
86	Near Data Processing. , 2015, , .		16
87	Optimization of FinFET-based circuits using a dual gate pitch technique. , 2015, , .		7
88	Experimental characterization of in-package microfluidic cooling on a System-on-Chip. , 2015, , .		3
89	A power-aware digital feedforward neural network platform with backpropagation driven approximate synapses. , 2015, , .		29
90	KitFox: Multiphysics Libraries for Integrated Power, Thermal, and Reliability Simulations of Multicore Microarchitecture. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2015, 5, 1590-1601.	2.5	7

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91	Negative Gate Transconductance in Gate/Source Overlapped Heterojunction Tunnel FET and Application to Single Transistor Phase Encoder. IEEE Electron Device Letters, 2015, 36, 201-203.	3.9	13
92	A Memory-Based Logic Block With Optimized-for-Read SRAM for Energy-Efficient Reconfigurable Computing Fabric. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 593-597.	3.0	8
93	Post-Silicon Estimation of Spatiotemporal Temperature Variations Using MIMO Thermal Filters. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2015, 5, 650-660.	2.5	3
94	On the Impact of Energy-Accuracy Tradeoff in a Digital Cellular Neural Network for Image Processing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1070-1081.	2.7	22
95	On-Chip Power Generation Using Ultrathin Thermoelectric Generators. Journal of Electronic Packaging, Transactions of the ASME, 2015, 137, .	1.8	8
96	Ultra-low power electronics with Si/Ge tunnel FET. , 2014, , .		16
97	A tunnel-FET SRAM array for energy-efficient embedded memory blocks in reconfigurable computing platforms. , 2014, , .		0
98	System-level chip/package co-design for multi-core processors implemented with power-gating technique. , 2014, , .		0
99	TSV-Aware Interconnect Distribution Models for Prediction of Delay and Power Consumption of 3-D Stacked ICs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1384-1395.	2.7	28
100	Energy Introspector: A parallel, composable framework for integrated power-reliability-thermal modeling for multicore architectures. , 2014, , .		8
101	Application of Silicon-Germanium Source Tunnel-FET to Enable Ultralow Power Cellular Neural Network-Based Associative Memory. IEEE Transactions on Electron Devices, 2014, 61, 3707-3715.	3.0	34
102	A Simulation Study of Oxygen Vacancy-Induced Variability in ${m HfO}_{2}$ /Metal Gated SOI FinFET. IEEE Transactions on Electron Devices, 2014, 61, 1262-1269.	3.0	17
103	Resilient Pipeline Under Supply Noise With Programmable Time Borrowing and Delayed Clock Gating. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 173-177.	3.0	8
104	Control Principles and On-Chip Circuits for Active Cooling Using Integrated Superlattice-Based Thin-Film Thermoelectric Devices. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1909-1919.	3.1	8
105	Post-Silicon Characterization and On-Line Prediction of Transient Thermal Field in Integrated Circuits Using Thermal System Identification. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2014, 4, 37-45.	2.5	3
106	A Wide Conversion Ratio, Extended Input 3.5-Î¼A Boost Regulator With 82% Efficiency for Low-Voltage Energy Harvesting. IEEE Transactions on Power Electronics, 2014, 29, 4776-4786.	7.9	25
107	A Variation-Aware Preferential Design Approach for Memory-Based Reconfigurable Computing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 2449-2461.	3.1	1
108	Analysis of the Performance, Power, and Noise Characteristics of a CMOS Image Sensor With 3-D Integrated Image Compression Unit. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2014, 4, 198-208.	2.5	8

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109	Ultra-low power electronics with Si/Ge tunnel FET. , 2014, , .		1
110	Guest Editorial Computing in Emerging Technologies (First Issue). IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2014, 4, 377-379.	3.6	0
111	Performance and Robustness of 3-D Integrated SRAM Considering Tier-to-Tier Thermal and Supply Crosstalk. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2013, 3, 943-953.	2.5	4
112	A 110nA synchronous boost regulator with autonomous bias gating for energy harvesting. , 2013, , .		3
113	Hotspot Cooling in Stacked Chips Using Thermoelectric Coolers. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2013, 3, 759-767.	2.5	35
114	Power Multiplexing for Thermal Field Management in Many-Core Processors. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2013, 3, 94-104.	2.5	4
115	Simulation of the TSV-to-device coupling in 3D ICs for short-channel strained silicon transistors. , 2013, , .		0
116	On the impact of 3D integration on high-throughput sensor information processing: A case study with image sensing. , 2013, , .		2
117	Thermal Investigation Into Power Multiplexing for Homogeneous Many-Core Processors. Journal of Heat Transfer, 2012, 134, .	2.1	10
118	Variation-Aware Clock Network Design Methodology for Ultralow Voltage (ULV) Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1222-1234.	2.7	8
119	Low-power design under variation using error prevention and error tolerance (invited paper). , 2012, , .		0
120	Through-Oxide-Via-Induced Back-Gate Effect in 3-D Integrated FDSOI Devices. IEEE Electron Device Letters, 2011, 32, 1020-1022.	3.9	8
121	Fast and Accurate Analytical Modeling of Through-Silicon-Via Capacitive Coupling. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2011, 1, 168-180.	2.5	71
122	Ultrathin Thermoelectric Devices for On-Chip Peltier Cooling. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2011, 1, 1395-1405.	2.5	66
123	Pre-Bond and Post-Bond Test and Signal Recovery Structure to Characterize and Repair TSV Defect Induced Signal Degradation in 3-D System. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2011, 1, 1718-1727.	2.5	50
124	Low energy process variation tolerant digital image processing system design based on accuracy-energy tradeoffs. , 2011, , .		0
125	A Scalable Design Methodology for Energy Minimization of STTRAM: A Circuit and Architecture Perspective. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 809-817.	3.1	30
126	Energy-Efficient Reconfigurable Computing Using a Circuit-Architecture-Software Co-Design Approach. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2011, 1, 369-380.	3.6	22

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127	Modeling and Analysis of Image Dependence and Its Implications for Energy Savings in Error Tolerant Image Processing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 1163-1172.	2.7	11
128	Analysis and Design of Energy and Slew Aware Subthreshold Clock Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 1349-1358.	2.7	11
129	Design method and test structure to characterize and repair TSV defect induced signal degradation in 3D system. , 2010, , .		55
130	Postsilicon Adaptation for Low-Power SRAM under Process Variation. IEEE Design and Test of Computers, 2010, 27, 26-35.	1.0	3
131	Dual-Source-Line-Bias Scheme to Improve the Read Margin and Sensing Accuracy of STTRAM in Sub-90-nm Nodes. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 208-212.	3.0	3
132	Thermal mangament of multicore processors using power multiplexing. , 2010, , .		3
133	On-chip Peltier cooling using current pulse. , 2010, , .		11
134	Accuracy-aware SRAM: A reconfigurable low power SRAM architecture for mobile multimedia applications. , 2009, , .		21
135	A Generic Data-Driven Nonparametric Framework for Variability Analysis of Integrated Circuits in Nanometer Technologies. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 1038-1046.	2.7	6
136	Design of Sub-90 nm Low-Power and Variation Tolerant PD/SOI SRAM Cell Based on Dynamic Stability Metrics. IEEE Journal of Solid-State Circuits, 2009, 44, 965-976.	5.4	27
137	Device Design and Optimization Methodology for Leakage and Variability Reduction in Sub-45-nm FD/SOI SRAM. IEEE Transactions on Electron Devices, 2008, 55, 152-162.	3.0	11
138	Optimal Dual-V_{T} Design in Sub-100-nm PD/SOI and Double-Gate Technologies. IEEE Transactions on Electron Devices, 2008, 55, 1161-1169.	3.0	1
139	Reduction of Parametric Failures in Sub-100-nm SRAM Array Using Body Bias. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 174-183.	2.7	27
140	A generic method for variability analysis of nanoscale circuits. , 2008, , .		3
141	Profit Aware Circuit Design Under Process Variations Considering Speed Binning. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 806-815.	3.1	20
142	Design and Analysis of a Self-Repairing SRAM with On-Chip Monitor and Compensation Circuitry. VLSI Test Symposium (VTS), Proceedings, IEEE, 2008, , .	1.0	5
143	Design of a Process Variation Tolerant Self-Repairing SRAM for Yield Enhancement in Nanoscaled CMOS. IEEE Journal of Solid-State Circuits, 2007, 42, 1370-1382.	5.4	50
144	Device-Optimization Technique for Robust and Low-Power FinFET SRAM Design in NanoScale Era. IEEE Transactions on Electron Devices, 2007, 54, 1409-1419.	3.0	85