Jun-Young Park

List of Publications by Year
in descending order

42	589	623734	642732
papers	citations	14 h-index	23 g-index

43	43	43	720
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Power Reduction in Punch-Through Current-Based Electro-Thermal Annealing in Gate-All-Around FETs. Micromachines, 2022, 13, 124.	2.9	3
2	Impact of Iterative Deuterium Annealing in Long-Channel MOSFET Performance. Materials, 2022, 15, 1960.	2.9	9
3	N-Type Nanosheet FETs without Ground Plane Region for Process Simplification. Micromachines, 2022, 13, 432.	2.9	9
4	Vacuum Inner Spacer to Improve Annealing Effect during Electro-Thermal Annealing of Nanosheet FETs. Micromachines, 2022, 13, 987.	2.9	0
5	Impact of Post-Metal Annealing With Deuterium or Nitrogen for Curing a Gate Dielectric Using Joule Heat Driven by Punch-Through Current. IEEE Electron Device Letters, 2021, 42, 276-279.	3.9	5
6	Inner Spacer Engineering to Improve Mechanical Stability in Channel-Release Process of Nanosheet FETs. Electronics (Switzerland), 2021, 10, 1395.	3.1	9
7	Gateless and Capacitorless Germanium Biristor with a Vertical Pillar Structure. Micromachines, 2021, 12, 899.	2.9	2
8	Dielectric Engineering to Suppress Cell-to-Cell Programming Voltage Interference in 3D NAND Flash Memory. Micromachines, 2021, 12, 1297.	2.9	2
9	A Study of High-Temperature Effects on an Asymmetrically Doped Vertical Pillar-Type Field-Effect Transistor. IEEE Nanotechnology Magazine, 2020, 19, 52-55.	2.0	7
10	Quantitative Analysis of High-Pressure Deuterium Annealing Effects on Vertically Stacked Gate-All-Around SONOS Memory. IEEE Transactions on Electron Devices, 2020, 67, 3903-3907.	3.0	15
11	Curing of Aged Gate Dielectric by the Self-Heating Effect in MOSFETs. IEEE Transactions on Electron Devices, 2020, 67, 777-788.	3.0	21
12	Self-Heating Effects in 3-D Vertical-NAND (V-NAND) Flash Memory. IEEE Transactions on Electron Devices, 2020, 67, 5505-5510.	3.0	0
13	A Comparative Study of the Curing Effects of Local and Global Thermal Annealing on a FinFET. IEEE Journal of the Electron Devices Society, 2019, 7, 954-958.	2.1	4
14	Curing of Hot-Carrier Induced Damage by Gate-Induced Drain Leakage Current in Gate-All-Around FETs. IEEE Electron Device Letters, 2019, 40, 1909-1912.	3.9	14
15	Nanoscale FET-Based Transduction toward Sensitive Extended-Gate Biosensors. ACS Sensors, 2019, 4, 1724-1729.	7.8	28
16	Suppression of Self-Heating Effects in 3-D V-NAND Flash Memory Using a Plugged Pillar-Shaped Heat Sink. IEEE Electron Device Letters, 2019, 40, 212-215.	3.9	12
17	Demonstration of Thermally-Assisted Programming With High Speed and Improved Reliability for Junctionless Nanowire NOR Flash Memory. IEEE Nanotechnology Magazine, 2019, 18, 1110-1113.	2.0	2
18	Electro-Thermal Erasing at 10⁴-Fold Faster Speeds in Charge-Trap Flash Memory. IEEE Electron Device Letters, 2019, 40, 196-199.	3.9	6

#	Article	IF	Citations
19	Demonstration of a Curable Nanowire FinFET Using Punchthrough Current to Repair Hot-Carrier Damage. IEEE Electron Device Letters, 2018, 39, 180-183.	3.9	20
20	A Comparative Study on Hot-Carrier Injection in 5-Story Vertically Integrated Inversion-Mode and Junctionless-Mode Gate-All-Around MOSFETs. IEEE Electron Device Letters, 2018, 39, 4-7.	3.9	26
21	Localized Electrothermal Annealing with Nanowatt Power for a Silicon Nanowire Field-Effect Transistor. ACS Applied Materials & Interfaces, 2018, 10, 4838-4843.	8.0	7
22	A Recoverable Synapse Device Using a Threeâ€Dimensional Silicon Transistor. Advanced Functional Materials, 2018, 28, 1804844.	14.9	34
23	On-Chip Curing by Microwave for Long Term Usage of Electronic Devices in Harsh Environments. Scientific Reports, 2018, 8, 14953.	3.3	4
24	Electrothermal Annealing to Enhance the Electrical Performance of an Exfoliated MoS2 Field-Effect Transistor. IEEE Electron Device Letters, 2018, , 1-1.	3.9	7
25	Sanitization of Data in Nanoscale Flash Memory by Thermal Erasing and Reuse of Storage. Physica Status Solidi (A) Applications and Materials Science, 2018, 215, 1800194.	1.8	2
26	Investigation of Self-Heating Effects in Gate-All-Around MOSFETs With Vertically Stacked Multiple Silicon Nanowire Channels. IEEE Transactions on Electron Devices, 2017, 64, 4393-4399.	3.0	31
27	A Novel Technique for Curing Hot-Carrier-Induced Damage by Utilizing the Forward Current of the PN-Junction in a MOSFET. IEEE Electron Device Letters, 2017, 38, 1012-1014.	3.9	21
28	Nano-electromechanical Switch Based on a Physical Unclonable Function for Highly Robust and Stable Performance in Harsh Environments. ACS Nano, 2017, 11, 12547-12552.	14.6	34
29	Electro-Thermal Annealing Method for Recovery of Cyclic Bending Stress in Flexible a-IGZO TFTs. IEEE Transactions on Electron Devices, 2017, 64, 3189-3192.	3.0	22
30	LF Noise Analysis for Trap Recovery in Gate Oxides Using Built-In Joule Heater. IEEE Transactions on Electron Devices, 2017, 64, 5081-5086.	3.0	6
31	Improved Technique for Extraction of Effective Mobility by Considering Gate Bias-Dependent Inversion Charges in a Floating-Body Si/SiGe pMOSFET. Journal of Nanoscience and Nanotechnology, 2017, 17, 3247-3250.	0.9	1
32	Controllable electrical and physical breakdown of poly-crystalline silicon nanowires by thermally assisted electromigration. Scientific Reports, 2016, 6, 19314.	3.3	12
33	Physically Transient Memory on a Rapidly Dissoluble Paper for Security Application. Scientific Reports, 2016, 6, 38324.	3.3	36
34	First demonstration of a wrap-gated CNT-FET with vertically-suspended channels. , 2016, , .		1
35	Sustainable electronics for nano-spacecraft in deep space missions. , 2016, , .		19
36	Joule Heating to Enhance the Performance of a Gate-All-Around Silicon Nanowire Transistor. IEEE Transactions on Electron Devices, 2016, 63, 2288-2292.	3.0	8

#	Article	IF	Citations
37	Threshold Voltage Tuning Technique in Gate-All-Around MOSFETs by Utilizing Gate Electrode With Potential Distribution. IEEE Electron Device Letters, 2016, 37, 1391-1394.	3.9	5
38	Electrothermal Annealing (ETA) Method to Enhance the Electrical Performance of Amorphous-Oxide-Semiconductor (AOS) Thin-Film Transistors (TFTs). ACS Applied Materials & Interfaces, 2016, 8, 23820-23826.	8.0	14
39	Three-Dimensional Fin-Structured Semiconducting Carbon Nanotube Network Transistor. ACS Nano, 2016, 10, 10894-10900.	14.6	16
40	Local Electro-Thermal Annealing for Repair of Total Ionizing Dose-Induced Damage in Gate-All-Around MOSFETs. IEEE Electron Device Letters, 2016, 37, 843-846.	3.9	22
41	Self-Curable Gate-All-Around MOSFETs Using Electrical Annealing to Repair Degradation Induced From Hot-Carrier Injection. IEEE Transactions on Electron Devices, 2016, 63, 910-915.	3.0	33
42	Vertically Integrated Multiple Nanowire Field Effect Transistor. Nano Letters, 2015, 15, 8056-8061.	9.1	60