Azad R Naeemi

List of Publications by Year
in descending order

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183	4,157	218381	138251
papers	citations	26 h-index	58 g-index

183	183	183	2567
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Bipolar Electric-Field Switching of Perpendicular Magnetic Tunnel Junctions through Voltage-Controlled Exchange Coupling. Nano Letters, 2022, 22, 622-629.	4.5	15
2	Physics-Based Models for Magneto-Electric Spin-Orbit Logic Circuits. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2022, 8, 10-18.	1.1	4
3	Evaluating the Performances of the Ultralow Power Magnetoelectric Random Access Memory With a Physics-Based Compact Model of the Antiferromagnet/Ferromagnet Bilayer. IEEE Transactions on Electron Devices, 2022, 69, 2331-2337.	1.6	7
4	Performance Benchmarking of Spin-Orbit Torque Magnetic RAM (SOT-MRAM) for Deep Neural Network (DNN) Accelerators. , 2022, , .		1
5	Modeling and Design for Magnetoelectric Ternary Content Addressable Memory (TCAM). IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2022, 8, 44-52.	1.1	4
6	Plasmonic MIM and MSM Waveguide Couplers for Plasmonic Integrated Computing System. IEEE Photonics Journal, 2022, 14, 1-10.	1.0	3
7	Improving SRAM Performance With Different Interconnect Options at the 7 nm Process Node. , 2022, , .		1
8	Quantum games and interactive tools for quantum technologies outreach and education. Optical Engineering, 2022, 61, .	0.5	29
9	Hysteresis-Free Negative Capacitance Effect in Metal-Ferroelectric-Insulator-Metal Capacitors with Dielectric Leakage and Interfacial Trapped Charges. Physical Review Applied, 2021, 15, .	1.5	6
10	Nonvolatile Voltage Controlled Molecular Spin-State Switching for Memory Applications. Magnetochemistry, 2021, 7, 37.	1.0	29
11	The 2021 Magnonics Roadmap. Journal of Physics Condensed Matter, 2021, 33, 413001.	0.7	287
12	IEEE Journal on Exploratory Solid-State Computational Devices and Circuitsâ€”Volume 7, No. 1. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2021, 7, ii-iii.	1.1	0
13	Impact of carrier mobility and lifetime on the potential performance of a plasmonic detector. , 2021, , .		0
14	IEEE Journal on Exploratory Solid-State Computational Devices and Circuitsâ€”Volume 7, No. 2. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2021, 7, ii-iii.	1.1	0
15	Understanding the Switching Mechanisms of the Antiferromagnet/Ferromagnet Heterojunction. Nano Letters, 2020, 20, 7919-7926.	4.5	11
16	IEEE Journal on Exploratory Solid-State Computational Devices and Circuitsâ€”Volume 6, No. 1. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2020, 6, ii-iii.	1.1	0
17	Valley-Spin Logic Gates. Physical Review Applied, 2020, 13, .	1.5	27
18	Modeling and Optimization of Plasmonic Detectors for Beyond-CMOS Plasmonic Majority Logic Gates. Journal of Lightwave Technology, 2020, 38, 5092-5099.	2.7	4

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19	Multiplier Architectures: Challenges and Opportunities with Plasmonic-based Logic : (Special Session) Tj ETQq1 1 0.784314 rgBT /Ove		2
20	Benchmarking and Optimization of Spintronic Memory Arrays. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2020, 6, 9-17.	1.1	15
21	Accurate Determination of Interlayer Resistivity of 2-D Layered Systems: Graphene Case Study. IEEE Transactions on Electron Devices, 2020, 67, 627-632.	1.6	2
22	Materials Requirements of High-Speed and Low-Power Spin-Orbit-Torque Magnetic Random-Access Memory. IEEE Journal of the Electron Devices Society, 2020, 8, 674-680.	1.2	18
23	A Theoretical Study of Multidomain Ferroelectric Switching Dynamics With a Physics-Based SPICE Circuit Model for Phase-Field Simulations. IEEE Transactions on Electron Devices, 2020, 67, 2952-2959.	1.6	10
24	Simulation of the Magnetization Dynamics of a Single-Domain BiFeOâ‚ƒ Nanoisland. IEEE Transactions on Magnetics, 2020, 56, 1-9.	1.2	7
25	IEEE Journal on Exploratory Solid-State Computational Devices and Circuitsâ€”Volume 6, No. 2. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2020, 6, ii-iii.	1.1	0
26	Modeling and Benchmarking Back End Of The Line Technologies on Circuit Designs at Advanced Nodes. , 2020, , .		4
27	IEEE Journal on Exploratory Solid-State Computational Devices and Circuitsâ€”Volume 5, No. 1. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2019, 5, ii-iii.	1.1	0
28	A Mixed Signal Architecture for Convolutional Neural Networks. ACM Journal on Emerging Technologies in Computing Systems, 2019, 15, 1-26.	1.8	16
29	Special Topic on Ferroelectric Transistors for Advanced Logic, Analog, and Memory Applications. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2019, 5, ii-iii.	1.1	0
30	Energy-Efficient Convolutional Neural Network Based on Cellular Neural Network Using Beyond-CMOS Technologies. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2019, 5, 85-93.	1.1	5
31	Materials Requirements of High-Speed and Low-Power Spin-Orbit-Torque Magnetic Random-Access Memory. , 2019, , .		2
32	Beyond Motivation and Memorization. , 2019, , .		2
33	Clocked Magnetostriction-Assisted Spintronic Device Design and Simulation. IEEE Transactions on Electron Devices, 2018, 65, 2040-2046.	1.6	7
34	Performance Analysis and Enhancement of Negative Capacitance Logic Devices Based on Internally Resistive Ferroelectrics. IEEE Electron Device Letters, 2018, 39, 765-768.	2.2	11
35	Hybrid piezoelectric-magnetic neurons. , 2018, , .		2
36	Particle in a Box: An Experiential Environment for Learning Introductory Quantum Mechanics. IEEE Transactions on Education, 2018, 61, 29-37.	2.0	21

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37	Accurate processor-level wirelength distribution model for technology pathfinding using a modernized interpretation of rent's rule. , 2018, , .		0
38	Correction to â€œA Nonvolatile Fast-Read Two-Transistor SRAM Based on Spintronic Devicesâ€•[Dec 17 93-100]. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2018, 4, 50-50.	1.1	0
39	Complementary Logic Implementation for Antiferromagnet Field-Effect Transistors. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2018, 4, 69-75.	1.1	9
40	Generic system-level modeling and optimization for beyond CMOS device applications. , 2018, , .		0
41	Transient Performance Analysis and Optimization of Crossbar Memory Arrays Using NbO2-Based Threshold Switching Selectors. IEEE Transactions on Electron Devices, 2018, 65, 3214-3220.	1.6	2
42	Analytic modeling of dipolar field requirements for robust coupling in a non-identical biaxial two-magnet system. Journal of Applied Physics, 2018, 124, 023901.	1.1	1
43	Modeling Interconnect Variability at Advanced Technology Nodes and Potential Solutions. IEEE Transactions on Electron Devices, 2017, 64, 1246-1253.	1.6	9
44	Nonvolatile Spintronic Memory Array Performance Benchmarking Based on Three-Terminal Memory Cell. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2017, 3, 10-17.	1.1	16
45	Theoretical Approach to Electroresistance in Ferroelectric Tunnel Junctions. Physical Review Applied, 2017, 7, .	1.5	26
46	Corrections to â€œInterconnect Design and Benchmarking for Charge-Based Beyond-CMOS Device Proposalsâ€•[Apr 16 508-511]. IEEE Electron Device Letters, 2017, 38, 690-690.	2.2	0
47	Beyond-CMOS non-Boolean logic benchmarking: Insights and future directions. , 2017, , .		8
48	A Pathway to Enable Exponential Scaling for the Beyond-CMOS Era. , 2017, , .		19
49	Overcoming thermal noise in non-volatile spin wave logic. Scientific Reports, 2017, 7, 1915.	1.6	6
50	A proposal for a magnetostriction-assisted all-spin logic device. , 2017, , .		4
51	Interconnect design for evolutionary, and revolutionary transistor technologies. , 2017, , .		4
52	Electrical-Spin Transduction for CMOS-Spintronic Interface and Long-Range Interconnects. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2017, 3, 47-55.	1.1	7
53	An overview of 3D integrated circuits. , 2017, , .		9
54	Overview of the Interconnect Problem. , 2017, , 3-36.		1

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55	An Expanded Benchmarking of Beyond-CMOS Devices Based on Boolean and Neuromorphic Representative Circuits. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2017, 3, 101-110.	1.1	35
56	A Nonvolatile Fast-Read Two-Transistor SRAM Based on Spintronic Devices. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2017, 3, 93-100.	1.1	7
57	Analytical models for coupling reliability in identical two-magnet systems during slow reversals. Journal of Applied Physics, 2017, 122, .	1.1	5
58	Proposal for nanoscale cascaded plasmonic majority gates for non-Boolean computation. Scientific Reports, 2017, 7, 17866.	1.6	19
59	Strain-Mediated Magnetization Reversal Through Spin-Transfer Torque. IEEE Transactions on Magnetics, 2017, 53, 1-8.	1.2	10
60	Performace modeling and optimization for on-chip interconnects in memory arrays. , 2016, , .		0
61	Performance modeling and optimization for on-chip interconnects in cross-bar ReRAM memory arrays. , 2016, , .		0
62	Impact of spintronics transducers on the performance of spin wave logic circuit. , 2016, , .		5
63	Non-Boolean Computing Benchmarking for Beyond-CMOS Devices Based on Cellular Neural Network. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2016, 2, 36-43.	1.1	30
64	A Probability-Density Function Approach to Capture the Stochastic Dynamics of the Nanomagnet and Impact on Circuit Performance. IEEE Transactions on Electron Devices, 2016, 63, 4119-4126.	1.6	8
65	Smart Detector Cell: A Scalable All-Spin Circuit for Low Power Non-Boolean Pattern Recognition. IEEE Nanotechnology Magazine, 2016, 15, 356-366.	1.1	7
66	Impact of On-Chip Interconnect on the Performance of 3-D Integrated Circuits With Through-Silicon Vias: Part II. IEEE Transactions on Electron Devices, 2016, 63, 2510-2516.	1.6	7
67	Impact of On-Chip Interconnect on the Performance of 3-D Integrated Circuits With Through Silicon Vias: Part I. IEEE Transactions on Electron Devices, 2016, 63, 2503-2509.	1.6	5
68	Performance analyses and benchmarking for spintronic devices and interconnects. , 2016, , .		2
69	Performance modeling and optimization for on-chip interconnects in STT-MRAM memory arrays. , 2016, , .		1
70	A Proposal for Energy-Efficient Cellular Neural Network Based on Spintronic Devices. IEEE Nanotechnology Magazine, 2016, 15, 820-827.	1.1	34
71	Ultra-High Mobility in Dielectrically Pinned CVD Graphene. IEEE Journal of the Electron Devices Society, 2016, 4, 466-472.	1.2	5
72	Spin-based interconnect technology and design. , 2016, , .		0

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73	Interconnect design for conventional and emerging charge-based devices. , 2016, , .		0
74	Performance modeling and optimization for on-chip interconnects in 3D memory arrays. , 2016, , .		0
75	Device/system performance modeling of stacked lateral NWFET logic. , 2016, , .		0
76	Impact of interconnect variability on circuit performance in advanced technology nodes. , 2016, , .		8
77	A Model Study of an Error-Free Magnetization Reversal Through Dipolar Coupling in a Two-Magnet System. IEEE Transactions on Magnetics, 2016, 52, 1-12.	1.2	8
78	Scaling Limits on All-Spin Logic. IEEE Transactions on Magnetics, 2016, 52, 1-4.	1.2	9
79	Interconnect Design and Benchmarking for Charge-Based Beyond-CMOS Device Proposals. IEEE Electron Device Letters, 2016, 37, 508-511.	2.2	11
80	Analysis of coupling strength in multi-domain magneto-systems. , 2015, , .		5
81	Phase-dependent deterministic switching of magnetoelectric spin wave detector in the presence of thermal noise via compensation of demagnetization. Applied Physics Letters, 2015, 107, 192404.	1.5	8
82	Performace modeling and optimization for on-chip interconnects in memory arrays. , 2015, , .		0
83	Adapting Interconnect Technology to Multigate Transistors for Optimum Performance. IEEE Transactions on Electron Devices, 2015, 62, 3938-3944.	1.6	22
84	System-Level Variation Analysis for Interconnection Networks at Sub-10-nm Technology Nodes Using Multiple Patterning Techniques. IEEE Transactions on Electron Devices, 2015, 62, 2071-2077.	1.6	9
85	A Paradigm Shift in Local Interconnect Technology Design in the Era of Nanoscale Multigate and Gate-All-Around Devices. IEEE Electron Device Letters, 2015, 36, 274-276.	2.2	24
86	Evaluating Chip-Level Impact of Cu/Low-<inline-formula> <tex-math notation="LaTeX">$kappa $ </tex-math></inline-formula> Performance Degradation on Circuit Performance at Future Technology Nodes. IEEE Transactions on Electron Devices, 2015, 62, 940-946.	1.6	12
87	Interconnects for All-Spin Logic Using Automotion of Domain Walls. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2015, 1, 49-57.	1.1	8
88	Non-volatile Clocked Spin Wave Interconnect for Beyond-CMOS Nanomagnet Pipelines. Scientific Reports, 2015, 5, 9861.	1.6	61
89	Technology/circuit co-optimization and benchmarking for graphene interconnects at Sub-10nm technology node. , 2015, , .		0
90	Technology/Circuit/System Co-Optimization and Benchmarking for Multilayer Graphene Interconnects at Sub-10-nm Technology Node. IEEE Transactions on Electron Devices, 2015, 62, 1530-1536.	1.6	18

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91	A Fast System-Level Design Methodology for Heterogeneous Multi-Core Processors Using Emerging Technologies. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2015, 5, 75-87.	2.7	5
92	Compact Physical Model for Crosstalk in Spin-Wave Interconnects. IEEE Transactions on Electron Devices, 2015, 62, 3863-3869.	1.6	3
93	Technology/System Codesign and Benchmarking for Lateral and Vertical GAA Nanowire FETs at 5-nm Technology Node. IEEE Transactions on Electron Devices, 2015, 62, 3125-3132.	1.6	36
94	Pipeline design in spintronic circuits. , 2014, , .		2
95	System level analysis and benchmarking of graphene interconnects for low-power applications. , 2014, , .		0
96	Interactive visualizations for teaching quantum mechanics and semiconductor physics. , 2014, , .		4
97	System-level chip/package co-design for multi-core processors implemented with power-gating technique. , 2014, , .		0
98	Wiring resource minimization for physically-complex Network-on-Chip architectures. , 2014, , .		0
99	Pipeline design in spintronic circuits. , 2014, , .		0
100	System-level variation analysis for interconnection networks. , 2014, , .		2
101	Impact of dimensional scaling and size effects on beyond CMOS All-Spin Logic interconnects. , 2014, , .		5
102	A Proposal for a Novel Hybrid Interconnect Technology for the End of Roadmap. IEEE Electron Device Letters, 2014, 35, 250-252.	2.2	41
103	Circuit Simulation of Magnetization Dynamics and Spin Transport. IEEE Transactions on Electron Devices, 2014, 61, 1553-1560.	1.6	37
104	SPICE Circuit Modeling of PMA Spin Wave Bus Excited Using Magnetoelectric Effect. IEEE Transactions on Magnetics, 2014, 50, 1-11.	1.2	22
105	An analytical approach to system-level variation analysis and optimization for multi-core processor. , 2014, , .		1
106	SPICE models for metallic all-spin-logic devices and interconnects. , 2014, , .		0
107	Impact of size effects in local interconnects for future technology nodes: A study based on full-chip layouts. , 2014, , .		23
108	Airgap Interconnects: Modeling, Optimization, and Benchmarking for Backplane, PCB, and Interposer Applications. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2014, 4, 1335-1346.	1.4	30

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109	BEOL Scaling Limits and Next Generation Technology Prospects. , 2014, , .		11
110	Design and Analysis of Copper and Aluminum Interconnects for All-Spin Logic. IEEE Transactions on Electron Devices, 2014, 61, 2905-2911.	1.6	30
111	Design and Analysis of Si Interconnects for All-Spin Logic. IEEE Transactions on Magnetics, 2014, 50, 1-13.	1.2	29
112	Performance modeling for emerging interconnect technologies in CMOS and beyond-CMOS circuits. , 2014, , .		3
113	System-level analysis for 3D interconnection networks. , 2013, , .		5
114	Review of multi-layer graphene nanoribbons for on-chip interconnect applications. , 2013, , .		2
115	Impact of conventional and emerging interconnects on the circuit performance of various post-CMOS devices. , 2013, , .		9
116	System-level optimization and benchmarking for InAs nanowire based gate-all-around tunneling FETs. , 2013, , .		1
117	Compact modeling and optimization of fine-pitch interconnects for silicon interposers. , 2013, , .		2
118	Roles of Doping, Temperature, and Electric Field on Spin Transport Through Semiconducting Channels in Spin Valves. IEEE Nanotechnology Magazine, 2013, 12, 796-805.	1.1	8
119	Cu Interconnect Limitations and Opportunities for SWNT Interconnects at the End of the Roadmap. IEEE Transactions on Electron Devices, 2013, 60, 374-382.	1.6	119
120	Cu/Low-k Interconnect Technology Design and Benchmarking for Future Technology Nodes. IEEE Transactions on Electron Devices, 2013, 60, 4041-4047.	1.6	10
121	Communicating Novel Computational State Variables: Post-CMOS Logic. IEEE Nanotechnology Magazine, 2013, 7, 15-23.	0.9	2
122	Evaluation of the Potential Performance of Graphene Nanoribbons as On-Chip Interconnects. Proceedings of the IEEE, 2013, 101, 1740-1765.	16.4	105
123	Hydrogenation of Graphene Nanoribbon Edges: Improvement in Carrier Transport. IEEE Electron Device Letters, 2013, 34, 707-709.	2.2	9
124	Performance modeling for interconnects for conventional and emerging switches. , 2013, , .		0
125	Design and fabrication of ultra low-loss, high-performance 3D chip-chip air-clad interconnect pathway. , 2013, , .		5
126	Impact of Dimensional Scaling and Size Effects on Spin Transport in Copper and Aluminum Interconnects. IEEE Transactions on Electron Devices, 2013, 60, 3913-3919.	1.6	34

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127	Interconnect analysis in spin-torque devices: Performance modeling, sptimal repeater insertion, and circuit-size limits. , 2012, , .		8
128	Power Delivery for 3-D Chip Stacks: Physical Modeling and Design Implication. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2012, 2, 852-859.	1.4	26
129	Analytical models for the frequency response of multi-layer graphene nanoribbon interconnects. , 2012, , .		11
130	Design and fabrication of low-loss horizontal and vertical interconnect links using air-clad transmission lines and through silicon vias. , 2012, , .		12
131	System-level performance optimization and benchmarking for on-chip graphene interconnects. , 2012, , .		5
132	Circuit-technology co-optimization of heterogeneous hierarchical network-on-chips. , 2012, , .		0
133	Performance and Energy-per-Bit Modeling of Multilayer Graphene Nanoribbon Conductors. IEEE Transactions on Electron Devices, 2012, 59, 2753-2761.	1.6	87
134	System-level design and performance modeling for multilevel interconnect networks for carbon nanotube field-effect transistors. , 2012, , .		1
135	System-level optimization and benchmarking of graphene PN junction logic system based on empirical CPI model. , 2012, , .		6
136	Compact modeling and performance optimization of 3D chip-to-chip interconnects with transmission lines, vias and discontinuities. , 2012, , .		3
137	Device- and system-level performance modeling for graphene P-N junction logic. , 2012, , .		8
138	Transport of Novel State Variables. , 2012, , 113-136.		0
139	Graphene Nanoribbon Spin Interconnects for Nonlocal Spin-Torque Circuits: Comparison of Performance and Energy Per Bit With CMOS Interconnects. IEEE Transactions on Electron Devices, 2012, 59, 51-59.	1.6	16
140	Multilevel interconnect networks for the end of the roadmap: Conventional Cu/low-k and emerging carbon based interconnects. , 2011, , .		2
141	On physical limits and challenges of interconnects for spin devices. , 2011, , .		1
142	Interconnection aspects of spin torque devices: Delay, energy-per-bit, and circuit size modeling. , 2011, , .		3
143	Ultralow-Power Single-Wall Carbon Nanotube Interconnects for Subthreshold Circuits. IEEE Nanotechnology Magazine, 2011, 10, 99-101.	1.1	25
144	Power Aware Post-manufacture Tuning of Analog Nanocircuits. , 2011, , .		3

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145	Interconnect performance and energy-per-bit for post-CMOS logic circuits: Modeling, analysis, and comparison with CMOS logic. , 2011, , .		1
146	Modeling, optimization and benchmarking of chip-to-chip electrical interconnects with low loss air-clad dielectrics. , 2011, , .		9
147	Modeling and optimization for multi-layer graphene nanoribbon conductors. , 2011, , .		21
148	Modeling Interconnects for Post-CMOS Devices and Comparison With Copper Interconnects. IEEE Transactions on Electron Devices, 2011, 58, 1319-1328.	1.6	13
149	Interconnect Network Analysis of Many-Core Chips. IEEE Transactions on Electron Devices, 2011, 58, 2831-2837.	1.6	9
150	Interconnects for Novel State Variables: Performance Modeling and Device and Circuit Implications. IEEE Transactions on Electron Devices, 2010, 57, 2711-2718.	1.6	18
151	Optimal Global Interconnects for Networks-on-Chip in Many-Core Architectures. IEEE Electron Device Letters, 2010, 31, 290-292.	2.2	7
152	Bandwidth, delay and energy aware optimization of global interconnects for many-core architectures. , 2010, , .		1
153	Work in progress — Carbon nanomaterials: A platform to teach fundamentals of nanoelectronics. , 2010, , .		0
154	Evolutionary and revolutionary interconnect technologies for performance enhancement of subthreshold circuits. , 2010, , .		4
155	Physical limitations on delay and energy dissipation of interconnects for post-CMOS devices. , 2010, , .		6
156	Compact Physics-Based Circuit Models for Graphene Nanoribbon Interconnects. IEEE Transactions on Electron Devices, 2009, 56, 1822-1833.	1.6	222
157	Carbon Nanotube Interconnects. Annual Review of Materials Research, 2009, 39, 255-275.	4.3	111
158	Performance Modeling for Carbon Nanotube Interconnects. Integrated Circuits and Systems, 2009, , 163-190.	0.2	13
159	Performance Modeling for Single- and Multiwall Carbon Nanotubes as Signal and Power Interconnects in Gigascale Systems. IEEE Transactions on Electron Devices, 2008, 55, 2574-2582.	1.6	141
160	Physical models for electron transport in graphene nanoribbons and their junctions. , 2008, , .		0
161	Electron Transport Modeling for Junctions of Zigzag and Armchair Graphene Nanoribbons (GNRs). IEEE Electron Device Letters, 2008, 29, 497-499.	2.2	24
162	Compact physical models for chip and package power and ground distribution networks for gigascale integration (GSI). , 2008, , .		4

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163	Performance Benchmarking for Graphene Nanoribbon, Carbon Nanotube, and Cu Interconnects. , 2008, , .		53
164	3D heterogeneous integrated systems: Liquid cooling, power delivery, and implementation. , 2008, , .		78
165	Carbon nanotube interconnects. , 2007, , .		18
166	Compact Physical Models for Power Supply Noise and Chip/Package Co-Design of Gigascale Integration. , 2007, , .		17
167	Performance Modeling for Carbon Nanotube Interconnects in On-Chip Power Distribution. , 2007, , .		17
168	Performance modeling and optimization for single- and multi-wall carbon nanotube interconnects. Proceedings - Design Automation Conference, 2007, , .	0.0	10
169	Intsim: a CAD tool for optimization of multilevel interconnect networks. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	15
170	Physical Modeling of Temperature Coefficient of Resistance for Single- and Multi-Wall Carbon Nanotube Interconnects. IEEE Electron Device Letters, 2007, 28, 135-138.	2.2	144
171	Power Delivery for 3D Chip Stacks: Physical Modeling and Design Implication. , 2007, , .		96
172	Physical Model for Power Supply Noise and Chip/Package Co-Design in Gigascale Systems with the Consideration of Hot Spots. , 2007, , .		9
173	Conductance Modeling for Graphene Nanoribbon (GNR) Interconnects. IEEE Electron Device Letters, 2007, 28, 428-431.	2.2	229
174	Design and Optimization for Nanoscale Power Distribution Networks in Gigascale Systems. , 2007, , .		7
175	Design and Performance Modeling for Single-Walled Carbon Nanotubes as Local, Semiglobal, and Global Interconnects in Gigascale Integrated Systems. IEEE Transactions on Electron Devices, 2007, 54, 26-37.	1.6	232
176	Performance Modeling and Optimization for Single- and Multi-Wall Carbon Nanotube Interconnects. Proceedings - Design Automation Conference, 2007, , .	0.0	3
177	Compact physical models for multiwall carbon-nanotube interconnects. IEEE Electron Device Letters, 2006, 27, 338-340.	2.2	311
178	Chip-level and Input/Output Interconnects for Gigascale SOCs: Limits and Opportunities. , 2006, , .		1
179	Impact of electron-phonon scattering on the performance of carbon nanotube interconnects for GSI. IEEE Electron Device Letters, 2005, 26, 476-478.	2.2	54
180	Monolayer metallic nanotube interconnects: promising candidates for short local interconnects. IEEE Electron Device Letters, 2005, 26, 544-546.	2.2	74

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181	Performance comparison between carbon nanotube and copper interconnects for gigascale integration (GSI). IEEE Electron Device Letters, 2005, 26, 84-86.	2.2	270
182	Optimal global interconnects for GSI. IEEE Transactions on Electron Devices, 2003, 50, 980-987.	1.6	46
183	Interconnect considerations. , 0, , 381-412.		1