Ulf Schlichtmann

List of Publications by Year
in descending order

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259	2,984	430874	414414
papers	citations	18 h-index	32 g-index

263	263	263	1393
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	The Bistable Ring PUF: A new architecture for strong Physical Unclonable Functions. , 2011, , .		156
2	Kraftwerk2â€"A Fast Force-Directed Quadratic Placement Approach Using an Accurate Net Model. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1398-1411.	2.7	151
3	The Sizing Rules Method for CMOS and Bipolar Analog Integrated Circuit Synthesis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 2209-2222.	2.7	124
4	Abacus. , 2008, , .		124
5	A Successive Approach to Compute the Bounded Pareto Front of Practical Multiobjective Optimization Problems. SIAM Journal on Optimization, 2009, 20, 915-934.	2.0	103
6	Aging analysis of circuit timing considering NBTI and HCI. , 2009, , .		91
7	Design and architectures for dependable embedded systems. , 2011, , .		73
8	Comprehensive Generation of Hierarchical Placement Rules for Analog Integrated Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 180-193.	2.7	53
9	Deterministic analog circuit placement using hierarchically bounded enumeration and enhanced shape functions. , 2008, , .		49
10	Predicting future product performance. , 2013, , .		42
11	Safety Evaluation of Automotive Electronics Using Virtual Prototypes. , 2014, , .		42
12	Aging analysis at gate and macro cell level. , 2010, , .		37
13	A compact model for NBTI degradation and recovery under use-profile variations and its application to aging analysis of digital integrated circuits. Microelectronics Reliability, 2014, 54, 1083-1089.	1.7	37
14	Aging-aware Lifetime Enhancement for Memristor-based Neuromorphic Computing. , 2019, , .		37
15	Columba 2.0: A Co-Layout Synthesis Tool for Continuous-Flow Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1588-1601.	2.7	36
16	Columba. , 2016, , .		35
17	Storage and Caching: Synthesis of Flow-Based Microfluidic Biochips. IEEE Design and Test, 2015, 32, 69-75.	1.2	34
18	Fast power estimation of large circuits. IEEE Design and Test of Computers, 1996, 13, 70-78.	1.0	33

#	Article	IF	Citations
19	Reliability-aware synthesis for flow-based microfluidic biochips by dynamic-device mapping. , 2015, , .		33
20	TimingCamouflage: Improving circuit security against counterfeiting by unconventional timing. , 2018, , .		29
21	Reliability-Aware Synthesis With Dynamic Device Mapping and Fluid Routing for Flow-Based Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1981-1994.	2.7	28
22	Testing microfluidic Fully Programmable Valve Arrays (FPVAs). , 2017, , .		28
23	Functional multiple-output decomposition with application to technology mapping for lookup table-based FPGAs. ACM Transactions on Design Automation of Electronic Systems, 1999, 4, 313-350.	2.6	27
24	Resilience Articulation Point (RAP): Cross-layer dependability modeling for nanometer system-on-chip resilience. Microelectronics Reliability, 2014, 54, 1066-1074.	1.7	27
25	Reliability challenges for electric vehicles. , 2013, , .		26
26	Efficiently analyzing the impact of aging effects on large integrated circuits. Microelectronics Reliability, 2012, 52, 1546-1552.	1.7	25
27	DeeperThings: Fully Distributed CNN Inference on Resource-Constrained Edge Devices. International Journal of Parallel Programming, 2021, 49, 600-624.	1.5	25
28	Statistical Training for Neuromorphic Computing using Memristor-based Crossbars Considering Process Variations and Noise. , 2020, , .		24
29	A CPPLL hierarchical optimization methodology considering jitter, power and locking time. , 2006, , .		22
30	Fully Distributed Deep Learning Inference on Resource-Constrained Edge Devices. Lecture Notes in Computer Science, 2019, , 77-90.	1.3	22
31	A Cross-Layer Technology-Based Study of How Memory Errors Impact System Resilience. IEEE Micro, 2013, 33, 46-55.	1.8	21
32	Automatic ILP-based Firewall Insertion for Secure Application-Specific Networks-on-Chip. , 2015, , .		20
33	MiniControl. , 2019, , .		20
34	Physical Synthesis of Flow-Based Microfluidic Biochips Considering Distributed Channel Storage. , 2019, , .		20
35	Hamming-distance-based valve-switching optimization for control-layer multiplexing in flow-based microfluidic biochips. , 2017, , .		19
36	Transport or Store?. , 2017, , .		19

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37	Multicontrol: Advanced Control-Logic Synthesis for Flow-Based Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2489-2502.	2.7	19
38	Lifetime Enhancement for RRAM-based Computing-In-Memory Engine Considering Aging and Thermal Effects. , 2020, , .		19
39	Sieve-valve-aware Synthesis of Flow-based Microfluidic Biochips Considering Specific Biological Execution Limitations. , 2016, , .		19
40	Deterministic approaches to analog performance space exploration (PSE). , 2005, , .		18
41	Application of mismatched Cellular Nonlinear Networks for Physical Cryptography. , 2010, , .		18
42	Control-Flow-Driven Source Level Timing Annotation for Embedded Software Models on Transaction Level. , 2011, , .		18
43	Iterative timing analysis based on nonlinear and interdependent flipflop modelling. IET Circuits, Devices and Systems, 2012, 6, 330.	1.4	18
44	PROTON: An automatic place-and-route tool for optical Networks-on-Chip. , 2013, , .		18
45	Statistical Timing Analysis and Criticality Computation for Circuits With Post-Silicon Clock Tuning Elements. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1784-1797.	2.7	18
46	Control-fluidic CoDesign for paper-based digital microfluidic biochips. , 2016, , .		18
47	EffiTest. , 2016, , .		18
48	Towards Reliable and Secure Post-Quantum Co-Processors based on RISC-V. , 2019, , .		18
49	DCSA: Distributed Channel-Storage Architecture for Flow-Based Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 115-128.	2.7	18
50	Deterministic Synthesis of Hybrid Application-Specific Network-on-Chip Topologies. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1503-1516.	2.7	17
51	Monitoring of aging in integrated circuits by identifying possible critical paths. Microelectronics Reliability, 2014, 54, 1075-1082.	1.7	17
52	Design-Phase Buffer Allocation for Post-Silicon Clock Binning by Iterative Learning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 392-405.	2.7	17
53	Computer-aided Design Techniques for Flow-based Microfluidic Lab-on-a-chip Systems. ACM Computing Surveys, 2022, 54, 1-29.	23.0	17
54	Towards Electrical, Integrated Implementations of SIMPL Systems. Lecture Notes in Computer Science, 2010, , 277-292.	1.3	17

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55	Pareto optimization of analog circuits considering variability. International Journal of Circuit Theory and Applications, 2009, 37, 283-299.	2.0	16
56	Schedulability Analysis for Processors with Aging-Aware Autonomic Frequency Scaling. , 2012, , .		16
57	On Timing Model Extraction and Hierarchical Statistical Timing Analysis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 367-380.	2.7	16
58	PROTON+. ACM Journal on Emerging Technologies in Computing Systems, 2016, 12, 1-28.	2.3	16
59	The extendable translating instruction set simulator (ETISS) interlinked with an MDA framework for fast RISC prototyping. , 2017, , .		16
60	Multi-channel and fault-tolerant control multiplexing for flow-based microfluidic biochips. , 2018, , .		16
61	CustomTopo. , 2018, , .		16
62	Countering variations and thermal effects for accurate optical neural networks. , 2020, , .		16
63	PieceTimer. , 2016, , .		15
64	Fast statistical timing analysis for circuits with Post-Silicon Tunable clock buffers. , 2011, , .		14
65	Goldilocks failures: Not too soft, not too hard. , 2012, , .		14
66	Component-Oriented High-level Synthesis for Continuous-Flow Microfluidics Considering Hybrid-Scheduling. , 2017, , .		14
67	Pressure-Aware Control Layer Optimization for Flow-Based Microfluidic Biochips. IEEE Transactions on Biomedical Circuits and Systems, 2017, 11, 1488-1499.	4.0	14
68	Columba S. , 2018, , .		14
69	Virtualsync. , 2018, , .		14
70	PlanarONoC. , 2018, , .		14
71	Workload- and Instruction-Aware Timing Analysis. , 2014, , .		13
72	CoSyn: Efficient single-cell analysis using a hybrid microfluidic platform. , 2017, , .		13

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73	Flow-Based Microfluidic Biochips With Distributed Channel Storage: Synthesis, Physical Design, and Wash Optimization. IEEE Transactions on Computers, 2022, 71, 464-478.	3.4	13
74	Bayesian Inference Based Robust Computing on Memristor Crossbar. , 2021, , .		13
75	Pareto optimization of analog circuits considering variability. , 2007, , .		12
76	Trade-Off Design of Analog Circuits using Goal Attainment and "Wave Front" Sequential Quadratic Programming. , 2007, , .		12
77	Current source modeling for power and timing analysis at different supply voltages. , 2012, , .		12
78	Where formal verification can help in functional safety analysis. , 2016, , .		12
79	EffiTest2: Efficient Delay Test and Prediction for Post-Silicon Clock Skew Configuration Under Process Variations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 705-718.	2.7	12
80	Automatic generation of hierarchical placement rules for analog integrated circuits. , 2010, , .		12
81	PLATON. , 2016, , .		12
82	Sampling-based Buffer Insertion for Post-Silicon Yield Improvement under Process Variability. , 2016, , .		12
83	Technology-aware system failure analysis in the presence of soft errors by Mixture Importance Sampling. , 2013, , .		11
84	Multivariate Modeling of Variability Supporting Non-Gaussian and Correlated Parameters. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 197-210.	2.7	11
85	Performance and accuracy in soft-error resilience evaluation using the multi-level processor simulator ETISS-ML. , 2018, , .		11
86	Machine learning and structural characteristics for reverse engineering. , 2019, , .		11
87	Wavelength-Routed Optical NoCs: Design and EDA â€" State of the Art and Future Directions: Invited Paper. , 2019, , .		11
88	From biochips to quantum circuits: computer-aided design for emerging technologies. , 2016, , .		10
89	Machine learning and structural characteristics for reverse engineering. The Integration VLSI Journal, 2020, 72, 1-12.	2.1	10
90	PSION. , 2019, , .		10

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91	Digital design at a crossroads How to make statistical design methodologies industrially relevant. , 2009, , .		9
92	An Analysis of Industrial SRAM Test Resultsâ€"A Comprehensive Study on Effectiveness and Classification of March Test Algorithms. IEEE Design and Test, 2014, 31, 42-53.	1.2	9
93	FinFET-based product performance: Modeling and evaluation of standard cells in FinFET technologies. Microelectronics Reliability, 2016, 61, 30-34.	1.7	9
94	From Process Variations to Reliability: A Survey of Timing of Digital Circuits in the Nanometer Era. IPSJ Transactions on System LSI Design Methodology, 2018, 11, 2-15.	0.8	9
95	PSION+: Combining Logical Topology and Physical Layout Optimization for Wavelength-Routed ONoCs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 5197-5210.	2.7	9
96	PathDriver+: Enhanced Path-Driven Architecture Design for Flow-Based Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2185-2198.	2.7	9
97	PathDriver. , 2020, , .		9
98	Reliable Memristor-based Neuromorphic Design Using Variation- and Defect-Aware Training. , 2021, , .		9
99	Extremely low-power logic. , 0, , .		8
100	Pareto-Front Computation and Automatic Sizing of CPPLLs. , 2007, , .		8
101	CIRCUIT-BASED APPROACHES TO SIMPL SYSTEMS. Journal of Circuits, Systems and Computers, 2011, 20, 107-123.	1.5	8
102	Non-intrusive trace & debug noc architecture with accurate timestamping for GALS SoCs. , 2012, , .		8
103	Timing Verification for Adaptive Integrated Circuits. , 2015, , .		8
104	Fault-tolerant valve-based microfluidic routing fabric for droplet barcoding in single-cell analysis. , 2018, , .		8
105	Synthesis of a Cyberphysical Hybrid Microfluidic Platform for Single-Cell Analysis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1237-1250.	2.7	8
106	Block-Flushing: A Block-based Washing Algorithm for Programmable Microfluidic Devices. , 2019, , .		8
107	Maximizing the Communication Parallelism for Wavelength-Routed Optical Networks-On-Chips. , 2020, , .		8
108	Fast and waveform independent characterization of current source models. , 2009, , .		7

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109	A Spectral Clustering Approach to Application-Specific Network-on-Chip Synthesis. , 2013, , .		7
110	System C-based multi-level error injection for the evaluation of fault-tolerant systems. , 2014, , .		7
111	Fault-tolerant embedded control systems for unreliable hardware. , 2014, , .		7
112	Emulation of an ASIC power and temperature monitoring system (eTPMon) for FPGA prototyping. Microprocessors and Microsystems, 2017, 50, 90-101.	2.8	7
113	ETISS-ML: A multi-level instruction set simulator with RTL-level fault injection support for the evaluation of cross-layer resiliency techniques. , 2018, , .		7
114	Overview of 2019 CAD Contest at ICCAD. , 2019, , .		7
115	Hierarchical control flow matching for source-level simulation of embedded software. , 2012, , .		6
116	Fast Cache Simulation for Host-Compiled Simulation of Embedded Software. , 2013, , .		6
117	ILP-Based Alleviation of Dense Meander Segments With Prioritized Shifting and Progressive Fixing in PCB Routing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1000-1013.	2.7	6
118	Generative adversarial network based scalable on-chip noise sensor placement. , 2017, , .		6
119	Graph-Grammar-Based IP-Integration (GRIP)â€"An EDA Tool for Software-Defined SoCs. ACM Transactions on Design Automation of Electronic Systems, 2018, 23, 1-26.	2.6	6
120	Efficient spanning-tree-based test pattern generation for Programmable Microfluidic Devices. Microelectronics Journal, 2018, 79, 38-45.	2.0	6
121	Synthesis of Reconfigurable Flow-Based Biochips for Scalable Single-Cell Screening. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 2255-2270.	2.7	6
122	Reliable and Robust RRAM-based Neuromorphic Computing. , 2020, , .		6
123	Ultra-Low-Power Design: Device and Logic Design Approaches. , 2004, , 1-20.		5
124	Robustness measurement of integrated circuits and its adaptation to aging effects. Microelectronics Reliability, 2014, 54, 1058-1065.	1.7	5
125	Integrating aging aware timing analysis into a commercial STA tool. , 2015, , .		5
126	Cross-Layer Resilience. , 2019, , .		5

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127	VOM: Flow-Path Validation and Control-Sequence Optimization for Multilayered Continuous-Flow Microfluidic Biochips. , 2019, , .		5
128	Integrated Control-Fluidic Codesign Methodology for Paper-Based Digital Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 613-625.	2.7	5
129	Transport-Free Module Binding for Sample Preparation using Microfluidic Fully Programmable Valve Arrays. , 2020, , .		5
130	TimingCamouflage+: Netlist Security Enhancement With Unconventional Timing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4482-4495.	2.7	5
131	BigIntegr: One-Pass Architectural Synthesis for Continuous-Flow Microfluidic Lab-on-a-Chip Systems. , 2021, , .		5
132	Sizing Rules for Bipolar Analog Circuit Design. , 2008, , .		4
133	Fast statistical timing analysis of latch-controlled circuits for arbitrary clock periods. , 2010, , .		4
134	Removal of unnecessary context switches from the systemc simulation kernel for fast VP simulation. , 2011, , .		4
135	Automated construction of a cycle-approximate transaction level model of a memory controller. , 2012, , .		4
136	Robustness validation of integrated circuits and systems. , 2012, , .		4
137	A greedy approach for latency-bounded deadlock-free routing path allocation for application-specific NoCs. , 2013, , .		4
138	Analytical Timing Estimation for Temporally Decoupled TLMs Considering Resource Conflicts. , 2013, , .		4
139	Runtime Adaptation of Application Execution under Thermal and Power Constraints in Massively Parallel Processor Arrays. , 2015, , .		4
140	Sortex: Efficient timing-driven synthesis of reconfigurable flow-based biochips for scalable single-cell screening. , 2017, , .		4
141	Frontiers of timing. , 2017, , .		4
142	Thermal-Aware Placement and Routing for 3D Optical Networks-on-Chips. , 2018, , .		4
143	An Efficient Fault-Tolerant Valve-Based Microfluidic Routing Fabric for Droplet Barcoding in Single-Cell Analysis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 359-372.	2.7	4
144	Test Generation for Flow-Based Microfluidic Biochips With General Architectures. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2530-2543.	2.7	4

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145	A Pulse-width Modulation Neuron with Continuous Activation for Processing-In-Memory Engines. , 2020, , .		4
146	An Efficient Programming Framework for Memristor-based Neuromorphic Computing. , 2021, , .		4
147	Fault Injection for Test-Driven Development of Robust SoC Firmware. Transactions on Embedded Computing Systems, 2018, 17, 1-26.	2.9	4
148	Predicting Memory Compiler Performance Outputs Using Feed-forward Neural Networks. ACM Transactions on Design Automation of Electronic Systems, 2020, 25, 1-19.	2.6	4
149	Machine Learning Approaches for Efficient Design Space Exploration of Application-Specific NoCs. ACM Transactions on Design Automation of Electronic Systems, 2020, 25, 1-27.	2.6	4
150	Partial Sharing Neural Networks for Multi-Target Regression on Power and Performance of Embedded Memories. , 2020, , .		4
151	PSION 2. , 2020, , .		4
152	An FPGA-based Approach to Evaluate Thermal and Resource Management Strategies of Many-core Processors. Transactions on Architecture and Code Optimization, 2022, 19, 1-24.	2.0	4
153	Fast evaluation of analog circuit structures by polytopal approximations. , 0, , .		3
154	A random and pseudo-gradient approach for analog circuit sizing with non-uniformly discretized parameters. , 2008, , .		3
155	Sizing rules for bipolar analog circuit design. , 2008, , .		3
156	Aging-aware Timing Analysis of Combinatorial Circuits on Gate Level. IT - Information Technology, 2010, 52, 181-187.	0.9	3
157	Program-aware circuit level timing analysis. , 2011, , .		3
158	Characterization of the bistable ring PUF. , 2012, , .		3
159	A Virtual Prototyping Platform for Real-time Systems with a Case Study for a Two-wheeled Robot. , 2013, , .		3
160	Post-route alleviation of dense meander segments in high-performance printed circuit boards. , 2013, , .		3
161	Dark silicon management: an integrated and coordinated cross-layer approach. IT - Information Technology, 2016, 58, 297-307.	0.9	3
162	Embedded software reliability testing by unit-level fault injection. , 2016, , .		3

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163	20nm FinFET-based SRAM cell: Impact of variability and design choices on performance characteristics. , 2017, , .		3
164	Wavefront-MCTS. , 2018, , .		3
165	Design-for-testability for continuous-flow microfluidic biochips. , 2018, , .		3
166	Fault Localization in Programmable Microfluidic Devices. , 2019, , .		3
167	ColoriSens: An open-source and low-cost portable color sensor board for microfluidic integration with wireless communication and fluorescence detection. HardwareX, 2022, 11, e00312.	2.2	3
168	Systems are made from transistors: UDSM technology creates new challenges for library and IC development. , 0, , .		2
169	Optimization of SC ΣΔ modulators based on worst-case-aware Pareto-optimal fronts. , 2007, , .		2
170	Statistical Timing Analysis for Latch-Controlled Circuits With Reduced Iterations and Graph Transformations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1670-1683.	2.7	2
171	Emulation of an ASIC power and temperature monitor system for FPGA prototyping. , 2015, , .		2
172	GRIP. , 2015, , .		2
173	Fully synthesized time-to-digital converter for cellular transceivers. , 2016, , .		2
174	Fault injection at host-compiled level with static fault set reduction for SoC firmware robustness testing. , 2016, , .		2
175	Efficient Fault Injection for Embedded Systems: As Fast as Possible but as Accurate as Necessary. , 2018, , .		2
176	VirtualSync: Timing Optimization by Synchronizing Logic Waves with Sequential and Combinational Components as Delay Units. , 2018, , .		2
177	Electronic design automation for increased robustness in inkjet-printed electronics. Flexible and Printed Electronics, 2019, 4, 045002.	2.7	2
178	SRAM Design Exploration with Integrated Application-Aware Aging Analysis. , 2019, , .		2
179	Cloud Columba: Accessible Design Automation Platform for Production and Inspiration: Invited Paper. , 2019, , .		2
180	Driver Generation for IoT Nodes With Optimization of the Hardware/Software Interface. IEEE Embedded Systems Letters, 2020, 12, 66-69.	1.9	2

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181	RobustONoC: Fault-Tolerant Optical Networks-on-Chip with Path Backup and Signal Reflection. , 2021, , .		2
182	Deterministic approaches to analog performance space exploration (PSE). , 2005, , .		2
183	White-Box Current Source Modeling Including Parameter Variation and Its Application in Timing Simulation. Lecture Notes in Computer Science, 2011, , 200-210.	1.3	2
184	Special session: How secure are PUFs really? On the reach and limits of recent PUF attacks. , 2014, , .		2
185	ToPro: A Topology Projector and Waveguide Router for Wavelength-Routed Optical Networks-on-Chip. , 2021, , .		2
186	Reducing Routing Overhead by Self-Enabling Functional Path Ring Oscillators. , 2022, , .		2
187	Reliability analysis of digital circuits considering intrinsic noise. , 2011, , .		1
188	Methods of Parameter Variations. , 2012, , 91-179.		1
189	Examination of Process Parameter Variations. , 2012, , 69-89.		1
190	Post-route refinement for high-frequency PCBs considering meander segment alleviation. , 2013, , .		1
191	Memory access reconstruction based on memory allocation mechanism for source-level simulation of embedded software. , 2013, , .		1
192	Connecting different worlds - Technology abstraction for reliability-aware design and Test. , 2014, , .		1
193	Probabilistic standard cell modeling considering non-Gaussian parameters and correlations. , 2014, , .		1
194	Automation of FPGA performance monitoring and debugging Using IP-XACT and graph-grammars. , 2015, , .		1
195	Application-aware cross-layer reliability analysis and optimization. IT - Information Technology, 2015, 57, 159-169.	0.9	1
196	On the measurement of power grid robustness under load uncertainties. , 2016, , .		1
197	Safety evaluation based on virtual prototypes: Fault injection with multi-level processor models. , 2016, , .		1
198	Novel CMOS RFIC layout generation with concurrent device placement and fixed-length microstrip routing. , 2016, , .		1

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199	Efficient handling of the fault space in functional safety analysis utilizing formal methods. , 2016, , .		1
200	Model-based framework for networks-on-chip design space exploration. , 2017, , .		1
201	A Method for Phase Noise Analysis of RF Circuits. , 2017, , .		1
202	An Efficient Two-Phase ILP-Based Algorithm for Precise CMOS RFIC Layout Generation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1313-1326.	2.7	1
203	Application of machine learning methods in post-silicon yield improvement. , 2017, , .		1
204	Methodology for automated phase noise minimization in RF circuit interconnect trees. , 2017, , .		1
205	Automated Redirection of Hardware Accesses for Host-Compiled Software Simulation. , 2018, , .		1
206	Emulation of an ASIC Power, Temperature and Aging Monitor System for FPGA Prototyping. , 2018, , .		1
207	Automated Phase-Noise-Aware Design of RF Clock Distribution Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2395-2405.	3.1	1
208	On enabling diagnosis for 1-Pin Test fails in an industrial flow. , 2018, , .		1
209	Timing with Virtual Signal Synchronization for Circuit Performance and Netlist Security. , 2018, , .		1
210	Runtime Monitoring of Inter- and Intra-Thread Requirements on Embedded MPSoCs. , 2020, , .		1
211	Investigating the Inherent Soft Error Resilience of Embedded Applications by Full-System Simulation. , 2020, , .		1
212	A Distributed Hardware Monitoring System for Runtime Verification on Multi-Tile MPSoCs. Transactions on Architecture and Code Optimization, 2021, 18, 1-25.	2.0	1
213	Timing Modeling of Flipflops Considering Aging Effects. Lecture Notes in Computer Science, 2011, , 63-72.	1.3	1
214	A New Bounding Technique for Handling Arbitrary Correlations in Path-Based SSTA. Lecture Notes in Computer Science, 2009, , 167-177.	1.3	1
215	Timing model extraction for sequential circuits considering process variations. , 2009, , .		1
216	Deterministic Analog Placement by Enhanced Shape Functions. , 2011, , 95-145.		1

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217	Connecting different worlds - Technology abstraction for reliability-aware design and Test. , 2014, , .		1
218	Circuit Resilience Roadmap. , 2015, , 121-143.		1
219	RAP Modelâ€"Enabling Cross-Layer Analysis and Optimization for System-on-Chip Resilience. Embedded Systems, 2021, , 1-27.	0.6	1
220	Power crisis in SoC design: strategies for constructing low-power, high-performance SoC designs. , 0, , .		0
221	Statistical Timing Analysis using Weibull Waveform Modeling. , 2007, , .		0
222	Integrated circuit design: dealing with variations. Proceedings in Applied Mathematics and Mechanics, 2007, 7, 1070203-1070204.	0.2	0
223	Sensitivity based parameter reduction for statistical analysis of circuit performance. , 2009, , .		0
224	A free-shape router for analog and RF applications. , 2009, , .		0
225	On hierarchical statistical static timing analysis. , 2009, , .		0
226	Accurately timed transaction level models for virtual prototyping at high abstraction level. , 2012, , .		0
227	ICMAT 2011 â€“ Reliability and variability of semiconductor devices and ICs. Microelectronics Reliability, 2012, 52, 1531.	1.7	0
228	Application of Dempster-Shafer Theory to task mapping under epistemic uncertainty. , 2013, , .		0
229	Probabilistic standard cell modeling considering non-Gaussian parameters and correlations. , 2014, , .		0
230	Special section reliability and variability of devices for circuits and systems. Microelectronics Reliability, 2014, 54, 1057.	1.7	0
231	A Cross-Layer Approach to Measure the Robustness of Integrated Circuits. ACM Journal on Emerging Technologies in Computing Systems, 2015, 12, 1-22.	2.3	0
232	Beyond GORDIAN and Kraftwerk. , 2015, , .		0
233	Hardware-Accelerated Software Library Drivers Generation for IP-Centric SoC Designs. , 2016, , .		0
234	The next frontier in IC design: Determining (and optimizing) robustness and resilience of integrated circuits and systems. , 2016, , .		0

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