Kurt Keutzer

List of Publications by Year in descending order

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39 papers	3,935 citations	840776 11 h-index	996975 15 g-index
39 all docs	39 docs citations	39 times ranked	2543 citing authors

#	Article	IF	Citations
1	Emotional Semantics-Preserved and Feature-Aligned CycleGAN for Visual Emotion Adaptation. IEEE Transactions on Cybernetics, 2022, 52, 10000-10013.	9.5	6
2	A Review of Single-Source Deep Unsupervised Visual Domain Adaptation. IEEE Transactions on Neural Networks and Learning Systems, 2022, 33, 473-493.	11.3	123
3	Curriculum CycleGAN for Textual Sentiment Domain Adaptation with Multiple Sources. , 2021, , .		9
4	MADAN: Multi-source Adversarial Domain Aggregation Network for Domain Adaptation. International Journal of Computer Vision, 2021, 129, 2399-2424.	15.6	27
5	Cross-Domain Sentiment Classification with Contrastive Learning and Mutual Information Maximization. , 2021, , .		15
6	Emotion Recognition From Multiple Modalities: Fundamentals and methodologies. IEEE Signal Processing Magazine, 2021, 38, 59-73.	5.6	55
7	Multi-Source Distilling Domain Adaptation. Proceedings of the AAAI Conference on Artificial Intelligence, 2020, 34, 12975-12983.	4.9	91
8	Co-design of deep neural nets and neural net accelerators for embedded vision applications. IBM Journal of Research and Development, 2019, 63, 6:1-6:14.	3.1	3
9	SqueezeSegV2: Improved Model Structure and Unsupervised Domain Adaptation for Road-Object Segmentation from a LiDAR Point Cloud. , 2019, , .		349
10	CycleEmotionGAN: Emotional Semantic Consistency Preserved CycleGAN for Adapting Image Emotions. Proceedings of the AAAI Conference on Artificial Intelligence, 2019, 33, 2620-2627.	4.9	35
11	Domain Randomization and Pyramid Consistency: Simulation-to-Real Generalization Without Accessing Target Domain Data. , 2019, , .		177
12	FBNet: Hardware-Aware Efficient ConvNet Design via Differentiable Neural Architecture Search. , 2019, , .		674
13	SqueezeNext: Hardware-Aware Neural Network Design. , 2018, , .		179
14	Shift: A Zero FLOP, Zero Parameter Alternative to Spatial Convolutions. , 2018, , .		192
15	SqueezeSeg: Convolutional Neural Nets with Recurrent CRF for Real-Time Road-Object Segmentation from 3D LiDAR Point Cloud. , 2018, , .		491
16	EmotionGAN. , 2018, , .		51
17	Co-design of deep neural nets and neural net accelerators for embedded vision applications. , 2018, , .		6
18	A LiDAR Point Cloud Generator. , 2018, , .		119

#	Article	IF	Citations
19	Affective Image Content Analysis: A Comprehensive Survey. , 2018, , .		49
20	Small neural nets are beautiful. , 2017, , .		22
21	A Predictive Model for Solving Small Linear Algebra Problems in GPU Registers. , 2012, , .		37
22	Automatic generation of application-specific accelerators for FPGAs from python loop nests. , 2012, , .		5
23	Accelerating Valueâ€atâ€Risk estimation on highly parallel architectures. Concurrency Computation Practice and Experience, 2012, 24, 895-907.	2.2	4
24	Communication-Avoiding QR Decomposition for GPUs. , 2011, , .		61
25	Practical parallel imaging compressed sensing MRI: Summary of two years of experience in accelerating body MRI of pediatric patients. , 2011, 2011, 1039-1043.		130
26	A design pattern language for engineering (parallel) software. , 2010, , .		50
27	A view of the parallel computing landscape. Communications of the ACM, 2009, 52, 56-67.	4.5	412
28	Scalable HMM based inference engine in large vocabulary continuous speech recognition. , 2009, , .		8
29	A Decomposition-based Constraint Optimization Approach for Statically Scheduling Task Graphs with Communication Delays to Multiprocessors. , 2007, , .		16
30	Linear programming for sizing, V/sub th/ and V/sub dd/ assignment. , 2005, , .		8
31	Impact of spatial intrachip gate length variability on the performance of high-speed digital circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2002, 21, 544-553.	2.7	128
32	A general probabilistic framework for worst case timing analysis. , 2002, , .		89
33	Functional vector generation for HDL models using linear programming and Boolean satisfiability. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2001, 20, 994-1002.	2.7	32
34	OCCOM-efficient computation of observability-based code coverage metrics for functional verification. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2001, 20, 1003-1015.	2.7	52
35	Limitations and challenges of computer-aided design technology for CMOS VLSI. Proceedings of the IEEE, 2001, 89, 341-365.	21.3	60
36	Why is Combinational ATPG Efficiently Solvable for Practical VLSI Circuits?. Journal of Electronic Testing: Theory and Applications (JETTA), 2001, 17, 509-527.	1.2	2

#	Article	IF	Citations
37	Code density optimization for embedded DSP processors using data compression techniques. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1998, 17, 601-608.	2.7	27
38	Why is ATPG easy?. , 0, , .		14
39	Bus encoding to prevent crosstalk delay. , 0, , .		127