Lutong Wang

List of Publications by Year
in descending order

19	336	1684188 5	1720034 7
papers	citations	h-index	g-index

19	19	19	159
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	TritonRoute-WXL: The Open-Source Router With Integrated DRC Engine. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1076-1089.	2.7	7
2	TritonRoute: The Open-Source Detailed Router. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 547-559.	2.7	16
3	The Tao of PAO: Anatomy of a Pin Access Oracle for Detailed Routing. , 2020, , .		9
4	On the superiority of modularity-based clustering for determining placement-relevant clusters. The Integration VLSI Journal, 2020, 74, 32-44.	2.1	7
5	RePlAce: Advancing Solution Quality and Routability Validation in Global Placement. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1717-1730.	2.7	82
6	Enhanced Optimal Multi-Row Detailed Placement for Neighbor Diffusion Effect Mitigation in Sub-10 nm VLSI. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1703-1716.	2.7	12
7	Toward an Open-Source Digital Flow. , 2019, , .		81
8	Detailed Placement for IR Drop Mitigation by Power Staple Insertion in Sub-10nm VLSI. , 2019, , .		12
9	Finding placement-relevant clusters with fast modularity-based clustering. , 2019, , .		6
10	Diffusion break-aware leakage power optimization and detailed placement in sub-10nm VLSI. , 2019, , .		1
11	2019 CAD Contest: LEF/DEF Based Global Routing. , 2019, , .		30
12	Wot the L. , 2018, , .		1
13	TritonRoute. , 2018, , .		31
14	Performance- and energy-aware optimization of BEOL interconnect stack geometry in advanced technology nodes. , 2017, , .		1
15	Vertical M1 Routing-Aware Detailed Placement for Congestion and Wirelength Reduction in Sub-10nm Nodes. , 2017, , .		11
16	MILP-Based Optimization of 2-D Block Masks for Timing-Aware Dummy Segment Removal in Self-Aligned Multiple Patterning Layouts. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1075-1088.	2.7	1
17	Optimal multi-row detailed placement for yield and model-hardware correlation improvements in sub-10nm VLSI. , 2017, , .		10
18	Improved flop tray-based design implementation for power reduction. , 2016, , .		13

#	Article	IF	Citations
19	ILP-based co-optimization of cut mask layout, dummy fill, and timing for sub-14nm BEOL technology. Proceedings of SPIE, 2015, , .	0.8	5