In-Cheol Park

List of Publications by Year
in descending order

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153	1,718	279798	395702
papers	citations	23 h-index	33 g-index

153	153	153	1142
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Multi-Mode QC-LDPC Decoding Architecture With Novel Memory Access Scheduling for 5G New-Radio Standard. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 2035-2048.	5.4	0
2	High-Speed Counter with Novel LFSR State Extension. IEEE Transactions on Computers, 2022, , 1-8.	3.4	3
3	Constant-Time Synchronous Binary Counter With Minimal Clock Period. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 2645-2649.	3.0	5
4	Real-Time SSDLite Object Detection on FPGA. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1192-1205.	3.1	20
5	Interleaved Local Sorting for Successive Cancellation List Decoding of Polar Codes. IEEE Access, 2021, 9, 128623-128632.	4.2	1
6	Bitwise Early Termination of Multiuser Detection for IDMA Systems. IEEE Communications Letters, 2021, 25, 2998-3002.	4.1	4
7	Hybrid Convolution Architecture for Energy-Efficient Deep Neural Network Processing. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 2017-2029.	5.4	4
8	A Low-Latency Multi-Touch Detector Based on Concurrent Processing of Redesigned Overlap Split and Connected Component Analysis. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 166-176.	5.4	8
9	Retrain-Less Weight Quantization for Multiplier-Less Convolutional Neural Networks. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 972-982.	5.4	13
10	A 120-mW 0.16-ms-Latency Connectivity-Scalable Multiuser Detector for Interleave Division Multiple Access. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 470-474.	3.0	3
11	Ultra-Low-Latency LDPC Decoding Architecture using Reweighted Offset Min-Sum Algorithm. , 2020, , .		4
12	Improved Parallel-IDMA Architecture with Low-Complexity Elementary Signal Estimators. , 2020, , .		1
13	Low-Complexity Address Generation for Multiuser Detectors in IDMA Systems. Electronics (Switzerland), 2020, 9, 2069.	3.1	3
14	Large-Small Sorting for Successive Cancellation List Decoding of Polar Codes. IEEE Access, 2020, 8, 96955-96962.	4.2	4
15	Energy-Efficient Symmetric BC-BCH Decoder Architecture for Mobile Storages. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 4462-4475.	5.4	4
16	Parallel IDMA Architecture Based on Interleaving with Replicated Subpatterns. , 2019, , .		7
17	Fast Low-Complexity Triple-Error-Correcting BCH Decoding Architecture. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 764-768.	3.0	7
18	A 2.4pJ/bit, 6.37Gb/s SPC-enhanced BC-BCH decoder in 65nm CMOS for NAND flash storage systems. , 2018, , .		3

#	Article	IF	Citations
19	Efficient Implementation of Multiple Interleavers in IDMA for 5G. , 2018, , .		6
20	Interference Cancellation Architecture for Pipelined Parallel MIMO Detectors. , 2018, , .		1
21	A Fast Successive Cancellation List Decoder for Polar Codes With an Early Stopping Criterion. IEEE Transactions on Signal Processing, 2018, 66, 4971-4979.	5.3	23
22	A Memory-Efficient IDMA Architecture Based on On-the-Fly Despreading. IEEE Journal of Solid-State Circuits, 2018, 53, 3327-3337.	5.4	10
23	Energy-Efficient Convolution Architecture Based on Rescheduled Dataflow. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 4196-4207.	5.4	45
24	DSIP: A Scalable Inference Accelerator for Convolutional Neural Networks. IEEE Journal of Solid-State Circuits, 2018, 53, 605-618.	5.4	48
25	High-Performance Low-Area Video Up-Scaling Architecture for 4-K UHD Video. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 437-441.	3.0	17
26	Multi-Bit Flipping Decoding of LDPC Codes for NAND Storage Systems. IEEE Communications Letters, 2017, 21, 979-982.	4.1	19
27	Improved Sorting Architecture for ${K}$ -Best MIMO Detection. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1042-1046.	3.0	12
28	Low-Power LDPC-CC Decoding Architecture Based on the Integration of Memory Banks. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1057-1061.	3.0	4
29	Improved Successive-Cancellation Decoding of Polar Codes Based on Recursive Syndrome Decomposition. IEEE Communications Letters, 2017, 21, 2344-2347.	4.1	3
30	Improved Hard-Reliability Based Majority-Logic Decoding for Non-Binary LDPC Codes. IEEE Communications Letters, 2017, 21, 230-233.	4.1	12
31	An energy-optimized (37840, 34320) symmetric BC-BCH decoder for healthy mobile storages. , 2017, , .		4
32	Low-Latency Low-Cost Architecture for Square and Cube Roots. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2017, E100.A, 1951-1955.	0.3	1
33	Low-complexity symbol detection for massive MIMO uplink based on Jacobi method. , 2016, , .		25
34	Efficient Pruning for Successive-Cancellation Decoding of Polar Codes. IEEE Communications Letters, 2016, 20, 2362-2365.	4.1	7
35	Area-Efficient Approach for Generating Quantized Gaussian Noise. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 1005-1013.	5.4	5
36	Efficient Sorting Architecture for Successive-Cancellation-List Decoding of Polar Codes. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 673-677.	3.0	32

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37	Low-Power Parallel Chien Search Architecture Using a Two-Step Approach. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 269-273.	3.0	7
38	Energy-Efficient Floating-Point MFCC Extraction Architecture for Speech Recognition Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 754-758.	3.1	39
39	Energy-Scalable 4KB LDPC Decoding Architecture for NAND-Flash-Based Storage Systems. IEICE Transactions on Electronics, 2016, E99.C, 293-301.	0.6	7
40	Reverse Rate Matching for Low-Power LTE-Advanced Turbo Decoders. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 2920-2928.	5.4	7
41	Low-Complexity Tree Architecture for Finding the First Two Minima. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 61-64.	3.0	29
42	Partially Parallel Encoder Architecture for Long Polar Codes. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 306-310.	3.0	28
43	Efficient Parallel Architecture for Linear Feedback Shift Registers. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 1068-1072.	3.0	26
44	Areaâ€efficient method to approximate two minima for LDPC decoders. Electronics Letters, 2014, 50, 1701-1702.	1.0	1
45	A search-less DEC BCH decoder for low-complexity fault-tolerant systems. , 2014, , .		5
46	Singleâ€step glitchâ€free NANDâ€based digitally controlled delay lines using dual loops. Electronics Letters, 2014, 50, 930-932.	1.0	4
47	7.3 Gb/s universal BCH encoder and decoder for SSD controllers. , 2014, , .		13
48	High-Throughput and Low-Complexity BCH Decoding Architecture for Solid-State Drives. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1183-1187.	3.1	23
49	Tail-Overlapped SISO Decoding for High-Throughput LTE-Advanced Turbo Decoders. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 2711-2720.	5.4	7
50	Low-Complexity Low-Latency Architecture for Matching of Data Encoded With Hard Systematic Error-Correcting Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1648-1652.	3.1	6
51	Efficient Tree-Traversal Strategy for Soft-Output MIMO Detection Based on Candidate-Set Reorganization. IEEE Communications Letters, 2013, 17, 1758-1761.	4.1	2
52	Low-Complexity Parallel QPP Interleaver Based on Permutation Patterns. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 162-166.	3.0	6
53	Area-Efficient Multimode Encoding Architecture for Long BCH Codes. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 872-876.	3.0	23
54	A 2.74-pJ/bit, 17.7-Gb/s Iterative Concatenated-BCH Decoder in 65-nm CMOS for NAND Flash Memory. IEEE Journal of Solid-State Circuits, 2013, 48, 2531-2540.	5.4	21

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55	A 3Gb/s 2.08mm² 100b error-correcting BCH decoder in 0.13µm CMOS process. , 2013, , .		1
56	Adaptive Metric Calculation for Improving Detection Capability of MIMO Detectors. , 2013, , .		0
57	Memory-Optimized Hybrid Decoding Method for Multi-Rate Turbo Codes. , 2013, , .		1
58	Area-Efficient QC-LDPC Decoder Architecture Based on Stride Scheduling and Memory Bank Division. IEICE Transactions on Communications, 2013, E96.B, 1772-1779.	0.7	2
59	SNR-Adaptive Input Quantization for Turbo Decoding. , 2012, , .		0
60	Low-latency area-efficient decoding architecture for shortened reed-solomon codes. , 2012, , .		6
61	Small-area parallel syndrome calculation for strong BCH decoding. , 2012, , .		9
62	Low-Complexity Tone Reservation for PAPR Reduction in OFDM Communication Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1919-1923.	3.1	10
63	Immediate Exchange of Extrinsic Information for High-Throughput Turbo Decoding. IEEE Communications Letters, 2012, 16, 2048-2051.	4.1	0
64	6.4Gb/s multi-threaded BCH encoder and decoder for multi-channel SSD controllers. , 2012, , .		45
65	Low-Complexity Parallel Chien Search Structure Using Two-Dimensional Optimization. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 522-526.	3.0	25
66	Statistical modeling of capacitor mismatch effects for successive approximation register ADCs. , 2011, , .		1
67	Division-less high-radix interleaved modular multiplication using a scaled modulus. , 2011, , .		0
68	QC-LDPC Decoding Architecture based on Stride Scheduling. , 2011, , .		1
69	Efficient Pruning for Infinity-Norm Sphere Decoding Based on Schnorr-Euchner Enumeration. IEICE Transactions on Communications, 2011, E94-B, 2677-2680.	0.7	1
70	Multiplier-less and Table-less Linear Approximation for Square-Related Functions. IEICE Transactions on Information and Systems, 2010, E93-D, 2979-2988.	0.7	2
71	Dual-rail decoding of low-density parity-check codes. , 2010, , .		0
72	Low-complex BPSK demodulation using absolute comparison. , 2010, , .		1

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73	Spur-Free MASH Delta-Sigma Modulation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 2426-2437.	5.4	47
74	High-Throughput and Area-Efficient MIMO Symbol Detection Based on Modified Dijkstra's Search. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 1756-1766.	5.4	28
75	Small-Area and Low-Energy K-Best MIMO Detector Using Relaxed Tree Expansion and Early Forwarding. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 2753-2761.	5.4	38
76	Capacitor array structure and switching control scheme to reduce capacitor mismatch effects for SAR analog-to-digital converters. , 2010, , .		6
77	Design of a Scalable and Programmable Sound Synthesizer. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 875-886.	3.1	1
78	Optimization of Arithmetic Coding for JPEG2000. IEEE Transactions on Circuits and Systems for Video Technology, 2010, 20, 446-451.	8.3	14
79	A scalable and programmable sound synthesizer. , 2009, , .		0
80	A unified parallel radix-4 turbo decoder for mobile WiMAX and 3GPP-LTE. , 2009, , .		51
81	Pipelined Discrete Wavelet Transform Architecture Scanning Dual Lines. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 916-920.	3.0	15
82	Novel pipelined DWT architecture for dual-line scan. , 2009, , .		5
83	Bit-Level Extrinsic Information Exchange Method for Double-Binary Turbo Codes. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 81-85.	3.0	30
84	Multiplier-less and table-less linear approximation for square and square-root. , 2009, , .		8
85	Low-Power and High-Accurate Synchronization for IEEE 802.16d Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 1620-1630.	3.1	12
86	FIR Filter Synthesis Considering Multiple Adder Graphs for a Coefficient. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 958-962.	2.7	17
87	Implementation of efficient architecture of two-dimensional discrete wavelet transform. , 2008, , .		0
88	Prediction-based real-time CABAC decoder for high definition H.264/AVC. , 2008, , .		6
89	Double-Binary Circular Turbo Decoding Based on Border Metric Encoding. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 79-83.	3.0	32
90	A 50Mbps double-binary turbo decoder for WiMAX based on bit-level extrinsic information exchange. , 2008, , .		8

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91	Design of a scalable sound synthesizer. , 2008, , .		0
92	Time-Domain Joint Estimation of Fine Symbol Timing Offset and Integer Carrier Frequency Offset. IEEE Vehicular Technology Conference, 2008, , .	0.4	3
93	Area and power efficient design of coarse time synchronizer and frequency offset estimator for fixed WiMAX systems. , 2008, , .		0
94	High Speed Sphere Decoding Based on Vertically Incremental Computation. , 2007, , .		6
95	SIMD Processor-Based Turbo Decoder Supporting Multiple Third-Generation Wireless Standards. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 801-810.	3.1	30
96	Fast and Area-Efficient Sphere Decoding Using Look-Ahead Search. IEEE Vehicular Technology Conference, 2007, , .	0.4	1
97	Balanced Binary-Tree Decomposition for Area-Efficient Pipelined FFT Processing. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2007, 54, 889-900.	0.1	67
98	Pipelined Cartesian-to-Polar Coordinate Conversion Based on SRT Division. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 680-684.	2.2	9
99	Two-Step Aprroach for Coarse Time Synchronization and Frequency Offset Estimation for IEEE 802.16D Systems. Signal Processing Systems Design and Implementation (siPS), IEEE Workshop on, 2007, , .	0.0	5
100	Low-power log-MAP decoding based on reduced metric memory access. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2006, 53, 1244-1253.	0.1	14
101	Loosely coupled memory-based decoding architecture for low density parity check codes. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2006, 53, 1045-1056.	0.1	44
102	A third-order /spl Sigma//spl Delta/ modulator in 0.18-/spl mu/m CMOS with calibrated mixed-mode integrators. IEEE Journal of Solid-State Circuits, 2005, 40, 918-925.	5.4	24
103	SAT-based unbounded symbolic model checking. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2005, 24, 129-140.	2.7	15
104	A low-power variable length decoder for MPEG-2 based on successive decoding of short codewords. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2003, 39, 73-82.	2.2	14
105	A single-chip programmable platform based on a multithreaded processor and configurable logic clusters. IEEE Journal of Solid-State Circuits, 2003, 38, 1703-1711.	5.4	5
106	Processor-based turbo interleaver for multiple third-generation wireless standards. IEEE Communications Letters, 2003, 7, 210-212.	4.1	18
107	High performance memory mode control for HDTV decoders. IEEE Transactions on Consumer Electronics, 2003, 49, 1348-1353.	3.6	15
108	Low-power hybrid structure of digital matched filters for direct sequence spread spectrum systems. , 2003, , .		1

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109	Digital filter synthesis based on an algorithm to generate all minimal signed digit representations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2002, 21, 1525-1529.	2.7	71
110	FIR filter synthesis algorithms for minimizing the delay and the number of adders. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2001, 48, 770-777.	2.2	74
111	A fixed-point MPEG audio processor operating at low frequency. IEEE Transactions on Consumer Electronics, 2001, 47, 779-786.	3.6	2
112	High-performance and low-power memory-interface architecture for video processing applications. IEEE Transactions on Circuits and Systems for Video Technology, 2001, 11, 1160-1170.	8.3	51
113	Pyramid texture compression and decompression using interpolative vector quantization. , 2000, , .		3
114	MetaCore: an application-specific programmable DSP development system. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2000, 8, 173-183.	3.1	17
115	Synthesis of application specific instructions for embedded DSP software. IEEE Transactions on Computers, 1999, 48, 603-614.	3.4	52
116	Node sampling technique to speed up probability-based power estimation methods. , 1999, , .		0
117	Digital signal processor with efficient RGB interpolation and histogram accumulation. IEEE Transactions on Consumer Electronics, 1998, 44, 1389-1395.	3.6	18
118	Design Verification of Complex Microprocessors. Journal of Circuits, Systems and Computers, 1997, 07, 301-318.	1.5	2
119	MetaCore: an application specific DSP development system. , 0, , .		0
120	Low-power hybrid structure of digital matched filters for direct sequence spread spectrum systems. , 0, , .		1
121	A low-power variable length decoder based on successive decoding of shoft codewords. , 0, , .		0
122	Design verification of complex microprocessors. , 0, , .		1
123	Single cycle access cache for the misaligned data and instruction prefetch. , 0, , .		0
124	A C-based RTL Design Verification Methodology For Complex Microprocessor. , 0, , .		2
125	Verification methodology of compatible microprocessors. , 0, , .		5
126	Multiple behavior module synthesis based on selective groupings. , 0, , .		1

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127	Virtual chip: making functional models work on real target systems. , 0, , .		1
128	Exploiting intellectual properties in ASIP designs for embedded DSP software. , 0, , .		3
129	A multi-threading MPEG processor with variable issue modes. , 0, , .		1
130	A single-chip MP@HL HDTV decoder with integrated audio decoding and display processing units. , 0, , .		0
131	A hardware accelerator for the specular intensity of Phong illumination model in 3-dimensional graphics. , 0, , .		2
132	FIR filter synthesis algorithms for minimizing the delay and the number of adders. , 0, , .		2
133	Multi-thread VLIW processor architecture for HDTV decoding. , 0, , .		3
134	iSAVE: a behavioral emulator for in-system algorithm verification. , 0, , .		0
135	Multiplier-less IIR filter synthesis algorithms to trade-off the delay and the number of adders. , 0, , .		4
136	A single-chip programmable platform based on a multithreaded processor and configurable logic clusters. , 0, , .		0
137	Low cost floating-point unit design for audio applications. , 0, , .		1
138	A fixed-point MPEG audio processor for low frequency-operation. , 0, , .		0
139	Area-efficient digital baseband module for Bluetooth wireless communications. , 0, , .		1
140	A single-chip programmable platform based on a multithreaded processor and configurable logic clusters. , 0, , .		0
141	History-based memory mode prediction for improving memory performance. , 0, , .		4
142	A programmable turbo decoder for multiple 3G wireless standards. , 0, , .		15
143	A hybrid delta-sigma modulator with adaptive calibration. , 0, , .		7
144	A 5-GHz self-calibrated I/Q clock generator using a quadrature LC-VCO. , 0, , .		2

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145	Memory-based low density parity check code decoder architecture using loosely coupled two data-flows. , 0, , .		0
146	Quadrature direct digital frequency synthesis using fine-grain angle rotation. , 0, , .		0
147	A fast Reed-Solomon Product-Code decoder without redundant computations. , 0, , .		4
148	Low-Power Log-Map Turbo Decoding Based on Reduced Metric Memory Access. , 0, , .		6
149	Scheduling Algorithm for Partially Parallel Architecture of LDPC Decoder by Matrix Permutation. , 0, , .		19
150	High speed decoding of context-based adaptive binary arithmetic codes using most probable symbol prediction. , 0, , .		15
151	Low-Power Hybrid Turbo Decoding Based on Reverse Calculation. , 0, , .		11
152	Digital filter synthesis based on minimal signed digit representation. , 0, , .		1
153	Synthesis of application specific instructions for embedded DSP software. , 0, , .		0