JosuÃ© Feliu

List of Publications by Year
in descending order

23	143	1937685 4	1474206 9
papers	citations	h-index	g-index

23	23	23	96
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Cache-Hierarchy Contention-Aware Scheduling in CMPs. IEEE Transactions on Parallel and Distributed Systems, 2014, 25, 581-590.	5.6	21
2	Perf&Fair: A Progress-Aware Scheduler to Enhance Performance and Fairness in SMT Multicores. IEEE Transactions on Computers, 2017, 66, 905-911.	3.4	20
3	Understanding Cache Hierarchy Contention in CMPs to Improve Job Scheduling. , 2012, , .		16
4	Bandwidth-Aware On-Line Scheduling in SMT Multicores. IEEE Transactions on Computers, 2016, 65, 422-434.	3.4	14
5	Addressing Fairness in SMT Multicores with a Progress-Aware Scheduler. , 2015, , .		12
6	Precise Runahead Execution. , 2020, , .		12
7	Symbiotic job scheduling on the IBM POWER8. , 2016, , .		11
8	The Forward Slice Core Microarchitecture. , 2020, , .		8
9	Bandwidth-Aware Dynamic Prefetch Configuration for IBM POWER8. IEEE Transactions on Parallel and Distributed Systems, 2020, 31, 1970-1982.	5.6	6
10	Improving IBM POWER8 Performance Through Symbiotic Job Scheduling. IEEE Transactions on Parallel and Distributed Systems, 2017, 28, 2838-2851.	5.6	4
11	Thread Isolation to Improve Symbiotic Scheduling on SMT Multicore Processors. IEEE Transactions on Parallel and Distributed Systems, 2020, 31, 359-373.	5.6	4
12	Effect of Hyper-Threading in Latency-Critical Multithreaded Cloud Applications and Utilization Analysis of the Major System Resources. Future Generation Computer Systems, 2022, 131, 194-208.	7.5	4
13	Precise Runahead Execution. IEEE Computer Architecture Letters, 2019, 18, 71-74.	1.5	3
14	An empirical model for predicting cross-core performance interference on multicore processors. , 2013, , .		2
15	Addressing bandwidth contention in SMT multicores through scheduling. , 2014, , .		2
16	Using Huge Pages and Performance Counters to Determine the LLC Architecture. Procedia Computer Science, 2013, 18, 2557-2560.	2.0	1
17	Designing lab sessions focusing on real processors for computer architecture courses: A practical perspective. Journal of Parallel and Distributed Computing, 2018, 118, 128-139.	4.1	1
18	ITSLF: Inter-Thread Store-to-Load Forwardingin Simultaneous Multithreading. , 2021, , .		1

#	Article	IF	Citations
19	DeepP: Deep Learning Multi-Program Prefetch Configuration for the IBM POWER 8. IEEE Transactions on Computers, 2022, 71, 2646-2658.	3.4	1
20	A Workload Generator for Evaluating SMT Real-Time Systems. , 2018, , .		0
21	VMT: Virtualized Multi-Threading for Accelerating Graph Workloads on Commodity Processors. IEEE Transactions on Computers, 2022, 71, 1386-1398.	3.4	0
22	The Forward Slice Core: A High-Performance, Yet Low-Complexity Microarchitecture. Transactions on Architecture and Code Optimization, 2022, 19, 1-25.	2.0	0
23	A Neural Network to Estimate Isolated Performance from Multi-Program Execution. , 2022, , .		0