Ke-Meng Yang

List of Publications by Year
in descending order

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14 papers	106 citations	1478505 6 h-index	1372567 10 g-index
14 all docs	14 docs citations	14 times ranked	84 citing authors

#	Article	IF	Citations
1	Effective Doping Concentration Theory: A New Physical Insight for the Double-RESURF Lateral Power Devices on SOI Substrate. IEEE Transactions on Electron Devices, 2018, 65, 648-654.	3.0	23
2	A Novel Variation of Lateral Doping Technique in SOI LDMOS With Circular Layout. IEEE Transactions on Electron Devices, 2018, 65, 1447-1452.	3.0	21
3	Analytical Model for the SOI Lateral Power Device With Step Width Technique and High-${k}$ Dielectric. IEEE Transactions on Electron Devices, 2019, 66, 3055-3059.	3.0	9
4	A Novel 3-D Analytical Method for Curvature Effect-Induced Electric Field Crowding in SOI Lateral Power Device. IEEE Transactions on Electron Devices, 2016, 63, 4359-4365.	3.0	8
5	Numerical and analytical investigations for the SOI LDMOS with alternated high-k dielectric and step doped silicon pillars*. Chinese Physics B, 2020, 29, 038503.	1.4	8
6	A New Physical Insight for the 3-D-Layout-Induced Cylindrical Breakdown in Lateral Power Devices on SOI Substrate. IEEE Transactions on Electron Devices, 2018, 65, 1843-1848.	3.0	6
7	Modeling of the Variation of Lateral Doping (VLD) Lateral Power Devices via 1-D Analysis Using Effective Concentration Profile Concept. IEEE Journal of the Electron Devices Society, 2019, 7, 990-996.	2.1	6
8	A New Low Turn-Off Loss SOI Lateral Insulated Gate Bipolar Transistor With Buried Variation of Lateral Doping Layer. IEEE Journal of the Electron Devices Society, 2019, 7, 62-69.	2.1	6
9	A new physical insight of RESURF effects based on gradual charge appointment concept for bulk silicon lateral power devices. Superlattices and Microstructures, 2016, 92, 111-123.	3.1	5
10	An Analytical Breakdown Model for the SOI LDMOS With Arbitrary Drift Doping Profile by Using Effective Substrate Voltage Method. IEEE Journal of the Electron Devices Society, 2020, 8, 49-56.	2.1	5
11	The New Structure and Analytical Model of a High-Voltage Interconnection Shielding Structure With High-k Dielectric Pillar. IEEE Transactions on Electron Devices, 2020, 67, 1745-1750.	3.0	5
12	Area-Efficient and Snapback-Free SOI LIGBT With L-Shaped Extraction Path. IEEE Journal of the Electron Devices Society, 2019, 7, 728-734.	2.1	3
13	Snapback-Free Reverse-Conducting SOI LIGBT with an Integrated Self-Biased MOSFET. Nanoscale Research Letters, 2022, 17, 46.	5.7	1
14	The Application of the High-k Dielectrics in Lateral Double-Diffused Metal Oxide Semiconductor. , 2021, , .		0