Huazhong Yang

List of Publications by Year
in descending order

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328	5,394	218677	223800
papers	citations	26 h-index	46 g-index

329	329	329	4025
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Senputing: An Ultra-Low-Power Always-On Vision Perception Chip Featuring the Deep Fusion of Sensing and Computing. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 232-243.	5.4	28
2	INCAME: Interruptible CNN Accelerator for Multirobot Exploration. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 964-978.	2.7	2
3	Accuracy Optimization With the Framework of Non-Volatile Computing-In-Memory Systems. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 518-529.	5.4	4
4	A 65-nm Energy-Efficient Interframe Data Reuse Neural Network Accelerator for Video Applications. IEEE Journal of Solid-State Circuits, 2022, 57, 2574-2585.	5.4	2
5	PACA: A Pattern Pruning Algorithm and Channel-Fused High PE Utilization Accelerator for CNNs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 5043-5056.	2.7	4
6	Computing-in-memory with thin-filmtransistors: challenges and opportunities. Flexible and Printed Electronics, 2022, 7, 024001.	2.7	5
7	A Bidirectional Integrated Equalizer Based on the Sepicâ€“Zeta Converter for Hybrid Energy Storage System. IEEE Transactions on Power Electronics, 2022, 37, 12659-12668.	7.9	16
8	STICKER-IM: A 65 nm Computing-in-Memory NN Processor Using Block-Wise Sparsity Optimization and Inter/Intra-Macro Data Reuse. IEEE Journal of Solid-State Circuits, 2022, 57, 2560-2573.	5.4	17
9	Toward Low-Bit Neural Network Training Accelerator by Dynamic Group Accumulation. , 2022, , .		0
10	Bit-Aware Fault-Tolerant Hybrid Retraining and Remapping Schemes for RRAM-Based Computing-in-Memory Systems. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 3144-3148.	3.0	2
11	Gibbon: Efficient Co-Exploration of NN Model and Processing-In-Memory Architecture. , 2022, , .		7
12	Explore-Bench: Data Sets, Metrics and Evaluations for Frontier-based and Deep-reinforcement-learning-based Autonomous Exploration. , 2022, , .		11
13	MACSen: A Processing-In-Sensor Architecture Integrating MAC Operations Into Image Sensor for Ultra-Low-Power BNN-Based Intelligent Visual Perception. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 627-631.	3.0	13
14	Temporal Matrices Mapping-Based Calibration Method for Event-Driven Structured Light Systems. IEEE Sensors Journal, 2021, 21, 1799-1808.	4.7	6
15	Mixup Asymmetric Tri-Training for Heartbeat Classification Under Domain Shift. IEEE Signal Processing Letters, 2021, 28, 718-722.	3.6	8
16	A Non-Volatile Computing-In-Memory Framework With Margin Enhancement Based CSA and Offset Reduction Based ADC. , 2021, , .		1
17	Epipolar Geometry Guided Highly Robust Structured Light 3D Imaging. IEEE Signal Processing Letters, 2021, 28, 887-891.	3.6	6
18	Bridge Dynamic Displacement Monitoring Using Adaptive Data Fusion of GNSS and Accelerometer Measurements. IEEE Sensors Journal, 2021, 21, 24359-24370.	4.7	7

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19	CLECG: A Novel Contrastive Learning Framework for Electrocardiogram Arrhythmia Classification. IEEE Signal Processing Letters, 2021, 28, 1993-1997.	3.6	10
20	Enabling Lower-Power Charge-Domain Nonvolatile In-Memory Computing With Ferroelectric FETs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 2262-2266.	3.0	18
21	Dynamic Ternary Content-Addressable Memory Is Indeed Promising: Design and Benchmarking Using Nanoelectromechanical Relays. , 2021, , .		4
22	Almost-Nonvolatile IGZO-TFT-Based Near-Sensor In-Memory Computing. , 2021, , .		8
23	STICKER-T: An Energy-Efficient Neural Network Processor Using Block-Circulant Algorithm and Unified Frequency-Domain Acceleration. IEEE Journal of Solid-State Circuits, 2021, 56, 1936-1948.	5.4	6
24	Capacitive Content-Addressable Memory. , 2021, , .		3
25	FTT-NAS: Discovering Fault-tolerant Convolutional Neural Architecture. ACM Transactions on Design Automation of Electronic Systems, 2021, 26, 1-24.	2.6	9
26	NS-FDN: Near-Sensor Processing Architecture of Feature-Configurable Distributed Network for Beyond-Real-Time Always-on Keyword Spotting. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 1892-1905.	5.4	19
27	Block-Circulant Neural Network Accelerator Featuring Fine-Grained Frequency-Domain Quantization and Reconfigurable FFT Modules. , 2021, , .		2
28	Low-Cost Multi-Agent Navigation via Reinforcement Learning With Multi-Fidelity Simulator. IEEE Access, 2021, 9, 84773-84782.	4.2	1
29	In Situ Blind Calibration of Sensor Networks for Infrastructure Monitoring. IEEE Sensors Journal, 2021, , 1-1.	4.7	1
30	Efficient Computing Platform Design for Autonomous Driving Systems. , 2021, , .		1
31	DyTAN: Dynamic Ternary Content Addressable Memory Using Nanoelectromechanical Relays. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1981-1993.	3.1	2
32	A community effort to assess and improve computerized interpretation of 12-lead resting electrocardiogram. Medical and Biological Engineering and Computing, 2021, 60, 33.	2.8	1
33	Reducing SRAM Reading Power With Column Data Segment and Weights Correlation Enhancement for CNN Processing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2237-2250.	2.7	1
34	Low-Power and Scalable Retention-Enhanced IGZO TFT eDRAM-Based Charge-Domain Computing. , 2021, , .		12
35	Low Bit-Width Convolutional Neural Network on RRAM. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 1414-1427.	2.7	37
36	Processing Near Sensor Architecture in Mixed-Signal Domain With CMOS Image Sensor of Convolutional-Kernel-Readout Method. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 389-400.	5.4	28

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37	ASP-SIFT: Using Analog Signal Processing Architecture to Accelerate Keypoint Detection of SIFT Algorithm. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 198-211.	3.1	3
38	Investigation and Modeling of Multi-Node Body Channel Wireless Power Transfer. Sensors, 2020, 20, 156.	3.8	3
39	STICKER: An Energy-Efficient Multi-Sparsity Compatible Accelerator for Convolutional Neural Networks in 65-nm CMOS. IEEE Journal of Solid-State Circuits, 2020, 55, 465-477.	5.4	51
40	CNN-based Monocular Decentralized SLAM on embedded FPGA. , 2020, , .		7
41	Optimization and Evaluation of Energy-Efficient Mixed-Signal MFCC Feature Extraction Architecture. , 2020, , .		5
42	Enabling Efficient and Flexible FPGA Virtualization for Deep Learning in the Cloud. , 2020, , .		13
43	Design of Almost-Nonvolatile Embedded DRAM Using Nanoelectromechanical Relay Devices. , 2020, , .		2
44	CDS-RSRAM: a Reconfigurable SRAM Architecture to Reduce Read Power with Column Data Segmentation. , 2020, , .		1
45	Enabling Secure NVM-Based in-Memory Neural Network Computing by Sparse Fast Gradient Encryption. IEEE Transactions on Computers, 2020, 69, 1596-1610.	3.4	15
46	INCA: INterruptible CNN Accelerator for Multi-tasking in Embedded Robots. , 2020, , .		5
47	Unsupervised Domain Adaptation for ECG Arrhythmia Classification. , 2020, 2020, 304-307.		15
48	Soft Error Mitigation for Deep Convolution Neural Network on FPGA Accelerators. , 2020, , .		11
49	One-Shot Refresh: A Low-Power Low-Congestion Approach for Dynamic Memories. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3402-3406.	3.0	3
50	CNN-based Feature-point Extraction for Real-time Visual SLAM on Embedded FPGA. , 2020, , .		26
51	MSP-MFCC: Energy-Efficient MFCC Feature Extraction Method With Mixed-Signal Processing Architecture for Wearable Speech Recognition Applications. IEEE Access, 2020, 8, 48720-48730.	4.2	37
52	FTT-NAS: Discovering Fault-Tolerant Neural Architecture. , 2020, , .		20
53	Black Box Search Space Profiling for Accelerator-Aware Neural Architecture Search. , 2020, , .		5
54	Long Live TIME: Improving Lifetime and Security for NVM-Based Training-in-Memory Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4707-4720.	2.7	9

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55	The Role and Challenges of Body Channel Communication in Wearable Flexible Electronics. IEEE Transactions on Biomedical Circuits and Systems, 2020, 14, 283-296.	4.0	28
56	GAAS: An Efficient Group Associated Architecture and Scheduler Module for Sparse CNN Accelerators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 5170-5182.	2.7	2
57	NS-CIM: A Current-Mode Computation-in-Memory Architecture Enabling Near-Sensor Processing for Intelligent IoT Vision Nodes. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 2909-2922.	5.4	25
58	An Energy-Efficient Quantized and Regularized Training Framework For Processing-In-Memory Accelerators. , 2020, , .		18
59	A Generic Graph-Based Neural Architecture Encoding Scheme for Predictor-Based NAS. Lecture Notes in Computer Science, 2020, , 189-204.	1.3	29
60	High PE Utilization CNN Accelerator with Channel Fusion Supporting Pattern-Compressed Sparse Neural Networks. , 2020, , .		10
61	FeFET-based low-power bitwise logic-in-memory with direct write-back and data-adaptive dynamic sensing interface. , 2020, , .		14
62	Autofocusing method for high-resolution three-dimensional profilometry. Optics Letters, 2020, 45, 375.	3.3	18
63	High-Quality Single-Model Deep Video Compression with Frame-Conv3D and Multi-frame Differential Modulation. Lecture Notes in Computer Science, 2020, , 239-254.	1.3	6
64	NS-KWS. , 2020, , .		6
65	Multi-channel precision-sparsity-adapted inter-frame differential data codec for video neural network processor. , 2020, , .		2
66	DSA: More Efficient Budgeted Pruning via Differentiable Sparsity Allocation. Lecture Notes in Computer Science, 2020, , 592-607.	1.3	36
67	A 3.77TOPS/W Convolutional Neural Network Processor With Priority-Driven Kernel Optimization. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 277-281.	3.0	21
68	A global and updatable ECG beat classification system based on recurrent neural networks and active learning. Information Sciences, 2019, 501, 523-542.	6.9	79
69	Dynamic Channel Modeling and OFDM System Analysis for Capacitive Coupling Body Channel Communication. IEEE Transactions on Biomedical Circuits and Systems, 2019, 13, 735-745.	4.0	11
70	An Auto Loss Compensation System for Capacitive-Coupled Body Channel Communication. IEEE Transactions on Biomedical Circuits and Systems, 2019, 13, 756-765.	4.0	10
71	On-Chip Instruction Generation for Cross-Layer CNN Accelerator on FPGA. , 2019, , .		4
72	A 3T/Cell Practical Embedded Nonvolatile Memory Supporting Symmetric Read and Write Access Based on Ferroelectric FETs. , 2019, , .		7

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73	HyVE: Hybrid Vertex-Edge Memory Hierarchy for Energy-Efficient Graph Processing. IEEE Transactions on Computers, 2019, 68, 1131-1146.	3.4	6
74	A Configurable Multi-Precision CNN Computing Framework Based on Single Bit RRAM. , 2019, , .		50
75	Design of 2T/Cell and 3T/Cell Nonvolatile Memories with Emerging Ferroelectric FETs. IEEE Design and Test, 2019, 36, 39-45.	1.2	26
76	AERIS. , 2019, , .		5
77	A Sparse-Adaptive CNN Processor with Area/Performance balanced N-Way Set-Associate PE Arrays Assisted by a Collision-Aware Scheduler. , 2019, , .		11
78	A 4-Mbps 41-pJ/bit On-off Keying Transceiver for Body-channel Communication with Enhanced Auto Loss Compensation Technique. , 2019, , .		9
79	Enabling New Computing Paradigms with Emerging Symmetric-Access Memories. , 2019, , .		0
80	Guided, Fusion-Based, Large Depth-of-field 3D Imaging Using a Focal Stack. Sensors, 2019, 19, 4845.	3.8	15
81	Demystifying and Mitigating Code-Dependent Switching Distortions in Current-Steering DACs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 68-81.	5.4	28
82	A 130-nm Ferroelectric Nonvolatile System-on-Chip With Direct Peripheral Restore Architecture for Transient Computing System. IEEE Journal of Solid-State Circuits, 2019, 54, 885-895.	5.4	13
83	A 2.2-GHz Configurable Direct Digital Frequency Synthesizer Based on LUT and Rotation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 1970-1980.	5.4	6
84	Design Methodology for TFT-Based Pseudo-CMOS Logic Array With Multilayer Interconnection Architecture and Optimization Algorithms. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 2043-2057.	2.7	1
85	GraphH: A Processing-in-Memory Architecture for Large-Scale Graph Processing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 640-653.	2.7	75
86	TIME: A Training-in-Memory Architecture for RRAM-Based Deep Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 834-847.	2.7	44
87	Large depth-of-field 3D shape measurement using an electrically tunable lens. Optics Express, 2019, 27, 29697.	3.4	26
88	Mechanical strain and temperature aware design methodology for thin-film transistor based pseudo-CMOS logic array. , 2018, , .		1
89	A Five-Tissue-Layer Human Body Communication Circuit Model Tunable to Individual Characteristics. IEEE Transactions on Biomedical Circuits and Systems, 2018, 12, 303-312.	4.0	22
90	Redundancyâ€bandwidth scalable techniques for signalâ€independent element transition rates in highâ€speed currentâ€steering DACs. International Journal of Circuit Theory and Applications, 2018, 46, 1006-1027.	2.0	5

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91	PAGANI Toolkit: Parallel graphâ€theoretical analysis package for brain network big data. Human Brain Mapping, 2018, 39, 1869-1885.	3.6	12
92	Lowering Area Overheads for FeFET-Based Energy-Efficient Nonvolatile Flip-Flops. IEEE Transactions on Electron Devices, 2018, 65, 2670-2674.	3.0	21
93	A Tissue-Channel Transcutaneous Power Transfer Technique for Implantable Devices. IEEE Transactions on Power Electronics, 2018, 33, 9753-9761.	7.9	34
94	Angel-Eye: A Complete Design Flow for Mapping CNN Onto Embedded FPGA. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 35-47.	2.7	382
95	Hardware Trojan Detection in Third-Party Digital Intellectual Property Cores by Multilevel Feature Analysis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1370-1383.	2.7	42
96	Stuck-at Fault Tolerance in RRAM Computing Systems. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 102-115.	3.6	88
97	Energy-Efficient SRAM Design with Data-Aware Dual-Modes L0T Storage Cell for CNN Processors. , 2018, , .		2
98	An Investigation on Inter-degeneration Effect in Body Channel Based Multi-node Wireless Power Transfer. , 2018, , .		1
99	Long live TIME. , 2018, , .		30
100	Energy-efficient MFCC extraction architecture in mixed-signal domain for automatic speech recognition. , 2018, , .		5
101	Blind Drift Calibration of Sensor Networks Using Multi-Output Gaussian Process. , 2018, , .		1
102	Energy Efficient ApproxSIFT Implementation for Image Mosaic with Approximate Computing Technologies. , 2018, , .		1
103	MINTIN: Maxout-Based and Input-Normalized Transformation Invariant Neural Network. , 2018, , .		2
104	CMOS Image Sensor Data-Readout Method for Convolutional Operations with Processing Near Sensor Architecture. , 2018, , .		6
105	Sticker: A 0.41-62.1 TOPS/W 8Bit Neural Network Processor with Multi-Sparsity Compatible Convolution Arrays and Online Tuning Acceleration for Fully Connected Layers. , 2018, , .		86
106	Scene-Adaptive Image Acquisition for Focus Stacking. , 2018, , .		4
107	Calibrating Process Variation at System Level with In-Situ Low-Precision Transfer Learning for Analog Neural Network Processors. , 2018, , .		0
108	NewGraph: Balanced Large-Scale Graph Processing on FPGAs with Low Preprocessing Overheads. , 2018, , .		0

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109	Approximate On-chip Memory Optimization Method For Deep Residual Networks. , 2018, , .		0
110	An Auto Loss Compensation System for Non-contact Capacitive Coupled Body Channel Communication. , 2018, , .		8
111	HyVE: Hybrid vertex-edge memory hierarchy for energy-efficient graph processing. , 2018, , .		13
112	Design of FPGA-Based Accelerator for Convolutional Neural Network under Heterogeneous Computing Framework with OpenCL. International Journal of Reconfigurable Computing, 2018, 2018, 1-10.	0.2	6
113	RRAM Based Buffer Design for Energy Efficient CNN Accelerator. , 2018, , .		5
114	Hu-Fu: Hardware and Software Collaborative Attack Framework Against Neural Networks. , 2018, , .		29
115	Binary convolutional neural network on RRAM. , 2017, , .		119
116	Computation-oriented fault-tolerance schemes for RRAM computing systems. , 2017, , .		31
117	A Deep Learning Approach for Blind Drift Calibration of Sensor Networks. IEEE Sensors Journal, 2017, 17, 4158-4171.	4.7	59
118	Low-overhead implementation of logic encryption using gate replacement techniques. , 2017, , .		9
119	A Ferroelectric Nonvolatile Processor with 46 $mu $ s System-Level Wake-up Time and 14 $mu $ s Sleep Time for Energy Harvesting Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 596-607.	5.4	35
120	Design Methodology for Thin-Film Transistor Based Pseudo-CMOS Logic Array with Multi-Layer Interconnect Architecture. , 2017, , .		2
121	A Self-Adaptive Capacitive Compensation Technique for Body Channel Communication. IEEE Transactions on Biomedical Circuits and Systems, 2017, 11, 1001-1012.	4.0	21
122	An Investigation on Ground Electrodes of Capacitive Coupling Human Body Communication. IEEE Transactions on Biomedical Circuits and Systems, 2017, 11, 910-919.	4.0	26
123	Noise Margin, Delay, and Power Model for Pseudo-CMOS TFT Logic Circuits. IEEE Transactions on Electron Devices, 2017, 64, 2635-2642.	3.0	5
124	CP-FPGA: Energy-Efficient Nonvolatile FPGA With Offline/Online Checkpointing Optimization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2153-2163.	3.1	5
125	All-Digital Galvanically-Coupled BCC Receiver Resilient to Frequency Misalignment. IEEE Transactions on Biomedical Circuits and Systems, 2017, 11, 714-726.	4.0	8
126	ForeGraph. , 2017, , .		100

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127	A General Framework for Hardware Trojan Detection in Digital Circuits by Statistical Learning Algorithms. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1633-1646.	2.7	23
128	CORAL: Coarse-grained reconfigurable architecture for Convolutional Neural Networks. , 2017, , .		10
129	MNSIM: Simulation Platform for Memristor-based Neuromorphic Computing System. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, , 1-1.	2.7	42
130	AICNN: Implementing Typical CNN Algorithms with Analog-to-Information Conversion Architecture. , 2017, , .		9
131	AIsim: Functional Simulator for Analog-to-Information Perceptual Systems. , 2017, , .		1
132	A 65-nm ReRAM-Enabled Nonvolatile Processor With Time-Space Domain Adaption and Self-Write-Termination Achieving $> 4imes $ Faster Clock Frequency and $> 6imes $ Higher Restore Speed. IEEE Journal of Solid-State Circuits, 2017, 52, 2769-2785.	5.4	8
133	A ReRAM-Based Nonvolatile Flip-Flop With Self-Write-Termination Scheme for Frequent-OFF Fast-Wake-Up Nonvolatile Processors. IEEE Journal of Solid-State Circuits, 2017, 52, 2194-2207.	5.4	41
134	Multistage Latency Adders Architecture Employing Approximate Computing. Journal of Circuits, Systems and Computers, 2017, 26, 1750039.	1.5	3
135	CNN-based pattern recognition on nonvolatile IoT platform for smart ultraviolet monitoring: (Invited) Tj ETQq1 1 0.784314 rgBT /Ove		1
136	DVFS-Based Long-Term Task Scheduling for Dual-Channel Solar-Powered Sensor Nodes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2981-2994.	3.1	6
137	Instruction driven cross-layer CNN accelerator with winograd transformation on FPGA. , 2017, , .		27
138	Using human body as a monopole antenna for energy harvesting from ambient electromagnetic energy. , 2017, , .		2
139	Region ensemble network: Improving convolutional network for hand pose estimation. , 2017, , .		92
140	Streaming sorting network based BWT acceleration on FPGA for lossless compression. , 2017, , .		3
141	Two-stream binocular network: Accurate near field finger detection based on binocular images. , 2017, , .		1
142	A priority-based selective bit dropping strategy to reduce DRAM and SRAM power in image processing. IEICE Electronics Express, 2016, 13, 20160990-20160990.	0.8	2
143	Blind Drift Calibration of Sensor Networks using Sparse Bayesian Learning. IEEE Sensors Journal, 2016, , 1-1.	4.7	22
144	A Real-Time and Energy-Efficient Implementation of Difference-of-Gaussian with Flexible Thin-Film Transistors. , 2016, , .		2

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145	Optimizing convolutional neural network on FPGA under heterogeneous computing framework with OpenCL. , 2016, , .		4
146	A Multi-accuracy-Level Approximate Memory Architecture Based on Data Significance Analysis. , 2016, , .		13
147	A precision-improved processing architecture of physical computing for energy-efficient SIFT feature extraction. , 2016, , .		2
148	Noise Margin Modeling for Zero-$V_{ext {GS}}$ Load TFT Circuits and Yield Estimation. IEEE Transactions on Electron Devices, 2016, 63, 684-690.	3.0	9
149	Going Deeper with Embedded FPGA Platform for Convolutional Neural Network. , 2016, , .		836
150	NXgraph: An efficient graph processing system on a single machine. , 2016, , .		63
151	Angel-Eye: A Complete Design Flow for Mapping CNN onto Customized Hardware. , 2016, , .		52
152	Accurate personal ultraviolet dose estimation with multiple wearable sensors. , 2016, , .		2
153	Host cancelationâ€based spread spectrum watermarking for audio antiâ€piracy over Internet. Security and Communication Networks, 2016, 9, 4691-4702.	1.5	1
154	An ultra-fast and low-power design of analog circuit network for DoG pyramid construction of SIFT algorithm. , 2016, , .		2
155	NVPsim: A simulator for architecture explorations of nonvolatile processors. , 2016, , .		6
156	Modeling Random Telegraph Noise as a Randomness Source and its Application in True Random Number Generation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1435-1448.	2.7	23
157	CP-FPGA: Computation data-aware software/hardware co-design for nonvolatile FPGAs based on checkpointing techniques. , 2016, , .		1
158	Spread spectrum audio watermarking based on perceptual characteristic aware extraction. IET Signal Processing, 2016, 10, 266-273.	1.5	27
159	Solar Power Prediction Assisted Intra-task Scheduling for Nonvolatile Sensor Nodes. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 724-737.	2.7	26
160	Technological Exploration of RRAM Crossbar Array for Matrix-Vector Multiplication. Journal of Computer Science and Technology, 2016, 31, 3-19.	1.5	117
161	Exploring the Precision Limitation for RRAM-Based Analog Approximate Computing. IEEE Design and Test, 2016, 33, 51-58.	1.2	15
162	Storage-Less and Converter-Less Photovoltaic Energy Harvesting With Maximum Power Point Tracking for Internet of Things. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 173-186.	2.7	87

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163	FPGP. , 2016, , .		91
164	Sparsity-Oriented Sparse Solver Design for Circuit Simulation. , 2016, , .		2
165	Drift detection and calibration of sensor networks. , 2015, , .		10
166	Design exploration of inrush current aware controller for nonvolatile processor. , 2015, , .		13
167	Blind drift calibration of sensor networks using signal space projection and Kalman filter. , 2015, , .		7
168	A 6-bit 320-MS/s 2-bit/cycle SAR ADC with tri-level charge redistribution. , 2015, , .		2
169	Simultaneous accelerator parallelization and point-to-point interconnect insertion for bus-based embedded SoCs. Tsinghua Science and Technology, 2015, 20, 644-660.	6.1	1
170	The effects of GND electrodes in capacitive-coupling body channel communication. , 2015, , .		7
171	An FPGA-based real-time simultaneous localization and mapping system. , 2015, , .		9
172	GPU-Accelerated Sparse LU Factorization for Circuit Simulation with Performance Modeling. IEEE Transactions on Parallel and Distributed Systems, 2015, 26, 786-795.	5.6	52
173	Modeling and optimization of low power resonant clock mesh. , 2015, , .		2
174	HS3-DPG: Hierarchical Simulation for 3-D P/G Network. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2307-2311.	3.1	1
175	A 14-bit 1.0-GS/s dynamic element matching DAC with >80 dB SFDR up to the Nyquist. , 2015, , .		21
176	A 5-tissue-layer lumped-element based HBC circuit model compatible to IEEE802.15.6. , 2015, , .		6
177	RRAM-Based Analog Approximate Computing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1905-1917.	2.7	100
178	Approximate Computing in Chrominance Cache for Image/Video Processing. , 2015, , .		11
179	Nonvolatile memory allocation and hierarchy optimization for high-level synthesis. , 2015, , .		3
180	Supply-Noise Interactions Among Submodules Inside a Charge-Pump PLL. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 771-775.	3.1	5

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181	Multistage Function Speculation Adders. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2015, E98.A, 954-965.	0.3	1
182	An Energy Efficient Backup Scheme with Low Inrush Current for Nonvolatile SRAM in Energy Harvesting Sensor Nodes. , 2015, , .		19
183	A Fast Parallel Sparse Solver for SPICE-Based Circuit Simulators. , 2015, , .		5
184	Increasing compression ratio of low complexity compressive sensing video encoder with application-aware configurable mechanism. , 2014, , .		2
185	A novel hybrid storage architecture for nonvolatile FPGA. , 2014, , .		1
186	Library based image processing system with circuit-switched reconfigurable interconnection. , 2014, , .		0
187	Exploration of Electrical and Novel Optical Chip-to-Chip Interconnects. IEEE Design and Test, 2014, 31, 28-35.	1.2	8
188	A single channel, 6-bit 410-ms/s asynchronous SAR ADC based on 3bits/stage. , 2014, , .		1
189	Statistical analysis of random telegraph noise in digital circuits. , 2014, , .		5
190	Intra-task scheduling for storage-less and converter-less solar-powered nonvolatile sensor nodes. , 2014, , .		13
191	A 12-bit 400-MS/s SHA-less pipelined ADC. , 2014, , .		1
192	A blind audio watermarking algorithm by logarithmic quantization index modulation. Multimedia Tools and Applications, 2014, 71, 1157-1177.	3.9	9
193	Design of RF transceivers for wireless sensor networks in hazardous applications. Analog Integrated Circuits and Signal Processing, 2014, 79, 319-329.	1.4	4
194	Efficient region-aware P/G TSV planning for 3D ICs. , 2014, , .		6
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