Meishoku Masahara

List of Publications by Year
in descending order

172	2,086	304743	330143
papers	citations	22 h-index	37 g-index

172	172	172	1336
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Simulation study of short-channel effects of tunnel field-effect transistors. Japanese Journal of Applied Physics, 2018, 57, 04FD04.	1.5	3
2	Structural and electrical characterization of epitaxial Ge thin films on Si(001) formed by sputtering. Japanese Journal of Applied Physics, 2017, 56, 04CB01.	1.5	0
3	On the drain bias dependence of long-channel silicon-on-insulator-based tunnel field-effect transistors. Japanese Journal of Applied Physics, 2017, 56, 04CD04.	1.5	2
4	Tunnel FinFET CMOS inverter with very low short-circuit current for ultralow-power Internet of Things application. Japanese Journal of Applied Physics, 2017, 56, 04CD19.	1.5	15
5	Impact of residual defects caused by extension ion implantation in FinFETs on parasitic resistance and its fluctuation. Solid-State Electronics, 2017, 132, 103-108.	1.4	3
6	Bias temperature instability in tunnel field-effect transistors. Japanese Journal of Applied Physics, 2017, 56, 04CA04.	1.5	2
7	Enhanced nickelidation rate in silicon nanowires with interfacial lattice disorder. Journal of Applied Physics, 2017, 122, .	2.5	6
8	Epitaxial growth of Ge thin film on Si (001) by DC magnetron sputtering. Materials Science in Semiconductor Processing, 2017, 70, 3-7.	4.0	4
9	Suppression of tunneling rate fluctuations in tunnel field-effect transistors by enhancing tunneling probability. Japanese Journal of Applied Physics, 2017, 56, 04CD02.	1.5	5
10	ON current enhancement of nanowire Schottky barrier tunnel field effect transistors. Japanese Journal of Applied Physics, 2016, 55, 04ED07.	1.5	3
11	Impact of extension implantation conditions of fin field-effect transistors on gate-induced drain leakage. Japanese Journal of Applied Physics, 2016, 55, 04EB01.	1.5	3
12	(Invited) Floating Gate Type SOI-FinFET Flash Memories with Different Channel Shapes and Interpoly Dielectric Materials. ECS Transactions, 2016, 72, 11-24.	0.5	1
13	Introduction of SiGe/Si heterojunction into novel multilayer tunnel FinFET. Japanese Journal of Applied Physics, 2016, 55, 04EB06.	1.5	15
14	Closed-form analytical model of static noise margin for ultra-low voltage eight-transistor tunnel FET static random access memory. Japanese Journal of Applied Physics, 2016, 55, 04ED06.	1.5	4
15	Robust and compact key generator using physically unclonable function based on logic-transistor-compatible poly-crystalline-Si channel FinFET technology. , 2015, , .		5
16	Spatial variation of the work function in nano-crystalline TiN films measured by dual-mode scanning tunneling microscopy. Japanese Journal of Applied Physics, 2015, 54, 04DA03.	1.5	14
17	Heated ion implantation for high-performance and highly reliable silicon-on-insulator complementary metalâ€“oxideâ€“silicon fin field-effect transistors. Japanese Journal of Applied Physics, 2015, 54, 04DA06.	1.5	4
18	Impact of granular work function variation in a gate electrode on low-frequency noise for fin field-effect transistors. Applied Physics Express, 2015, 8, 044201.	2.4	7

#	Article	IF	Citations
19	Effect of hot implantation on ON-current enhancement utilizing isoelectronic trap in Si-based tunnel field-effect transistors. Applied Physics Express, 2015, 8, 036503.	2.4	9
20	Impact of fin length on threshold voltage modulation by back bias for Independent double-gate tunnel fin field-effect transistors. Solid-State Electronics, 2015, 111, 62-66.	1.4	3
21	Highly Vt tunable and low variability triangular fin-channel MOSFETs on SOTB. Microelectronic Engineering, 2015, 147, 290-293.	2.4	0
22	Study of gate leakage current paths in p-channel tunnel field-effect transistor by current separation measurement and device simulation. Japanese Journal of Applied Physics, 2015, 54, 034202.	1.5	1
23	Improvement of epitaxial channel quality on heavily arsenic- and boron-doped Si surfaces and impact on performance of tunnel field-effect transistors. Solid-State Electronics, 2015, 113, 173-178.	1.4	6
24	Study of tunneling transport in Si-based tunnel field-effect transistors with ON current enhancement utilizing isoelectronic trap. Applied Physics Letters, 2015, 106, .	3.3	54
25	Channel shape and interpoly dielectric material effects on electrical characteristics of floating-gate-type three-dimensional fin channel flash memories. Japanese Journal of Applied Physics, 2015, 54, 04DD04.	1.5	2
26	Comparative Study of Charge Trapping Type SOI-FinFET Flash Memories with Different Blocking Layer Materials. Journal of Low Power Electronics and Applications, 2014, 4, 153-167.	2.0	5
27	Unexpected equivalent-oxide-thickness dependence of the subthreshold swing in tunnel field-effect transistors. Applied Physics Express, 2014, 7, 024201.	2.4	35
28	Scaling breakthrough for analog/digital circuits by suppressing variability and low-frequency noise for FinFETs by amorphous metal gate technology. , 2014, , .		4
29	Ultra-compact 8 Ã— 8 strictly-non-blocking Si-wire PILOSS switch. Optics Express, 2014, 22, 3887.	3.4	105
30	Band-to-band tunneling current enhancement utilizing isoelectronic trap and its application to TFETs. , 2014, , .		22
31	Heated ion implantation technology for FinFET application. , 2014, , .		2
32	Importance of interface engineering for synthesis of SrHfO₃ perovskite thin films on Si substrates through crystallization of amorphous films and control of flat-band voltages of metalâ€“oxideâ€“semiconductor capacitors. Japanese Journal of Applied Physics, 2014, 53, 04EA03.	1.5	4
33	Impact of thermal history of Si nanowire fabrication process on Ni silicidation rate. Japanese Journal of Applied Physics, 2014, 53, 085201.	1.5	4
34	Influence of work function variation of metal gates on fluctuation of sub-threshold drain current for fin field-effect transistors with undoped channels. Japanese Journal of Applied Physics, 2014, 53, 04EC11.	1.5	12
35	Experimental study of three-dimensional fin-channel charge trapping flash memories with titanium nitride and polycrystalline silicon gates. Japanese Journal of Applied Physics, 2014, 53, 04ED16.	1.5	2
36	(Invited) Charge Trapping Type SOI-FinFET Flash Memory. ECS Transactions, 2014, 61, 263-280.	0.5	4

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37	Performance Enhancement of Tunnel Field-Effect Transistors by Synthetic Electric Field Effect. IEEE Electron Device Letters, 2014, 35, 792-794.	3.9	53
38	Predictivity of the non-local BTBT model for structure dependencies of tunnel FETs. , 2014, , .		9
39	Performance evaluation of parallel electric field tunnel field-effect transistor by a distributed-element circuit model. Solid-State Electronics, 2014, 102, 82-86.	1.4	7
40	Experimental Demonstration of Ultrashort-Channel (3 nm) Junctionless FETs Utilizing Atomically Sharp V-Grooves on SOI. IEEE Nanotechnology Magazine, 2014, 13, 208-215.	2.0	59
41	Analysis of Threshold Voltage Flexibility in Ultrathin-BOX SOI FinFETs. Journal of Low Power Electronics and Applications, 2014, 4, 110-118.	2.0	1
42	Experimental study of charge trapping type FinFET flash memory. , 2014, , .		0
43	SOI CMOS Voltage Multiplier Circuits with Body Bias Control Technique for Battery-Less Wireless Sensor System. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2014, E97.A, 741-748.	0.3	0
44	Impact of atomic-scale structural design on ultra-short channel (3 nm) MOSFETs. , 2013, , .		1
45	Variability of short channel junctionless field-effect transistors caused by fluctuation of dopant concentration. , 2013, , .		1
46	Two-step annealing effects on ultrathin EOT higher-k (k=40) ALD-HfO2 gate stacks. Solid-State Electronics, 2013, 84, 58-64.	1.4	11
47	1/fNoise Characteristics of Fin-Type Field-Effect Transistors in Saturation Region. Japanese Journal of Applied Physics, 2013, 52, 04CC23.	1.5	0
48	A compact model for tunnel field-effect transistors incorporating nonlocal band-to-band tunneling. Journal of Applied Physics, 2013, 114, 144512.	2.5	25
49	Large current MOSFET on photonic silicon-on-insulator wafers and its monolithic integration with a thermoâ€“optic 2 Ã— 2 Machâ€“Zehnder switch. Optics Express, 2013, 21, 6889.	3.4	21
50	(Invited) Independent-Double-Gate FinFET SRAM Technology. ECS Transactions, 2013, 50, 193-199.	0.5	0
51	Tunnel Field-Effect Transistor with Epitaxially Grown Tunnel Junction Fabricated by Source/Drain-First and Tunnel-Junction-Last Processes. Japanese Journal of Applied Physics, 2013, 52, 04CC25.	1.5	16
52	Gate Structure Dependence of Variability in Polycrystalline Silicon Fin-Channel Flash Memories. Japanese Journal of Applied Physics, 2013, 52, 06GE01.	1.5	3
53	Atomic Layer Deposition of SiO₂ for the Performance Enhancement of Fin Field Effect Transistors. Japanese Journal of Applied Physics, 2013, 52, 116503.	1.5	8
54	(Invited) Extremely Short Channel Si-MOSFETs Prepared on SOI Substrates Using Anisotropic Wet Etching. ECS Transactions, 2013, 58, 273-280.	0.5	0

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55	Suppression of threshold voltage variability of double-gate fin field-effect transistors using amorphous metal gate with uniform work function. Applied Physics Letters, 2013, 102, .	3.3	15
56	Fabrication and Demonstration of 3-nm-Channel-Length Junctionless Field-Effect Transistors on Silicon-on-Insulator Substrates Using Anisotropic Wet Etching and Lateral Diffusion of Dopants. Japanese Journal of Applied Physics, 2013, 52, 04CA01.	1.5	21
57	Independent-Double-Gate FinFET SRAM Technology. IEICE Transactions on Electronics, 2013, E96.C, 413-423.	0.6	1
58	Fabrication of Floating-Gate-Type Fin-Channel Double- and Tri-Gate Flash Memories and Comparative Study of Their Electrical Characteristics. Japanese Journal of Applied Physics, 2012, 51, 04DD03.	1.5	2
59	Fabrication and Characterization of NOR-Type Tri-Gate Flash Memory with Improved Inter-Poly Dielectric Layer by Rapid Thermal Oxidation. Japanese Journal of Applied Physics, 2012, 51, 06FE19.	1.5	6
60	Experimental Study of Floating-Gate-Type Metalâ€“Oxideâ€“Semiconductor Capacitors with Nanosize Triangular Cross-Sectional Tunnel Areas for Low Operating Voltage Flash Memory Application. Japanese Journal of Applied Physics, 2012, 51, 06FF01.	1.5	2
61	Experimental Comparisons between Tetrakis(dimethylamino)titanium Precursor-Based Atomic-Layer-Deposited and Physical-Vapor-Deposited Titaniumâ€“Nitride Gate for High-Performance Fin-Type Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2012, 51, 04DA05.	1.5	0
62	(Invited) FinFET Flash Memory Technology. ECS Transactions, 2012, 45, 289-310.	0.5	2
63	(Invited) On-Current Variability Sources of FinFETs: Analysis and Perspective for 14nm-Lg Technology. ECS Transactions, 2012, 45, 231-242.	0.5	0
64	Suppressing V<inf>t</inf> and G<inf>m</inf> variability of FinFETs using amorphous metal gates for 14 nm and beyond. , 2012, , .		22
65	Enhancement of FinFET performance using 25-nm-thin sidewall spacer grown by atomic layer deposition. Solid-State Electronics, 2012, 74, 13-18.	1.4	13
66	Demonstration of Split-Gate Type Trigate Flash Memory With Highly Suppressed Over-Erase. IEEE Electron Device Letters, 2012, 33, 345-347.	3.9	10
67	Variability Origins of Parasitic Resistance in FinFETs With Silicided Source/Drain. IEEE Electron Device Letters, 2012, 33, 474-476.	3.9	15
68	Variability Analysis of Scaled Crystal Channel and Poly-Si Channel FinFETs. IEEE Transactions on Electron Devices, 2012, 59, 573-581.	3.0	12
69	Fin-Height Effect on Poly-Si/PVD-TiN Stacked-Gate FinFET Performance. IEEE Transactions on Electron Devices, 2012, 59, 647-653.	3.0	14
70	A Correlative Analysis Between Characteristics of FinFETs and SRAM Performance. IEEE Transactions on Electron Devices, 2012, 59, 1345-1352.	3.0	3
71	Decomposition of On-Current Variability of nMOS FinFETs for Prediction Beyond 20 nm. IEEE Transactions on Electron Devices, 2012, 59, 2003-2010.	3.0	27
72	High-Frequency Precise Characterization of Intrinsic FinFET Channel. IEICE Transactions on Electronics, 2012, E95.C, 752-760.	0.6	1

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73	Fabrication and Characterization of NOR-Type Tri-Gate Flash Memory with Improved Inter-Poly Dielectric Layer by Rapid Thermal Oxidation. Japanese Journal of Applied Physics, 2012, 51, 06FE19.	1.5	2
74	A 0.7-V Opamp in Scaled Low-Standby-Power FinFET Technology. IEICE Transactions on Electronics, 2012, E95.C, 686-695.	0.6	0
75	Fabrication of Floating-Gate-Type Fin-Channel Double- and Tri-Gate Flash Memories and Comparative Study of Their Electrical Characteristics. Japanese Journal of Applied Physics, 2012, 51, 04DD03.	1.5	1
76	Experimental Comparisons between Tetrakis(dimethylamino)titanium Precursor-Based Atomic-Layer-Deposited and Physical-Vapor-Deposited Titaniumâ€“Nitride Gate for High-Performance Fin-Type Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2012, 51, 04DA05.	1.5	2
77	Experimental Study of Floating-Gate-Type Metalâ€“Oxideâ€“Semiconductor Capacitors with Nanosize Triangular Cross-Sectional Tunnel Areas for Low Operating Voltage Flash Memory Application. Japanese Journal of Applied Physics, 2012, 51, 06FF01.	1.5	1
78	Variability origins of FinFETs and perspective beyond 20nm node. , 2011, , .		3
79	Atomic layer deposition of 25-nm-thin sidewall spacer for enhancement of FinFET performance. , 2011, , .		2
80	Independent double-gate FinFET SRAM technology. , 2011, , .		4
81	Static noise margin enhancement by flex-pass-gate SRAM. Electronics and Communications in Japan, 2011, 94, 57-64.	0.5	0
82	Comprehensive analysis of I<inf>on</inf> variation in metal gate FinFETs for 20nm and beyond. , 2011, , .		7
83	Tunnel Field-Effect Transistors with Extremely Low Off-Current Using Shadowing Effect in Drain Implantation. Japanese Journal of Applied Physics, 2011, 50, 06GF14.	1.5	7
84	Correlative analysis between characteristics of 30-nm L<inf>G</inf> FinFETs and SRAM performance. , 2011, , .		1
85	Low activation energy, high-quality oxidation of Si and Ge using neutral beam. Applied Physics Letters, 2011, 98, 203111.	3.3	21
86	Experimental Study of Physical-Vapor-Deposited Titanium Nitride Gate with An n⁺-Polycrystalline Silicon Capping Layer and Its Application to 20 nm Fin-Type Double-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2011, 50, 04DC14.	1.5	12
87	Experimental Study of Physical-Vapor-Deposited Titanium Nitride Gate with An n+-Polycrystalline Silicon Capping Layer and Its Application to 20 nm Fin-Type Double-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2011, 50, 04DC14.	1.5	6
88	Tunnel Field-Effect Transistors with Extremely Low Off-Current Using Shadowing Effect in Drain Implantation. Japanese Journal of Applied Physics, 2011, 50, 06GF14.	1.5	13
89	Fabrication of Four-Terminal Fin Field-Effect Transistors with Asymmetric Gate-Oxide Thickness Using an Anisotropic Oxidation Process with a Neutral Beam. Applied Physics Express, 2010, 3, 096502.	2.4	5
90	Design of SOI FinFET on 32nm technology node for low standby power (LSTP) operation considering gate-induced drain leakage (GIDL). Solid-State Electronics, 2010, 54, 1060-1065.	1.4	7

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91	(Invited) Advanced FinFET Technologies: Extension Doping, Vth Controllable CMOS Inverters and SRAM. ECS Transactions, 2010, 28, 385-401.	0.5	1
92	Investigation of Low-Energy Tilted Ion Implantation for Fin-Type Double-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistor Extension Doping. Japanese Journal of Applied Physics, 2010, 49, 04DC18.	1.5	22
93	High-Performance Three-Terminal Fin Field-Effect Transistors Fabricated by a Combination of Damage-Free Neutral-Beam Etching and Neutral-Beam Oxidation. Japanese Journal of Applied Physics, 2010, 49, 04DC17.	1.5	11
94	Minimization of Gate-Induced Drain Leakage by Controlling Gate Underlap Length for Low-Standby-Power Operation of 20-nm-Level Four-Terminal Silicon-on-Insulator Fin-Shaped Field Effect Transistor. Japanese Journal of Applied Physics, 2010, 49, 024203.	1.5	0
95	Investigation of Thermal Stability of TiN Film Formed by Atomic Layer Deposition Using Tetrakis(dimethylamino)titanium Precursor for Metal-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistor. Japanese Journal of Applied Physics, 2010, 49, 04DA16.	1.5	7
96	Variability Analysis of TiN Metal-Gate FinFETs. IEEE Electron Device Letters, 2010, 31, 546-548.	3.9	63
97	Variability analysis of TiN FinFET SRAM cell performance and its compensation using Vth-controllable independent double-gate FinFET. , 2010, , .		0
98	Variability Analysis of TiN FinFET SRAM Cells and Its Compensation by Independent-DG FinFETs. IEEE Electron Device Letters, 2010, 31, 1095-1097.	3.9	4
99	Nanoscale Wet Etching of Physical-Vapor-Deposited Titanium Nitride and Its Application to Sub-30-nm-Gate-Length Fin-Type Double-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistor Fabrication. Japanese Journal of Applied Physics, 2010, 49, 06GH18.	1.5	27
100	On the gate-stack origin threshold voltage variability in scaled FinFETs and multi-FinFETs. , 2010, , .		32
101	Rigorous Design of 22-nm Node 4-Terminal SOI FinFETs for Reliable Low Standby Power Operation with Semi-empirical Parameters. Journal of Semiconductor Technology and Science, 2010, 10, 265-275.	0.4	5
102	Independent-Double-Gate FINFET SRAM Cell for Drastic Leakage Current Reduction. Lecture Notes in Electrical Engineering, 2010, , 67-79.	0.4	0
103	Enhancing Noise Margins of Fin-Type Field Effect Transistor Static Random Access Memory Cell by Using Threshold Voltage-Controllable Flexible-Pass-Gates. Applied Physics Express, 2009, 2, 054502.	2.4	4
104	Experimental evaluation of parallel transmission using optical ZCZ-CDMA system. , 2009, , .		2
105	Low Temperature, Beam-Orientation-Dependent, Lattice-Plane-Independent, and Damage-Free Oxidation for Three-Dimensional Structure by Neutral Beam Oxidation. Japanese Journal of Applied Physics, 2009, 48, 04C007.	1.5	21
106	A Comparative Study of Nitrogen Gas Flow Ratio Dependence on the Electrical Characteristics of Sputtered Titanium Nitride Gate Bulk Planar Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors and Fin-Type Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2009, 48, 05DC01.	1.5	23
107	Vertical ultrathinâ€channel multiâ€gate MOSFETs (MuGFETs): technological challenges and future developments. IEEJ Transactions on Electrical and Electronic Engineering, 2009, 4, 386-391.	1.4	2
108	Dual metal gate FinFET integration by Ta/Mo diffusion technology for Vt reduction and multi-Vt CMOS application. Solid-State Electronics, 2009, 53, 701-705.	1.4	3

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109	Fluctuation Analysis of Parasitic Resistance in FinFETs With Scaled Fin Thickness. IEEE Electron Device Letters, 2009, 30, 407-409.	3.9	23
110	Metal-Gate FinFET Variation Analysis by Measurement and Compact Model. IEEE Electron Device Letters, 2009, 30, 556-558.	3.9	11
111	Independent-Double-Gate FinFET SRAM for Leakage Current Reduction. IEEE Electron Device Letters, 2009, 30, 757-759.	3.9	24
112	Vertical doubleâ€gate MOSFET device technology. Electronics and Communications in Japan, 2008, 91, 46-51.	0.5	4
113	Flex-pass-gate SRAM for static noise margin enhancement using FinFET-based technology. Solid-State Electronics, 2008, 52, 1694-1702.	1.4	1
114	Threshold-Voltage Reduction of FinFETs by Ta/Mo Interdiffusion Dual Metal-Gate Technology for Low-Operating-Power Application. IEEE Transactions on Electron Devices, 2008, 55, 2454-2461.	3.0	12
115	Independent-gate four-terminal FinFET SRAM for drastic leakage current reduction. , 2008, , .		1
116	Enhancing SRAM cell performance by using independent double-gate FinFET. , 2008, , .		30
117	Dual metal gate FinFET integration by Ta/Mo diffusion technology for Vt reduction and multi-Vt CMOS application. , 2008, , .		8
118	Variable-Threshold-Voltage FinFETs with a Control-Voltage Range within the Logic-Level Swing Using Asymmetric Work-Function Double Gates. International Power Modulator Symposium and High-Voltage Workshop, 2008, , .	0.0	0
119	Enhancing noise margins of FinFET SRAM by integrating V<inf>th</inf>-controllable flexible-pass-gates. , 2008, , .		3
120	Logic gate threshold voltage controllable single metal gate FinFET CMOS inverters implemented by using co-integration of 3T/4T-FinFETs. , 2008, , .		2
121	Impact of extension and source/drain resistance on FinFET performance. , 2008, , .		6
122	A Ta/Mo Interdiffusion Dual Metal Gate Technology for Drivability Enhancement of FinFETs. IEEE Electron Device Letters, 2008, 29, 618-620.	3.9	9
123	Dual-Metal-Gate Transistors with Symmetrical Threshold Voltages Using Work-Function-Tuned Ta/Mo Bilayer Metal Gates. Japanese Journal of Applied Physics, 2008, 47, 2428-2432.	1.5	4
124	Nitrogen Gas Flow Ratio and Rapid Thermal Annealing Temperature Dependences of Sputtered Titanium Nitride Gate Work Function and Their Effect on Device Characteristics. Japanese Journal of Applied Physics, 2008, 47, 2433.	1.5	20
125	Static Noise Margin Enhancement by Flex-Pass-Gate SRAM. IEEJ Transactions on Electronics, Information and Systems, 2008, 128, 919-925.	0.2	0
126	FinFET-Based Flex-Vth SRAM Design for Drastic Standby-Leakage-Current Reduction. IEICE Transactions on Electronics, 2008, E91-C, 534-542.	0.6	2

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127	Ta/Mo Stack Dual Metal Gate Technology Applicable to Gate-First Processes. Japanese Journal of Applied Physics, 2007, 46, 1825-1829.	1.5	4
128	Flex-Pass-Gate SRAM Design for Static Noise Margin Enhancement Using FinFET-Based Technology. , 2007, , .		13
129	Experimental Evaluation of Effects of Channel Doping on Characteristics of FinFETs. IEEE Electron Device Letters, 2007, 28, 1123-1125.	3.9	28
130	Nitrogen gas flow ratio controlled PVD TiN metal gate technology for FinFET CMOS. , 2007, , .		0
131	Cointegration of High-Performance Tied-Gate Three-Terminal FinFETs and Variable Threshold-Voltage Independent-Gate Four-Terminal FinFETs With Asymmetric Gate-Oxide Thicknesses. IEEE Electron Device Letters, 2007, 28, 517-519.	3.9	48
132	Demonstration of Asymmetric Gate-Oxide Thickness Four-Terminal FinFETs Having Flexible Threshold Voltage and Good Subthreshold Slope. IEEE Electron Device Letters, 2007, 28, 217-219.	3.9	31
133	A Dynamical Power-Management Demonstration Using Four-Terminal Separated-Gate FinFETs. IEEE Electron Device Letters, 2007, 28, 452-454.	3.9	9
134	Four-Terminal FinFETs Fabricated Using an Etch-Back Gate Separation. IEEE Nanotechnology Magazine, 2007, 6, 201-205.	2.0	18
135	Independent double-gate FinFETs with asymmetric gate stacks. Microelectronic Engineering, 2007, 84, 2097-2100.	2.4	6
136	Experimental Investigation of Optimum Gate Workfunction for CMOS Four-Terminal Multigate MOSFETs (MUGFETs). IEEE Transactions on Electron Devices, 2007, 54, 1431-1437.	3.0	11
137	A novel approach to Au nanoparticle-based identification of DNA nanoarrays. Frontiers in Bioscience - Landmark, 2007, 12, 4773.	3.0	3
138	Optimum Gate Workfunction for $V_{m th}$-Controllable Four-Terminal-Driven Double-Gate MOSFETs (4T-XMOSFETs)â€"Band-Edge Workfunction Versus Midgap Workfunction. IEEE Nanotechnology Magazine, 2006, 5, 716-722.	2.0	12
139	Investigation of the TiN Gate Electrode With Tunable Work Function and Its Application for FinFET Fabrication. IEEE Nanotechnology Magazine, 2006, 5, 723-730.	2.0	90
140	Fabrication of FinFETs by Damage-Free Neutral-Beam Etching Technology. IEEE Transactions on Electron Devices, 2006, 53, 1826-1833.	3.0	37
141	Investigation of N-Channel Triple-Gate Metalâ€"Oxideâ€"Semiconductor Field-Effect Transistors on (100) Silicon On Insulator Substrate. Japanese Journal of Applied Physics, 2006, 45, 3097-3100.	1.5	8
142	Demonstration and Analysis of Accumulation-Mode Double-Gate Metalâ€"Oxideâ€"Semiconductor Field-Effect Transistor. Japanese Journal of Applied Physics, 2006, 45, 3079-3083.	1.5	5
143	Experimental Study of Effective Carrier Mobility of Multi-Fin-Type Double-Gate Metalâ€"Oxideâ€"Semiconductor Field-Effect Transistors with (111) Channel Surface Fabricated by Orientation-Dependent Wet Etching. Japanese Journal of Applied Physics, 2006, 45, 3084-3087.	1.5	18
144	New Fabrication Technology of Fin Field Effect Transistors Using Neutral-Beam Etching. Japanese Journal of Applied Physics, 2006, 45, 5513-5516.	1.5	5

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145	Fabrication of a Vertical-Channel Double-Gate Metal-Oxide-Semiconductor Field-Effect Transistor Using a Neutral Beam Etching. Japanese Journal of Applied Physics, 2006, 45, L279-L281.	1.5	9
146	Doping integrity diagnostics of planar transistor channel structures by scanning nonlinear dielectric microscopy. Journal of Vacuum Science & Technology B, 2006, 24, 237.	1.3	0
147	Advanced FinFET CMOS Technology: TiN-Gate, Fin-Height Control and Asymmetric Gate Insulator Thickness 4T-FinFETs. , 2006, , .		28
148	Fabrication and characterization of vertical-type double-gate metal-oxide-semiconductor field-effect transistor with ultrathin Si channel and self-aligned source and drain. Applied Physics Letters, 2006, 88, 072103.	3.3	7
149	Electron mobility in multi-FinFET with a (111) channel surface fabricated by orientation-dependent wet etching. Microelectronic Engineering, 2005, 80, 390-393.	2.4	5
150	Demonstration, Analysis, and Device Design Considerations for Independent DG MOSFETs. IEEE Transactions on Electron Devices, 2005, 52, 2046-2053.	3.0	115
151	A Novel Process for Fabrication of Gated Silicon Field Emitter Array Taking Advantage of Ion Bombardment Retarded Etching. Japanese Journal of Applied Physics, 2005, 44, 5191-5192.	1.5	1
152	Device Design Consideration forVth-Controllable Four-Terminal Double-Gate Metal-Oxide-Semiconductor Field-Effect Transistor. Japanese Journal of Applied Physics, 2005, 44, 2351-2356.	1.5	1
153	Demonstration of Dopant Profiling in Ultrathin Channels of Vertical-Type Double-Gate Metal-Oxide-Semiconductor Field-Effect-Transistor by Scanning Nonlinear Dielectric Microscopy. Japanese Journal of Applied Physics, 2005, 44, 2400-2404.	1.5	2
154	Work function uniformity of Alâ€“Ni alloys obtained by scanning Maxwell-stress microscopy as an effective tool for evaluating metal transistor gates. Applied Physics Letters, 2005, 86, 094104.	3.3	9
155	Fabrication and characterization of vertical-type, self-aligned asymmetric double-gate metal-oxide-semiconductor field-effect-transistors. Applied Physics Letters, 2005, 86, 123512.	3.3	9
156	P-Channel Vertical Double-Gate MOSFET Fabricated by Utilizing Ion-Bombardment-Retarded Etching Processs. Japanese Journal of Applied Physics, 2004, 43, 2156-2159.	1.5	2
157	Cross-Sectional Channel Shape Dependence of Short-Channel Effects in Fin-Type Double-Gate Metal Oxide Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2004, 43, 2151-2155.	1.5	39
158	Dopant profiling in vertical ultrathin channels of double-gate metalâ€“oxideâ€“semiconductor field-effect transistors by using scanning nonlinear dielectric microscopy. Applied Physics Letters, 2004, 85, 4139-4141.	3.3	22
159	Diagnostics of doping integrity in n+/p/n+ transistor-channel structure by scanning nonlinear dielectric microscopy. Applied Physics Letters, 2004, 84, 3169-3171.	3.3	6
160	A Highly Threshold Voltage-Controllable 4T FinFET with an 8.5-nm-Thick Si-Fin Channel. IEEE Electron Device Letters, 2004, 25, 510-512.	3.9	97
161	Ideal rectangular cross-section Si-Fin channel double-gate MOSFETs fabricated using orientation-dependent wet etching. IEEE Electron Device Letters, 2003, 24, 484-486.	3.9	83
162	Systematic electrical characteristics of ideal rectangular cross section si-fin channel double-gate MOSFETs fabricated by a wet process. IEEE Nanotechnology Magazine, 2003, 2, 198-204.	2.0	21

#	Article	IF	Citations
163	Fin-Type Double-Gate Metal-Oxide-Semiconductor Field-Effect Transistors Fabricated by Orientation-Dependent Etching and Electron Beam Lithography. Japanese Journal of Applied Physics, 2003, 42, 4142-4146.	1.5	21
164	Doping diagnosis by evaluation of the surface Fermi level using scanning Maxwell-stress microscopy. Applied Physics Letters, 2003, 82, 2166-2168.	3.3	3
165	Programmable Conductivity of Silicon Nanowires with Side Gates by Surface Charging. Japanese Journal of Applied Physics, 2003, 42, 2422-2425.	1.5	1
166	Fabrication of ultrathin Si Channel Wall For Vertical Double-Gate Metal-Oxide-Semiconductor Field-Effect Transistor (DG MOSFET) by Using Ion-Bombardment-Retarded Etching (IBRE). Japanese Journal of Applied Physics, 2003, 42, 1916-1918.	1.5	13
167	Novel Process for Vertical Double-Gate (DG) Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) Fabrication. Japanese Journal of Applied Physics, 2003, 42, 4138-4141.	1.5	7
168	Silicon nanowire with programmable conductivity analyzed by scanning Maxwell-stress microscopy. Journal of Vacuum Science & Technology an Official Journal of the American Vacuum Society B, Microelectronics Processing and Phenomena, 2003, 21, 664.	1.6	3
169	Silicon nanowire memory using surface charging and its operation analysis by scanning Maxwell-stress microcopy (SMM). , 0, , .		0
170	Flexible threshold voltage 4-terminal FinFETs. , 0, , .		0
171	Demonstration of threshold voltage control techniques for vertical-type 4-terminal double-gate MOSFETs (4T-DGFET). , 0, , .		4
172	Work function control of metal gates by interdiffused Ni-Ta with high thermal stability. , 0, , .		0