Abhinav Kranti

List of Publications by Year
in descending order

74 papers	1,655 citations	257450 24 h-index	302126 39 g-index
74 all docs	74 docs citations	74 times ranked	791 citing authors

#	Article	IF	Citations
1	Junctionless Multiple-Gate Transistors for Analog Applications. IEEE Transactions on Electron Devices, 2011, 58, 2511-2519.	3.0	234
2	Design and Optimization of FinFETs for Ultra-Low-Voltage Analog Applications. IEEE Transactions on Electron Devices, 2007, 54, 3308-3316.	3.0	102
3	High-Performance Junctionless MOSFETs for Ultralow-Power Analog/RF Applications. IEEE Electron Device Letters, 2012, 33, 1477-1479.	3.9	99
4	Ultra Low Power Junctionless MOSFETs for Subthreshold Logic Applications. IEEE Transactions on Electron Devices, 2013, 60, 1540-1546.	3.0	78
5	Source/Drain Extension Region Engineering in FinFETs for Low-Voltage Analog Applications. IEEE Electron Device Letters, 2007, 28, 139-141.	3.9	77
6	Engineering source/drain extension regions in nanoscale double gate (DG) SOI MOSFETs: Analytical model and design considerations. Solid-State Electronics, 2006, 50, 437-447.	1.4	65
7	Dielectric Modulated Biosensor Architecture: Tunneling or Accumulation Based Transistor?. IEEE Sensors Journal, 2018, 18, 3228-3235.	4.7	64
8	Enhanced sensitivity of double gate junctionless transistor architecture for biosensing applications. Nanotechnology, 2015, 26, 145201.	2.6	54
9	Applicability of Transconductance-to-Current Ratio ($g_{mathrm {m}}/I_{mathrm {ds}}$) as a Sensing Metric for Tunnel FET Biosensors. IEEE Sensors Journal, 2017, 17, 1030-1036.	4.7	54
10	Revisiting the doping requirement for low power junctionless MOSFETs. Semiconductor Science and Technology, 2014, 29, 075006.	2.0	41
11	Bipolar effects in unipolar junctionless transistors. Applied Physics Letters, 2012, 101, 093507.	3.3	39
12	Improved Retention Time in Twin Gate 1T DRAM With Tunneling Based Read Mechanism. IEEE Electron Device Letters, 2016, 37, 1127-1130.	3.9	37
13	Investigation of barrier inhomogeneities and interface state density in Au/MgZnO: Ga Schottky contact. Journal Physics D: Applied Physics, 2016, 49, 445303.	2.8	36
14	Overcoming Biomolecule Location-Dependent Sensitivity Degradation Through Point and Line Tunneling in Dielectric Modulated Biosensors. IEEE Sensors Journal, 2018, 18, 9604-9611.	4.7	35
15	Investigation of high-performance sub-50nm junctionless nanowire transistors. Microelectronics Reliability, 2011, 51, 1166-1171.	1.7	32
16	Device Design and Estimated Performance for p-Type Junctionless Transistors on Bulk Germanium Substrates. IEEE Transactions on Electron Devices, 2012, 59, 2308-2313.	3.0	31
17	Retention and Scalability Perspective of Sub-100-nm Double Gate Tunnel FET DRAM. IEEE Transactions on Electron Devices, 2017, 64, 1561-1567.	3.0	30
18	Gate-All-Around Nanowire Junctionless Transistor-Based Hydrogen Gas Sensor. IEEE Sensors Journal, 2019, 19, 4758-4764.	4.7	30

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19	A Simulation Comparison between Junctionless and Inversion-Mode MuGFETs. ECS Transactions, 2011, 35, 63-72.	0.5	29
20	Single transistor latch phenomenon in junctionless transistors. Journal of Applied Physics, 2013, 113, .	2.5	29
21	Improving retention time in tunnel field effect transistor based dynamic memory by back gate engineering. Journal of Applied Physics, 2016, 119, .	2.5	28
22	Buffer Layer Engineering for High ($geq 10^{mathrm {13}}$ cm $^{mathrm {-2}}$) 2-DEG Density in ZnO-Based Heterostructures. IEEE Transactions on Electron Devices, 2017, 64, 1015-1019.	3.0	26
23	Analytical Model for 2DEG Density in Graded MgZnO/ZnO Heterostructures With Cap Layer. IEEE Transactions on Electron Devices, 2017, 64, 3661-3667.	3.0	26
24	Two-dimensional electron gases in MgZnO/ZnO and ZnO/MgZnO/ZnO heterostructures grown by dual ion beam sputtering. Journal Physics D: Applied Physics, 2018, 51, 13LT02.	2.8	26
25	A Model for Gate-Underlap-Dependent Short- Channel Effects in Junctionless MOSFET. IEEE Transactions on Electron Devices, 2018, 65, 881-887.	3.0	26
26	Bipolar snapback in junctionless transistors for capacitorless dynamic random access memory. Applied Physics Letters, 2012, 101, .	3.3	24
27	Modeling Short-Channel Effects in Asymmetric Junctionless MOSFETs With Underlap. IEEE Transactions on Electron Devices, 2018, 65, 3669-3675.	3.0	21
28	1T-DRAM With Shell-Doped Architecture. IEEE Transactions on Electron Devices, 2019, 66, 428-435.	3.0	21
29	Modeling Short-Channel Effects in Coreâ€“Shell Junctionless MOSFET. IEEE Transactions on Electron Devices, 2019, 66, 292-299.	3.0	21
30	Doping Dependent Assessment of Accumulation Mode and Junctionless FET for 1T DRAM. IEEE Transactions on Electron Devices, 2018, 65, 1205-1210.	3.0	20
31	Back bias induced dynamic and steep subthreshold swing in junctionless transistors. Applied Physics Letters, 2014, 105, .	3.3	14
32	Limits on Hysteresis-Free Sub-60 mV/Decade Operation of MFIS Nanowire Transistor. IEEE Transactions on Electron Devices, 2020, 67, 3868-3875.	3.0	14
33	A New Electron Bridge Channel 1T-DRAM Employing Underlap Region Charge Storage. IEEE Journal of the Electron Devices Society, 2017, 5, 59-63.	2.1	12
34	Extraction of mobility and Degradation coefficients in double gate junctionless transistors. Semiconductor Science and Technology, 2017, 32, 125011.	2.0	10
35	Overcoming the drawback of lower sense margin in tunnel FET based dynamic memory along with enhanced charge retention and scalability. Nanotechnology, 2017, 28, 445203.	2.6	10
36	Steep-Switching Germanium Junctionless MOSFET With Reduced OFF-State Tunneling. IEEE Transactions on Electron Devices, 2017, 64, 3582-3587.	3.0	10

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37	Enhanced Sheet Charge Density in DIBS Grown CdO Alloyed ZnO Buffer Based Heterostructure. IEEE Electron Device Letters, 2018, 39, 827-830.	3.9	10
38	Sidewall spacer optimization for steep switching junctionless transistors. Semiconductor Science and Technology, 2016, 31, 065017.	2.0	9
39	Variation of Threshold Voltage With Temperature in Impact Ionization-Induced Steep Switching Si and Ge Junctionless MOSFETs. IEEE Transactions on Electron Devices, 2017, 64, 2061-2066.	3.0	9
40	Role of Surface States and Interface Charges in 2DEG in Sputtered ZnO Heterostructures. IEEE Transactions on Electron Devices, 2018, 65, 2850-2854.	3.0	9
41	Raised Body Doping-Less 1T-DRAM With Source/Drain Schottky Contact. IEEE Journal of the Electron Devices Society, 2019, 7, 276-281.	2.1	9
42	Insights into Gate-Underlap Design in FinFETs for Ultra-Low Voltage Analog Performance. SOI Conference, Proceedings of the IEEE International, 2007, , .	0.0	8
43	Insights into operation of planar tri-gate tunnel field effect transistor for dynamic memory application. Journal of Applied Physics, 2017, 122, 044502.	2.5	8
44	High Retention With <inline-formula> <tex-math notation="LaTeX">${n}$ </tex-math> </inline-formula>-Oxide-<inline-formula> <tex-math notation="LaTeX">${p}$ </tex-math> </inline-formula> Junctionless Architecture for 1T DRAM. IEEE Transactions on Electron Devices, 2018, 65, 2797-2803.	3.0	8
45	Vertical Transistor With n-Bridge and Body on Gate for Low-Power 1T-DRAM Application. IEEE Transactions on Electron Devices, 2017, 64, 4937-4945.	3.0	7
46	Raised Source/Drain Germanium Junctionless MOSFET for Subthermal OFF-to-ON Transition. IEEE Transactions on Electron Devices, 2018, 65, 2406-2412.	3.0	7
47	Insights into unconventional behaviour of negative capacitance transistor through a physics-based analytical model. Semiconductor Science and Technology, 2021, 36, 095018.	2.0	6
48	Unconventional VTC of subthreshold inverter with MFMIS negative capacitance transistor: An analytical modelling framework with implications for ultralow power logic design. Semiconductor Science and Technology, 2022, 37, 065012.	2.0	6
49	Enhancing multi-functionality of reconfigurable transistors by implementing high retention capacitorless dynamic memory. Semiconductor Science and Technology, 2021, 36, 115003.	2.0	5
50	Improved Mobility Extraction Methodology for Reconfigurable Transistors Considering Resistive Components and Effective Drain Bias. IEEE Transactions on Electron Devices, 2021, 68, 4797-4800.	3.0	5
51	Source/Drain Extension Region Engineering in Nanoscale Double Gate MOSFETs for Low-Voltage Analog Applications. SOI Conference, Proceedings of the IEEE International, 2006, , .	0.0	4
52	Hysteresis free negative total gate capacitance in junctionless transistors. Semiconductor Science and Technology, 2017, 32, 095014.	2.0	4
53	Performance Assessment of TFET Architectures as 1T-DRAM. , 2018, , .		4
54	Assessment of mobility and its degradation parameters in a shell doped junctionless transistor. Semiconductor Science and Technology, 2018, 33, 115020.	2.0	4

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55	Relevance of Device Cross Section to Overcome Boltzmann Switching Limit in 3-D Junctionless Transistor. IEEE Transactions on Electron Devices, 2019, 66, 2704-2709.	3.0	4
56	An Insightful Assessment of 1T-DRAM With Misaligned Polarity Gate in RFET. IEEE Transactions on Electron Devices, 2022, 69, 3163-3168.	3.0	4
57	Regaining Switching by Overcoming Single-Transistor Latch in Ge Junctionless MOSFETs. IEEE Transactions on Electron Devices, 2018, 65, 3600-3607.	3.0	3
58	Bi-Directional Junctionless Transistor for Logic and Memory Applications. IEEE Transactions on Electron Devices, 2019, 66, 4446-4452.	3.0	3
59	Performance Assessment of Nanoscale Multiple Gate MOSFETs (MuGFETs) for RF Applications. , 2006, , .		2
60	Improving charge retention in capacitorless DRAM through material and device innovation. Japanese Journal of Applied Physics, 2019, 58, SBBB03.	1.5	2
61	Ultra-low-power subthreshold logic with germanium junctionless transistors. Semiconductor Science and Technology, 2021, 36, 075011.	2.0	2
62	A metalâ€“ferroelectricâ€“insulatorâ€“semiconductor transistor perspective: Nanowire or planar architecture?. Journal of Materials Research, 2021, 36, 3484-3494.	2.6	2
63	Incorporating Quantum Effects in Ultralow Power (ULP) Subthreshold Logic Design With Junctionless Nanowire Transistor. IEEE Transactions on Electron Devices, 2022, 69, 3983-3989.	3.0	2
64	Sensitivity implications for programmable transistor based 1T-DRAM. Solid-State Electronics, 2022, 194, 108353.	1.4	2
65	Architecture Evaluation for Standalone and Embedded 1T-DRAM. , 2019, , .		1
66	(Invited) Junctionless Device Cross-Section: A Key Aspect for Overcoming Boltzmann Tyranny. ECS Transactions, 2020, 97, 39-44.	0.5	1
67	1T DRAM with Vertically Stacked n-Oxide-p Architecture. , 2018, , .		0
68	Physical Insights on Junction Controllability for Improved Performance of Planar Trigate Tunnel FET as Capacitorless Dynamic Memory. , 2018, , .		0
69	Retention Enhancement through Architecture Optimization in Junctionless Capacitorless DRAM. , 2018, , .		0
70	Estimation of doping in junctionless transistors through dc characteristics. Semiconductor Science and Technology, 2019, 34, 055020.	2.0	0
71	Enhanced Sheet Carrier Density in ZnO Based Heterostructure by Alloying Cadmium in Buffer Layer ZnO. Springer Proceedings in Physics, 2019, , 1273-1275.	0.2	0
72	Ferroelectric Thickness Dependent Characteristics of Negative Capacitance Transistors. , 2021, , .		0

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73	Investigation of Junctionless Transistor Based DRAM. Springer Proceedings in Physics, 2019, , 629-632.	0.2	0
74	TFET based 1T-DRAM: Physics, Significance and Trade-offs. , 2019, , .		0