M Jagadesh Kumar

List of Publications by Year
in descending order

234 papers	6,806 citations	76326 40 h-index	76900 74 g-index
250 all docs	250 docs citations	250 times ranked	1957 citing authors

#	Article	IF	Citations
1	Digital University â€“ Indian Education Reaching out to Everyone. IETE Technical Review (Institution of) Tj ETQq1 1 0.784314 rgBT /Ov	3.2	2
2	What is in store in the March-April 2021 issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2021, 38, 195-196.	3.2	0
3	Is India going to be a major hub of semiconductor chip manufacturing?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2021, 38, 279-281.	3.2	2
4	COVID-19, Mathematical Models and Optimism. IETE Technical Review (Institution of Electronics and) Tj ETQq0 0 0 rgBT /Overlock 10 Tf	3.2	0
5	Reconfigurable FET Biosensor for a Wide Detection Range and Electrostatically Tunable Sensing Response. IEEE Sensors Journal, 2020, 20, 2261-2269.	4.7	27
6	Sub-10 nm Scalability of Junctionless FETs Using a Ground Plane in High-K BOX: A Simulation Study. IEEE Access, 2020, 8, 137540-137548.	4.2	11
7	National Education Policy: How does it Affect Higher Education in India?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2020, 37, 327-328.	3.2	10
8	What is in store in the September-October 2020 issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2020, 37, 439-440.	3.2	0
9	COVID-19: How Institutions, Teachers and Students in India have geared up for Online Education?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2020, 37, 221-222.	3.2	2
10	What is in store in the January-February 2020 issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2020, 37, 1-2.	3.2	1
11	Efforts of reviewers and editors need to be recognized for their service to the research community and scientific development. IETE Technical Review (Institution of Electronics and Telecommunication) Tj ETQq1 1 0.784314 rgBT /Ove	3.2	9
12	What is in store in January-February 2019 issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2019, 36, 1-2.	3.2	3
13	Investigation of the Scalability of Emerging Nanotube Junctionless FETs Using an Intrinsic Pocket. IEEE Journal of the Electron Devices Society, 2019, 7, 888-896.	2.1	14
14	Nanotube Tunneling FET With a Core Source for Ultrasteep Subthreshold Swing: A Simulation Study. IEEE Transactions on Electron Devices, 2019, 66, 4425-4432.	3.0	49
15	What is in store in the May-June 2019 issue of IETE Technical Review?. IETE Technical Review (Institution) Tj ETQq1 1 0.784314 rgBT /Ov	3.2	0
16	Investigating the Doping Profiles in emerging Nanowire Junctionless Accumulation Mode FETs from the L-BTBT perspective. , 2019, , .		1
17	Realizing a Planar 4H-SiC Junctionless FET for Sub-10-nm Regime Using P⁺ Pocket. IEEE Transactions on Electron Devices, 2019, 66, 3209-3214.	3.0	21
18	National Centre on Artificial Intelligence: India on the Move. IETE Technical Review (Institution of) Tj ETQq0 0 0 rgBT /Overlock 10 Tf 50	3.2	3

#	Article	IF	Citations
19	A Line Tunneling Field-Effect Transistor Based on Misaligned Coreâ€“Shell Gate Architecture in Emerging Nanotube FETs. IEEE Transactions on Electron Devices, 2019, 66, 2809-2816.	3.0	42
20	Controlling L-BTBT in the Ultra-short channel Nanowire Junctionless Accumulation FETs using Overlapping Gate-on- Drain. , 2019, , .		1
21	An Impact Ionization MOSFET With Reduced Breakdown Voltage Based on Back-Gate Misalignment. IEEE Transactions on Electron Devices, 2019, 66, 868-875.	3.0	16
22	Investigating the Scalability of Nanowire Junctionless Accumulation Mode FETs using an Intrinsic Pocket. , 2019, , .		0
23	A New On-Chip ESD Strategy Using TFETs-TCAD Based Device and Network Simulations. IEEE Journal of the Electron Devices Society, 2018, 6, 298-308.	2.1	10
24	Controlling L-BTBT in Emerging Nanotube FETs Using Dual-Material Gate. IEEE Journal of the Electron Devices Society, 2018, 6, 611-621.	2.1	39
25	What is in store in the November-December 2018 issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2018, 35, 549-550.	3.2	0
26	What is in store in store in September-October 2018 issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2018, 35, 439-440.	3.2	0
27	Coming Out of the Past: Time for Engineers to Work Alongside with Social Scientists. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2018, 35, 221-222.	3.2	0
28	Charge Plasma High Voltage PIN Diode Investigation. , 2018, , .		3
29	1-T Capacitorless DRAM Using Laterally Bandgap Engineered Si-Si:C Heterostructure Bipolar I-MOS for Improved Sensing Margin and Retention Time. IEEE Nanotechnology Magazine, 2018, 17, 543-551.	2.0	10
30	Kudos to the Reviewers. IETE Technical Review (Institution of Electronics and Telecommunication) Tj ETQq0 0 0 rgBT /Overlock 10 Tf 50	3.2	1
31	Diameter Dependence of Leakage Current in Nanowire Junctionless Field Effect Transistors. IEEE Transactions on Electron Devices, 2017, 64, 1330-1335.	3.0	87
32	What is in Store in the January-February 2017 Issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2017, 34, 1-2.	3.2	0
33	1-T Capacitorless DRAM Using Bandgap-Engineered Silicon-Germanium Bipolar I-MOS. IEEE Transactions on Electron Devices, 2017, 64, 1583-1590.	3.0	24
34	Schottky bipolar I-MOS: An I-MOS with Schottky electrodes and an open-base BJT configuration for reduced operating voltage. Superlattices and Microstructures, 2017, 104, 422-427.	3.1	3
35	Nanotube Junctionless FET: Proposal, Design, and Investigation. IEEE Transactions on Electron Devices, 2017, 64, 1851-1856.	3.0	106
36	Symmetric Operation in an Extended Back Gate JLFET for Scaling to the 5-nm Regime Considering Quantum Confinement Effects. IEEE Transactions on Electron Devices, 2017, 64, 21-27.	3.0	42

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37	What is in Store in the Mayâ€“June 2017 issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2017, 34, 221-222.	3.2	0
38	A Tunnel Dielectric-Based Junctionless Transistor With Reduced Parasitic BJT Action. IEEE Transactions on Electron Devices, 2017, 64, 3470-3475.	3.0	16
39	Spacer Design Guidelines for Nanowire FETs From Gate-Induced Drain Leakage Perspective. IEEE Transactions on Electron Devices, 2017, 64, 3007-3015.	3.0	61
40	DC Drain Current Model for Tunnel FETs Considering Source and Drain Depletion Regions. , 2017, , .		2
41	Physical Insights Into the Nature of Gate-Induced Drain Leakage in Ultrashort Channel Nanowire FETs. IEEE Transactions on Electron Devices, 2017, 64, 2604-2610.	3.0	56
42	Comprehensive Analysis of Gate-Induced Drain Leakage in Emerging FET Architectures: Nanotube FETs Versus Nanowire FETs. IEEE Access, 2017, 5, 18918-18926.	4.2	36
43	What is in Store in the Marchâ€“April 2017 issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2017, 34, 111-112.	3.2	0
44	What is in Store in the Julyâ€“August 2017 Issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2017, 34, 341-342.	3.2	0
45	In_{0.53}Ga_{0.47}As/InP Trench-Gate Power MOSFET Based on Impact Ionization for Improved Performance: Design and Analysis. IEEE Transactions on Electron Devices, 2017, 64, 4561-4567.	3.0	7
46	The Charge Plasma n-p-n Impact Ionization MOS on FDSOI Technology: Proposal and Analysis. IEEE Transactions on Electron Devices, 2017, 64, 3-7.	3.0	21
47	A Planar Junctionless FET Using SiC With Reduced Impact of Interface Traps: Proposal and Analysis. IEEE Transactions on Electron Devices, 2017, 64, 4430-4434.	3.0	32
48	Thin Capacitively-Coupled Thyristor as an Ultrasensitive Label-Free Nanogap Biosensor: Proposal and Investigation. , 2017, 1, 1-4.		2
49	What is in Store in the September-October 2017 Issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2017, 34, 461-462.	3.2	0
50	Happiness and Technological Advances: Where are we heading?. IETE Technical Review (Institution of) Tj ETQq0 0 0 rgBT /Overlock 10 Tf	3.2	0
51	Schottky Barrier FET Biosensor for Dual Polarity Detection: A Simulation Study. IEEE Electron Device Letters, 2017, 38, 1594-1597.	3.9	9
52	Double gate symmetric tunnel FET: investigation and analysis. IET Circuits, Devices and Systems, 2017, 11, 365-370.	1.4	19
53	Induced dielectric modulated tunnel field effect transistor biosensor (I-DMTFET): Proposal and investigation. , 2017, , .		4
54	What is in Store in the November-December 2016 issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2016, 33, 571-572.	3.2	0

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55	A Novel Cascade-Free 5-V ESD Clamp Using I-MOS: Proposal and Analysis. IEEE Transactions on Device and Materials Reliability, 2016, 16, 200-207.	2.0	7
56	IETE Technical Reviewâ€" A Rising International Journal from India. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2016, 33, 91-92.	3.2	0
57	Modeling a Dual-Material-Gate Junctionless FET Under Full and Partial Depletion Conditions Using Finite-Differentiation Method. IEEE Transactions on Electron Devices, 2016, 63, 2282-2287.	3.0	13
58	Raised Source/Drain Dopingless Junctionless Accumulation Mode FET: Design and Analysis. IEEE Transactions on Electron Devices, 2016, 63, 4185-4190.	3.0	20
59	What is in Store in the Julyâ€"August issue of IETE Technical Review?. IETE Technical Review (Institution) Tj ETQq1 1 0.784314 rgBT /Ov	3.2	0
60	Dielectric-Modulated Field Effect Transistors for DNA Detection: Impact of DNA Orientation. IEEE Electron Device Letters, 2016, 37, 1485-1488.	3.9	44
61	2-D Threshold Voltage Model for the Double-Gate p-n-p-n TFET With Localized Charges. IEEE Transactions on Electron Devices, 2016, 63, 3663-3668.	3.0	22
62	Controlling L-BTBT and Volume Depletion in Nanowire JLFETs Using Coreâ€"Shell Architecture. IEEE Transactions on Electron Devices, 2016, 63, 3790-3794.	3.0	70
63	Insight into Lateral Band-to-Band-Tunneling in Nanowire Junctionless FETs. IEEE Transactions on Electron Devices, 2016, 63, 4138-4142.	3.0	90
64	A Novel Gate-Stack-Engineered Nanowire FET for Scaling to the Sub-10-nm Regime. IEEE Transactions on Electron Devices, 2016, 63, 5055-5059.	3.0	50
65	What is in Store in the Mayâ€"June issue of IETE Technical Review?. IETE Technical Review (Institution of) Tj ETQq1 1 0.784314 rgBT /Ov	3.2	0
66	What is in Store in the Septemberâ€"October 2016 Issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2016, 33, 453-454.	3.2	0
67	Controlling BTBT-Induced Parasitic BJT Action in Junctionless FETs Using a Hybrid Channel. IEEE Transactions on Electron Devices, 2016, 63, 3350-3353.	3.0	65
68	Realizing Efficient Volume Depletion in SOI Junctionless FETs. IEEE Journal of the Electron Devices Society, 2016, 4, 110-115.	2.1	75
69	Schottky Biristor: A Metal-Semiconductorâ€"Metal Bistable Resistor. IEEE Transactions on Electron Devices, 2015, 62, 2360-2363.	3.0	16
70	Global University Rankings: What should India do?. IETE Technical Review (Institution of Electronics) Tj ETQq0 0 0 rgBT /Overlock 10 Tf 5	3.2	2
71	A pseudo 2-D surface potential model of a dual material double gate junctionless field effect transistor. Journal of Computational Electronics, 2015, 14, 686-693.	2.5	14
72	Innovation and Technology should Lead to Abundance not Scarcity. IETE Technical Review (Institution) Tj ETQq0 0 0 rgBT /Overlock 10 T	3.2	12

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73	A Compact Analytical Model for the drain current of a TFET with non-abrupt doping profile incorporating the effect of band-gap narrowing. , 2015, , .		1
74	Two dimensional analytical model for the threshold voltage of a Gate All Around Nanowire tunneling FET with localized charges. , 2015, , .		2
75	A Compact Analytical Model for the Drain Current of Gate-All-Around Nanowire Tunnel FET Accurate From Sub-Threshold to ON-State. IEEE Nanotechnology Magazine, 2015, 14, 358-362.	2.0	30
76	Vertical Bipolar Charge Plasma Transistor with Buried Metal Layer. Scientific Reports, 2015, 5, 7860.	3.3	37
77	A full-range dual material gate tunnel field effect transistor drain current model considering both source and drain depletion region band-to-band tunneling. Journal of Computational Electronics, 2015, 14, 280-287.	2.5	34
78	An Accurate Compact Analytical Model for the Drain Current of a TFET From Subthreshold to Strong Inversion. IEEE Transactions on Electron Devices, 2015, 62, 478-484.	3.0	40
79	PNPN tunnel FET with controllable drain side tunnel barrier width: Proposal and analysis. Superlattices and Microstructures, 2015, 86, 121-125.	3.1	36
80	Dielectric modulated overlapping gate-on-drain tunnel-FET as a label-free biosensor. Superlattices and Microstructures, 2015, 86, 198-202.	3.1	89
81	Junctionless Biristor: A Bistable Resistor Without Chemically Doped P-N Junctions. IEEE Journal of the Electron Devices Society, 2015, 3, 311-315.	2.1	17
82	Investigation of laterally single-diffused metal oxide semiconductor (LSMOS) field effect transistor. Current Applied Physics, 2015, 15, 1130-1133.	2.4	12
83	Charge-Modulated Underlap I-MOS Transistor as a Label-Free Biosensor: A Simulation Study. IEEE Transactions on Electron Devices, 2015, 62, 2645-2651.	3.0	43
84	A Silicon Biristor With Reduced Operating Voltage: Proposal and Analysis. IEEE Journal of the Electron Devices Society, 2015, 3, 67-72.	2.1	19
85	The Pay or Perish Game: Why we should stand up against â€˜active discriminationâ€™ for the survival of net neutrality. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2015, 32, 161-163.	3.2	0
86	Controlling the Drain Side Tunneling Width to Reduce Ambipolar Current in Tunnel FETs Using Heterodielectric BOX. IEEE Transactions on Electron Devices, 2015, 62, 3882-3886.	3.0	123
87	Bipolar I-MOSâ€"An Impact-Ionization MOS With Reduced Operating Voltage Using the Open-Base BJT Configuration. IEEE Transactions on Electron Devices, 2015, 62, 4345-4348.	3.0	29
88	Call Drops in Mobile Wireless Networks: Calling your attention. IETE Technical Review (Institution of) Tj ETQq0 0 0 rgBT /Overlock 10 Tf	3.2	0
89	Smart Cities with Massive Data Centric Living are Hard to Build Without 5G Networks. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2015, 32, 237-239.	3.2	4
90	GaAs Tunnel Diode With Electrostatically Doped n-Region: Proposal and Analysis. IEEE Transactions on Electron Devices, 2015, 62, 3445-3448.	3.0	9

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91	Controlling Ambipolar Current in Tunneling FETs Using Overlapping Gate-on-Drain. IEEE Journal of the Electron Devices Society, 2014, 2, 187-190.	2.1	271
92	Facing the Students on Facebook: Are You Game for It?. IETE Technical Review (Institution of) Tj ETQq0 0 0 rgBT /Overlock 10 Tf 50 702	3.2	1
93	A Drain-side Gate-underlap I-MOS (DGI-MOS) transistor as a label-free biosensor for detection of charged biomolecules. , 2014, , .		2
94	Numerical study of the threshold voltage of TFETs with localized charges. , 2014, , .		1
95	Drain current model for SOI TFET considering source and drain side tunneling. , 2014, , .		6
96	Expanding the Boundaries of Your Research Using Social Media: Stand-Up and Be Counted. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2014, 31, 255-257.	3.2	8
97	Telling Lies to Describe Truth: Do we Emphasize the Importance of â€œThe Art of Approximationsâ€• to the Students?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2014, 31, 1-3.	3.2	1
98	Quantum Computing in India: An Opportunity that Should Not Be Missed. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2014, 31, 187-189.	3.2	0
99	Compact Analytical Model of Dual Material Gate Tunneling Field-Effect Transistor Using Interband Tunneling and Channel Transport. IEEE Transactions on Electron Devices, 2014, 61, 1936-1942.	3.0	102
100	Controlling the ON-resistance in SOI LDMOS using parasitic bipolar junction transistor. Journal of Computational Electronics, 2014, 13, 857-861.	2.5	2
101	Compact Analytical Drain Current Model of Gate-All-Around Nanowire Tunneling FET. IEEE Transactions on Electron Devices, 2014, 61, 2599-2603.	3.0	93
102	A Pseudo-2-D-Analytical Model of Dual Material Gate All-Around Nanowire Tunneling FET. IEEE Transactions on Electron Devices, 2014, 61, 2264-2270.	3.0	64
103	In-Built N⁺ Pocket p-n-p-n Tunnel Field-Effect Transistor. IEEE Electron Device Letters, 2014, 35, 1170-1172.	3.9	131
104	2-D Analytical Model for the Threshold Voltage of a Tunneling FET With Localized Charges. IEEE Transactions on Electron Devices, 2014, 61, 3054-3059.	3.0	43
105	Junctionless Impact Ionization MOS: Proposal and Investigation. IEEE Transactions on Electron Devices, 2014, 61, 4295-4298.	3.0	58
106	Thin-Film Bipolar Transistors on Recrystallized Polycrystalline Silicon Without Impurity Doped Junctions: Proposal and Investigation. Journal of Display Technology, 2014, 10, 590-594.	1.2	35
107	Impact of gate leakage considerations in tunnel field effect transistor design. Japanese Journal of Applied Physics, 2014, 53, 074201.	1.5	24
108	We are Expanding the Editorial Board. IETE Technical Review (Institution of Electronics and) Tj ETQq0 0 0 rgBT /Overlock 10 Tf 50 62 Td	3.2	0

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109	A dc model for partially depleted SOI laterally diffused MOSFETs utilizing the HiSIM-HV compact model. Journal of Computational Electronics, 2013, 12, 460-468.	2.5	2
110	Doping-Less Tunnel Field Effect Transistor: Design and Investigation. IEEE Transactions on Electron Devices, 2013, 60, 3285-3290.	3.0	521
111	Dielectric-Modulated Impact-Ionization MOS Transistor as a Label-Free Biosensor. IEEE Electron Device Letters, 2013, 34, 1575-1577.	3.9	112
112	Face Recognition by Machines: Is It an Effective Surveillance Tactic?. IETE Technical Review (Institution) Tj ETQq0 0 0 rgBT /Overlock 10 T	3.2	3
113	Kudos to our reviewers. IETE Technical Review (Institution of Electronics and Telecommunication) Tj ETQq1 1 0.784314 rgBT /Overloc	3.2	0
114	How does the power of "Suggestion" influence studentsâ€² performance?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2013, 30, 273.	3.2	0
115	Making Your Research Paper Discoverable: Title Plays the Winning Trick. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2013, 30, 361.	3.2	7
116	Schottky Collector Bipolar Transistor Without Impurity Doped Emitter and Base: Design and Performance. IEEE Transactions on Electron Devices, 2013, 60, 2956-2959.	3.0	49
117	The Malady of Technology in Our Lives: Is Anyone Listening?. IETE Technical Review (Institution of) Tj ETQq1 1 0.784314 rgBT /Overlock	3.2	3
118	Back to Basics: Why Every Student and Professor Should Ride a Bicycle on a University Campus?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2013, 30, 165.	3.2	0
119	Modeling of Partially Depleted SOI DEMOSFETs with a Sub-circuit Utilizing the HiSIM-HV Compact Model. , 2012, , .		0
120	Improving the breakdown voltage, ON-resistance and gate-charge of InGaAs LDMOS power transistors. Semiconductor Science and Technology, 2012, 27, 105030.	2.0	28
121	Controlled deposition of aligned carbon nanotubes by floating electrodes dielectrophoresis. , 2012, , .		1
122	Honestly speaking about academic dishonesty. IETE Technical Review (Institution of Electronics and) Tj ETQq0 0 0 rgBT /Overlock 10 Tf 5	3.2	4
123	Literal and Intelligent Plagiarism: Students Beware!. IETE Technical Review (Institution of Electronics) Tj ETQq1 1 0.784314 rgBT /Over	3.2	1
124	Polysilicon Spacer Gate Technique to Reduce Gate Charge of a Trench Power MOSFET. IEEE Transactions on Electron Devices, 2012, 59, 738-744.	3.0	27
125	Bipolar Charge-Plasma Transistor: A Novel Three Terminal Device. IEEE Transactions on Electron Devices, 2012, 59, 962-967.	3.0	197
126	An academicianâ€²s reminiscences on giving interesting and effective public lectures. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2012, 29, 435.	3.2	0

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127	A novel Doping-less Bipolar Transistor with Schottky Collector. , 2011, , .		7
128	Novel Attributes of a Dual Material Gate Nanoscale Tunnel Field-Effect Transistor. IEEE Transactions on Electron Devices, 2011, 58, 404-410.	3.0	392
129	Compact Modeling of Partially Depleted Silicon-on-Insulator Drain-Extended MOSFET (DEMOSFET) Including High-Voltage and Floating-Body Effects. IEEE Transactions on Electron Devices, 2011, 58, 3485-3493.	3.0	7
130	Reflections on Teaching a Large Class. IETE Technical Review (Institution of Electronics and) Tj ETQq0 0 0 rgBT /Overlock 10 Tf 50 622 T	3.2	0
131	Guest Editorial Special Issue on Light-Emitting Diodes. IEEE Transactions on Electron Devices, 2010, 57, 7-11.	3.0	4
132	Extended-$hbox{p}^{+}$ Stepped Gate LDMOS for Improved Performance. IEEE Transactions on Electron Devices, 2010, 57, 1719-1724.	3.0	69
133	Estimation and Compensation of Process-Induced Variations in Nanoscale Tunnel Field-Effect Transistors for Improved Reliability. IEEE Transactions on Device and Materials Reliability, 2010, 10, 390-395.	2.0	64
134	Guidelines for Theme-based Special Issues. IETE Technical Review (Institution of Electronics and) Tj ETQq0 0 0 rgBT /Overlock 10 Tf 50 4	3.2	0
135	Linearity and speed optimization in SOI LDMOS using gate engineering. Semiconductor Science and Technology, 2010, 25, 015006.	2.0	16
136	A New Hetero-material Stepped Gate (HSG) SOI LDMOS for RF Power Amplifier Applications. , 2010, , .		9
137	Dual-Material-Gate Technique for Enhanced Transconductance and Breakdown Voltage of Trench Power MOSFETs. IEEE Transactions on Electron Devices, 2009, 56, 517-522.	3.0	38
138	A Stepped Oxide Hetero-Material Gate Trench Power MOSFET for Improved Performance. IEEE Transactions on Electron Devices, 2009, 56, 1355-1359.	3.0	41
139	Recessed source concept in nanoscale vertical surrounding gate (VSG) MOSFETs for controlling short-channel effects. Physica E: Low-Dimensional Systems and Nanostructures, 2009, 41, 671-676.	2.7	13
140	A New Buried-Oxide-In-Drift-Region Trench MOSFET With Improved Breakdown Voltage. IEEE Electron Device Letters, 2009, 30, 990-992.	3.9	10
141	Memristor - Why Do We Have to Know About It?. IETE Technical Review (Institution of Electronics and) Tj ETQq1 1 0.784314 rgBT /Ov	3.2	15
142	Impact of Strain on Drain Current and Threshold Voltage of Nanoscale Double Gate Tunnel Field Effect Transistor: Theoretical Investigation and Analysis. Japanese Journal of Applied Physics, 2009, 48, 064503.	1.5	124
143	Evaluating Scientists: Citations, Impact Factor, h-Index, Online Page Hits and What Else?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2009, 26, 165.	3.2	14
144	Writing Skills and Review Articles: "Walking the Path from Idea to Print". IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2009, 26, 225.	3.2	0

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145	Spam Email: The Unwanted Guest at Your Doorstep!. IETE Technical Review (Institution of Electronics) Tj ETQq1 1 0.784314 rgBT /Ov	3.2	0
146	Analytical drain current model for nanoscale strainedâ€Si/SiGe MOSFETs. COMPEL - the International Journal for Computation and Mathematics in Electrical and Electronic Engineering, 2009, 28, 353-371.	0.9	22
147	A new SiGe Stepped Gate (SSG) thin film SOI LDMOS for enhanced breakdown voltage and reduced delay. , 2009, , .		2
148	Effect of the Ge mole fraction on the formation of a conduction path in cylindrical strained-silicon-on-SiGe MOSFETs. Superlattices and Microstructures, 2008, 44, 79-85.	3.1	25
149	Compact Surface Potential Model for FD SOI MOSFET Considering Substrate Depletion Region. IEEE Transactions on Electron Devices, 2008, 55, 789-795.	3.0	22
150	A New Strained-Silicon Channel Trench-Gate Power MOSFET: Design and Analysis. IEEE Transactions on Electron Devices, 2008, 55, 3299-3304.	3.0	20
151	Special Issue on Nanowire Transistors: Modeling, Device Design, and Technology. IEEE Transactions on Electron Devices, 2008, 55, 2813-2819.	3.0	6
152	The Ground Plane in Buried Oxide for Controlling Short-Channel Effects in Nanoscale SOI MOSFETs. IEEE Transactions on Electron Devices, 2008, 55, 1554-1557.	3.0	49
153	Guest Editorial Special Issue on Nanowire Transistors: Modeling, Device Design, and Technology. IEEE Nanotechnology Magazine, 2008, 7, 643-650.	2.0	4
154	Being Wary of Plagiarism. IETE Technical Review (Institution of Electronics and Telecommunication) Tj ETQq0 0 0 rgBT /Overlock 10 Tf 5	3.2	3
155	QUANTUM CONFINEMENT EFFECTS IN STRAINED SILICON MOSFETS. International Journal of Nanoscience, 2008, 07, 81-84.	0.7	31
156	Transition to Online System and Thoughts on Peer Review Process. IETE Technical Review (Institution) Tj ETQq0 0 0 rgBT /Overlock 10 Tf	3.2	0
157	Molecular Diodes and Applications. Recent Patents on Nanotechnology, 2007, 1, 51-57.	1.3	23
158	Analytical Drain Current Model of Nanoscale Strained-Si/SiGe MOSFETs for Analog Circuit Simulation. , 2007, , .		7
159	Impact of Strain or Ge Content on the Threshold Voltage of Nanoscale Strained-Si/SiGe Bulk MOSFETs. IEEE Transactions on Device and Materials Reliability, 2007, 7, 181-187.	2.0	46
160	Approaches to nanoscale MOSFET compact modeling using surface potential based models. , 2007, , .		2
161	Compact Analytical Threshold-Voltage Model of Nanoscale Fully Depleted Strained-Si on Siliconâ€“Germanium-on-Insu lator (SGOI) MOSFETs. IEEE Transactions on Electron Devices, 2007, 54, 554-562.	3.0	57
162	Comprehensive approach to modeling threshold voltage ofÂnanoscale strained silicon SOI MOSFETs. Journal of Computational Electronics, 2007, 6, 439-444.	2.5	14

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