M Jagadesh Kumar

List of Publications by Year
in descending order

234 papers	6,806 citations	76326 40 h-index	76900 74 g-index
250 all docs	250 docs citations	250 times ranked	1957 citing authors

#	Article	IF	Citations
1	Doping-Less Tunnel Field Effect Transistor: Design and Investigation. IEEE Transactions on Electron Devices, 2013, 60, 3285-3290.	3.0	521
2	Novel Attributes of a Dual Material Gate Nanoscale Tunnel Field-Effect Transistor. IEEE Transactions on Electron Devices, 2011, 58, 404-410.	3.0	392
3	Controlling Short-Channel Effects in Deep-Submicron SOI MOSFETs for Improved Reliability: A Review. IEEE Transactions on Device and Materials Reliability, 2004, 4, 99-109.	2.0	363
4	Controlling Ambipolar Current in Tunneling FETs Using Overlapping Gate-on-Drain. IEEE Journal of the Electron Devices Society, 2014, 2, 187-190.	2.1	271
5	Two-Dimensional Analytical Modeling of Fully Depleted DMG SOI MOSFET and Evidence for Diminished SCEs. IEEE Transactions on Electron Devices, 2004, 51, 569-574.	3.0	249
6	A New Dual-Material Double-Gate (DMDG) Nanoscale SOI MOSFETâ€"Two-Dimensional Analytical Modeling and Simulation. IEEE Nanotechnology Magazine, 2005, 4, 260-268.	2.0	202
7	Bipolar Charge-Plasma Transistor: A Novel Three Terminal Device. IEEE Transactions on Electron Devices, 2012, 59, 962-967.	3.0	197
8	In-Built N⁺ Pocket p-n-p-n Tunnel Field-Effect Transistor. IEEE Electron Device Letters, 2014, 35, 1170-1172.	3.9	131
9	Investigation of the Novel Attributes of a Fully Depleted Dual-Material Gate SOI MOSFET. IEEE Transactions on Electron Devices, 2004, 51, 1463-1467.	3.0	127
10	Impact of Strain on Drain Current and Threshold Voltage of Nanoscale Double Gate Tunnel Field Effect Transistor: Theoretical Investigation and Analysis. Japanese Journal of Applied Physics, 2009, 48, 064503.	1.5	124
11	Controlling the Drain Side Tunneling Width to Reduce Ambipolar Current in Tunnel FETs Using Heterodielectric BOX. IEEE Transactions on Electron Devices, 2015, 62, 3882-3886.	3.0	123
12	Dielectric-Modulated Impact-Ionization MOS Transistor as a Label-Free Biosensor. IEEE Electron Device Letters, 2013, 34, 1575-1577.	3.9	112
13	Nanotube Junctionless FET: Proposal, Design, and Investigation. IEEE Transactions on Electron Devices, 2017, 64, 1851-1856.	3.0	106
14	Compact Analytical Model of Dual Material Gate Tunneling Field-Effect Transistor Using Interband Tunneling and Channel Transport. IEEE Transactions on Electron Devices, 2014, 61, 1936-1942.	3.0	102
15	Compact Analytical Drain Current Model of Gate-All-Around Nanowire Tunneling FET. IEEE Transactions on Electron Devices, 2014, 61, 2599-2603.	3.0	93
16	Insight into Lateral Band-to-Band-Tunneling in Nanowire Junctionless FETs. IEEE Transactions on Electron Devices, 2016, 63, 4138-4142.	3.0	90
17	Dielectric modulated overlapping gate-on-drain tunnel-FET as a label-free biosensor. Superlattices and Microstructures, 2015, 86, 198-202.	3.1	89
18	Diameter Dependence of Leakage Current in Nanowire Junctionless Field Effect Transistors. IEEE Transactions on Electron Devices, 2017, 64, 1330-1335.	3.0	87

#	Article	IF	Citations
19	Realizing Efficient Volume Depletion in SOI Junctionless FETs. IEEE Journal of the Electron Devices Society, 2016, 4, 110-115.	2.1	75
20	New dual-material SG nanoscale MOSFET: analytical threshold-voltage model. IEEE Transactions on Electron Devices, 2006, 53, 920-922.	3.0	74
21	Controlling L-BTBT and Volume Depletion in Nanowire JLFETs Using Coreâ€“Shell Architecture. IEEE Transactions on Electron Devices, 2016, 63, 3790-3794.	3.0	70
22	Extended-$hbox{p}^{+}$ Stepped Gate LDMOS for Improved Performance. IEEE Transactions on Electron Devices, 2010, 57, 1719-1724.	3.0	69
23	Controlling BTBT-Induced Parasitic BJT Action in Junctionless FETs Using a Hybrid Channel. IEEE Transactions on Electron Devices, 2016, 63, 3350-3353.	3.0	65
24	Estimation and Compensation of Process-Induced Variations in Nanoscale Tunnel Field-Effect Transistors for Improved Reliability. IEEE Transactions on Device and Materials Reliability, 2010, 10, 390-395.	2.0	64
25	A Pseudo-2-D-Analytical Model of Dual Material Gate All-Around Nanowire Tunneling FET. IEEE Transactions on Electron Devices, 2014, 61, 2264-2270.	3.0	64
26	Spacer Design Guidelines for Nanowire FETs From Gate-Induced Drain Leakage Perspective. IEEE Transactions on Electron Devices, 2017, 64, 3007-3015.	3.0	61
27	Two-Dimensional Analytical Threshold Voltage Model of Nanoscale Fully Depleted SOI MOSFET With Electrically Induced S/D Extensions. IEEE Transactions on Electron Devices, 2005, 52, 1568-1575.	3.0	58
28	Junctionless Impact Ionization MOS: Proposal and Investigation. IEEE Transactions on Electron Devices, 2014, 61, 4295-4298.	3.0	58
29	Compact Analytical Threshold-Voltage Model of Nanoscale Fully Depleted Strained-Si on Siliconâ€“Germanium-on-Insu lator (SGOI) MOSFETs. IEEE Transactions on Electron Devices, 2007, 54, 554-562.	3.0	57
30	Physical Insights Into the Nature of Gate-Induced Drain Leakage in Ultrashort Channel Nanowire FETs. IEEE Transactions on Electron Devices, 2017, 64, 2604-2610.	3.0	56
31	New buried P+-grid polysilicon emitter bipolar power transistor. Solid-State Electronics, 1995, 38, 1854-1856.	1.4	51
32	A Novel Gate-Stack-Engineered Nanowire FET for Scaling to the Sub-10-nm Regime. IEEE Transactions on Electron Devices, 2016, 63, 5055-5059.	3.0	50
33	The Ground Plane in Buried Oxide for Controlling Short-Channel Effects in Nanoscale SOI MOSFETs. IEEE Transactions on Electron Devices, 2008, 55, 1554-1557.	3.0	49
34	Schottky Collector Bipolar Transistor Without Impurity Doped Emitter and Base: Design and Performance. IEEE Transactions on Electron Devices, 2013, 60, 2956-2959.	3.0	49
35	Nanotube Tunneling FET With a Core Source for Ultrasteep Subthreshold Swing: A Simulation Study. IEEE Transactions on Electron Devices, 2019, 66, 4425-4432.	3.0	49
36	Investigation of the novel attributes of a single-halo double gate SOI MOSFET: 2D simulation study. Microelectronics Journal, 2004, 35, 761-765.	2.0	48

#	Article	IF	Citations
37	A simple analytical threshold voltage model of nanoscale single-layer fully depleted strained-silicon-on-insulator MOSFETs. IEEE Transactions on Electron Devices, 2006, 53, 2500-2506.	3.0	47
38	Impact of Strain or Ge Content on the Threshold Voltage of Nanoscale Strained-Si/SiGe Bulk MOSFETs. IEEE Transactions on Device and Materials Reliability, 2007, 7, 181-187.	2.0	46
39	Dielectric-Modulated Field Effect Transistors for DNA Detection: Impact of DNA Orientation. IEEE Electron Device Letters, 2016, 37, 1485-1488.	3.9	44
40	2-D Analytical Model for the Threshold Voltage of a Tunneling FET With Localized Charges. IEEE Transactions on Electron Devices, 2014, 61, 3054-3059.	3.0	43
41	Charge-Modulated Underlap I-MOS Transistor as a Label-Free Biosensor: A Simulation Study. IEEE Transactions on Electron Devices, 2015, 62, 2645-2651.	3.0	43
42	Symmetric Operation in an Extended Back Gate JLFET for Scaling to the 5-nm Regime Considering Quantum Confinement Effects. IEEE Transactions on Electron Devices, 2017, 64, 21-27.	3.0	42
43	A Line Tunneling Field-Effect Transistor Based on Misaligned Coreâ€“Shell Gate Architecture in Emerging Nanotube FETs. IEEE Transactions on Electron Devices, 2019, 66, 2809-2816.	3.0	42
44	A Stepped Oxide Hetero-Material Gate Trench Power MOSFET for Improved Performance. IEEE Transactions on Electron Devices, 2009, 56, 1355-1359.	3.0	41
45	An Accurate Compact Analytical Model for the Drain Current of a TFET From Subthreshold to Strong Inversion. IEEE Transactions on Electron Devices, 2015, 62, 478-484.	3.0	40
46	Profile design considerations for minimizing base transit time in SiGe HBT's. IEEE Transactions on Electron Devices, 1998, 45, 1725-1731.	3.0	39
47	Compact modeling of the effects of parasitic internal fringe capacitance on the threshold voltage of high-k gate-dielectric nanoscale SOI MOSFETs. IEEE Transactions on Electron Devices, 2006, 53, 706-711.	3.0	39
48	Controlling L-BTBT in Emerging Nanotube FETs Using Dual-Material Gate. IEEE Journal of the Electron Devices Society, 2018, 6, 611-621.	2.1	39
49	Dual-Material-Gate Technique for Enhanced Transconductance and Breakdown Voltage of Trench Power MOSFETs. IEEE Transactions on Electron Devices, 2009, 56, 517-522.	3.0	38
50	Investigation of a new modified source/drain for diminished self-heating effects in nanoscale MOSFETs using computer simulation. Physica E: Low-Dimensional Systems and Nanostructures, 2006, 33, 134-138.	2.7	37
51	Vertical Bipolar Charge Plasma Transistor with Buried Metal Layer. Scientific Reports, 2015, 5, 7860.	3.3	37
52	Leakage Current Reduction Techniques in Poly-Si TFTs for Active Matrix Liquid Crystal Displays: A Comprehensive Study. IEEE Transactions on Device and Materials Reliability, 2006, 6, 315-325.	2.0	36
53	PNPN tunnel FET with controllable drain side tunnel barrier width: Proposal and analysis. Superlattices and Microstructures, 2015, 86, 121-125.	3.1	36
54	Comprehensive Analysis of Gate-Induced Drain Leakage in Emerging FET Architectures: Nanotube FETs Versus Nanowire FETs. IEEE Access, 2017, 5, 18918-18926.	4.2	36

#	Article	IF	Citations
55	Thin-Film Bipolar Transistors on Recrystallized Polycrystalline Silicon Without Impurity Doped Junctions: Proposal and Investigation. Journal of Display Technology, 2014, 10, 590-594.	1.2	35
56	A full-range dual material gate tunnel field effect transistor drain current model considering both source and drain depletion region band-to-band tunneling. Journal of Computational Electronics, 2015, 14, 280-287.	2.5	34
57	A Planar Junctionless FET Using SiC With Reduced Impact of Interface Traps: Proposal and Analysis. IEEE Transactions on Electron Devices, 2017, 64, 4430-4434.	3.0	32
58	Shielded channel double-gate MOSFET: a novel device for reliable nanoscale CMOS applications. IEEE Transactions on Device and Materials Reliability, 2005, 5, 509-514.	2.0	31
59	QUANTUM CONFINEMENT EFFECTS IN STRAINED SILICON MOSFETS. International Journal of Nanoscience, 2008, 07, 81-84.	0.7	31
60	A Compact Analytical Model for the Drain Current of Gate-All-Around Nanowire Tunnel FET Accurate From Sub-Threshold to ON-State. IEEE Nanotechnology Magazine, 2015, 14, 358-362.	2.0	30
61	Bipolar I-MOSâ€"An Impact-Ionization MOS With Reduced Operating Voltage Using the Open-Base BJT Configuration. IEEE Transactions on Electron Devices, 2015, 62, 4345-4348.	3.0	29
62	Improving the breakdown voltage, ON-resistance and gate-charge of InGaAs LDMOS power transistors. Semiconductor Science and Technology, 2012, 27, 105030.	2.0	28
63	Polysilicon Spacer Gate Technique to Reduce Gate Charge of a Trench Power MOSFET. IEEE Transactions on Electron Devices, 2012, 59, 738-744.	3.0	27
64	Reconfigurable FET Biosensor for a Wide Detection Range and Electrostatically Tunable Sensing Response. IEEE Sensors Journal, 2020, 20, 2261-2269.	4.7	27
65	Collector design tradeoffs for low voltage applications of advanced bipolar transistors. IEEE Transactions on Electron Devices, 1993, 40, 1478-1483.	3.0	25
66	A new 4H-SiC lateral merged double Schottky (LMDS) rectifier with excellent forward and reverse characteristics. IEEE Transactions on Electron Devices, 2001, 48, 2695-2700.	3.0	25
67	Effect of the Ge mole fraction on the formation of a conduction path in cylindrical strained-silicon-on-SiGe MOSFETs. Superlattices and Microstructures, 2008, 44, 79-85.	3.1	25
68	Surface Accumulation Layer Transistor (SALTran): A New Bipolar Transistor for Enhanced Current Gain and Reduced Hot-Carrier Degradation. IEEE Transactions on Device and Materials Reliability, 2004, 4, 509-515.	2.0	24
69	Impact of gate leakage considerations in tunnel field effect transistor design. Japanese Journal of Applied Physics, 2014, 53, 074201.	1.5	24
70	1-T Capacitorless DRAM Using Bandgap-Engineered Silicon-Germanium Bipolar I-MOS. IEEE Transactions on Electron Devices, 2017, 64, 1583-1590.	3.0	24
71	Molecular Diodes and Applications. Recent Patents on Nanotechnology, 2007, 1, 51-57.	1.3	23
72	Nanoscale SOI MOSFETs with electrically induced source/drain extension: Novel attributes and design considerations for suppressed short-channel effects. Superlattices and Microstructures, 2006, 39, 395-405.	3.1	22

#	Article	IF	Citations
73	Compact Surface Potential Model for FD SOI MOSFET Considering Substrate Depletion Region. IEEE Transactions on Electron Devices, 2008, 55, 789-795.	3.0	22
74	Analytical drain current model for nanoscale strainedâ€Si/SiGe MOSFETs. COMPEL - the International Journal for Computation and Mathematics in Electrical and Electronic Engineering, 2009, 28, 353-371.	0.9	22
75	2-D Threshold Voltage Model for the Double-Gate p-n-p-n TFET With Localized Charges. IEEE Transactions on Electron Devices, 2016, 63, 3663-3668.	3.0	22
76	The Charge Plasma n-p-n Impact Ionization MOS on FDSOI Technology: Proposal and Analysis. IEEE Transactions on Electron Devices, 2017, 64, 3-7.	3.0	21
77	Realizing a Planar 4H-SiC Junctionless FET for Sub-10-nm Regime Using P⁺ Pocket. IEEE Transactions on Electron Devices, 2019, 66, 3209-3214.	3.0	21
78	A New Strained-Silicon Channel Trench-Gate Power MOSFET: Design and Analysis. IEEE Transactions on Electron Devices, 2008, 55, 3299-3304.	3.0	20
79	Raised Source/Drain Dopingless Junctionless Accumulation Mode FET: Design and Analysis. IEEE Transactions on Electron Devices, 2016, 63, 4185-4190.	3.0	20
80	Diminished Short Channel Effects in Nanoscale Double-Gate Silicon-on-Insulator Metalâ€“Oxideâ€“Semiconductor Field-Effect-Transistors due to Induced Back-Gate Step Potential. Japanese Journal of Applied Physics, 2005, 44, 6508-6509.	1.5	19
81	A Silicon Biristor With Reduced Operating Voltage: Proposal and Analysis. IEEE Journal of the Electron Devices Society, 2015, 3, 67-72.	2.1	19
82	Double gate symmetric tunnel FET: investigation and analysis. IET Circuits, Devices and Systems, 2017, 11, 365-370.	1.4	19
83	The effects of collector lifetime on the characteristics of high-voltage power transistors operating in the quasi-saturation region. IEEE Transactions on Electron Devices, 1987, 34, 1163-1169.	3.0	17
84	Elimination of bipolar induced drain breakdown and single transistor latch in submicron PD SOI MOSFET. IEEE Transactions on Reliability, 2002, 51, 367-370.	4.6	17
85	A new symmetrical double gate nanoscale MOSFET with asymmetrical side gates for electrically induced source/drain. Microelectronic Engineering, 2006, 83, 409-414.	2.4	17
86	Junctionless Biristor: A Bistable Resistor Without Chemically Doped P-N Junctions. IEEE Journal of the Electron Devices Society, 2015, 3, 311-315.	2.1	17
87	Linearity and speed optimization in SOI LDMOS using gate engineering. Semiconductor Science and Technology, 2010, 25, 015006.	2.0	16
88	Schottky Biristor: A Metal-Semiconductorâ€“Metal Bistable Resistor. IEEE Transactions on Electron Devices, 2015, 62, 2360-2363.	3.0	16
89	A Tunnel Dielectric-Based Junctionless Transistor With Reduced Parasitic BJT Action. IEEE Transactions on Electron Devices, 2017, 64, 3470-3475.	3.0	16
90	An Impact Ionization MOSFET With Reduced Breakdown Voltage Based on Back-Gate Misalignment. IEEE Transactions on Electron Devices, 2019, 66, 868-875.	3.0	16

#	Article	IF	Citations
91	Evidence for suppressed short-channel effects in deep submicron dual-material gate (DMG) partially depleted SOI MOSFETs â€“ A two-dimensional analytical approach. Microelectronic Engineering, 2004, 75, 367-374.	2.4	15
92	A super beta bipolar transistor using SiGe-base surface accumulation layer transistor(SALTran) concept: a simulation study. IEEE Transactions on Electron Devices, 2006, 53, 577-579.	3.0	15
93	Memristor - Why Do We Have to Know About It?. IETE Technical Review (Institution of Electronics and) Tj ETQq1 1 0.784314 rgBT /Over	3.2	15
94	On the iterative schemes to obtain base doping profiles for reducing base transit time in a bipolar transistor. IEEE Transactions on Electron Devices, 2001, 48, 1222-1224.	3.0	14
95	A new lateral PNM Schottky collector bipolar transistor (SCBT) on SOI for nonsaturating VLSI logic design. IEEE Transactions on Electron Devices, 2002, 49, 1070-1072.	3.0	14
96	Comprehensive approach to modeling threshold voltage ofÂnanoscale strained silicon SOI MOSFETs. Journal of Computational Electronics, 2007, 6, 439-444.	2.5	14
97	Evaluating Scientists: Citations, Impact Factor, h-Index, Online Page Hits and What Else?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2009, 26, 165.	3.2	14
98	A pseudo 2-D surface potential model of a dual material double gate junctionless field effect transistor. Journal of Computational Electronics, 2015, 14, 686-693.	2.5	14
99	Investigation of the Scalability of Emerging Nanotube Junctionless FETs Using an Intrinsic Pocket. IEEE Journal of the Electron Devices Society, 2019, 7, 888-896.	2.1	14
100	Novel Ge-profile design for high-speed SiGe HBTs: modelling and analysis. IET Circuits, Devices and Systems, 1999, 146, 291.	0.6	13
101	Study of the extended p/sup +/ dual source structure for eliminating bipolar induced breakdown in submicron SOI MOSFET's. IEEE Transactions on Electron Devices, 2000, 47, 1678-1680.	3.0	13
102	A New Poly-Si TG-TFT With Diminished Pseudosubthreshold Region: Theoretical Investigation and Analysis. IEEE Transactions on Electron Devices, 2005, 52, 1815-1820.	3.0	13
103	A New High Breakdown Voltage Lateral Schottky Collector Bipolar Transistor on SOI: Design and Analysis. IEEE Transactions on Electron Devices, 2005, 52, 2496-2501.	3.0	13
104	Recessed source concept in nanoscale vertical surrounding gate (VSG) MOSFETs for controlling short-channel effects. Physica E: Low-Dimensional Systems and Nanostructures, 2009, 41, 671-676.	2.7	13
105	Modeling a Dual-Material-Gate Junctionless FET Under Full and Partial Depletion Conditions Using Finite-Differentiation Method. IEEE Transactions on Electron Devices, 2016, 63, 2282-2287.	3.0	13
106	Innovation and Technology should Lead to Abundance not Scarcity. IETE Technical Review (Institution) Tj ETQq0 0 0 rgBT /Overlock 10 T	3.2	12
107	Investigation of laterally single-diffused metal oxide semiconductor (LSMOS) field effect transistor. Current Applied Physics, 2015, 15, 1130-1133.	2.4	12
108	Sub-10 nm Scalability of Junctionless FETs Using a Ground Plane in High-K BOX: A Simulation Study. IEEE Access, 2020, 8, 137540-137548.	4.2	11

#	Article	IF	Citations
109	A New Buried-Oxide-In-Drift-Region Trench MOSFET With Improved Breakdown Voltage. IEEE Electron Device Letters, 2009, 30, 990-992.	3.9	10
110	A New On-Chip ESD Strategy Using TFETs-TCAD Based Device and Network Simulations. IEEE Journal of the Electron Devices Society, 2018, 6, 298-308.	2.1	10
111	1-T Capacitorless DRAM Using Laterally Bandgap Engineered Si-Si:C Heterostructure Bipolar I-MOS for Improved Sensing Margin and Retention Time. IEEE Nanotechnology Magazine, 2018, 17, 543-551.	2.0	10
112	National Education Policy: How does it Affect Higher Education in India?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2020, 37, 327-328.	3.2	10
113	The effects of emitter region recombination and bandgap narrowing on the current gain and the collector lifetime of high-voltage bipolar transistors. IEEE Transactions on Electron Devices, 1989, 36, 1803-1810.	3.0	9
114	Selective reactive ion etching of PECVD silicon nitride over amorphous silicon in and nitrogen containing plasma gas mixtures. Solid-State Electronics, 1996, 39, 33-37.	1.4	9
115	A New Hetero-material Stepped Gate (HSG) SOI LDMOS for RF Power Amplifier Applications. , 2010, , .		9
116	GaAs Tunnel Diode With Electrostatically Doped n-Region: Proposal and Analysis. IEEE Transactions on Electron Devices, 2015, 62, 3445-3448.	3.0	9
117	Schottky Barrier FET Biosensor for Dual Polarity Detection: A Simulation Study. IEEE Electron Device Letters, 2017, 38, 1594-1597.	3.9	9
118	Realizing highâ€voltage thin film lateral bipolar transistors on SOI with a collectorâ€tub. Microelectronics International, 2005, 22, 3-9.	0.6	8
119	ShOC rectifier: a new metal-semiconductor device with excellent forward and reverse characteristics. IEEE Transactions on Electron Devices, 2005, 52, 130-132.	3.0	8
120	Enhanced Breakdown Voltage, Diminished Quasi-Saturation, and Self-Heating Effects in SOI Thin-Film Bipolar Transistors for Improved Reliability: A TCAD Simulation Study. IEEE Transactions on Device and Materials Reliability, 2006, 6, 306-314.	2.0	8
121	Expanding the Boundaries of Your Research Using Social Media: Stand-Up and Be Counted. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2014, 31, 255-257.	3.2	8
122	Novel lateral merged double Schottky (LMDS) rectifier: proposal and design. IET Circuits, Devices and Systems, 2001, 148, 165.	0.6	7
123	A new low-loss lateral trench sidewall Schottky (LTSS) rectifier on SOI with high and sharp breakdown voltage. IEEE Transactions on Electron Devices, 2002, 49, 1316-1319.	3.0	7
124	Realising wide bandgap P-SiC-emitter lateral heterojunction bipolar transistors with low collectorâ€“emitter offset voltage and high current gain: a novel proposal using numerical simulation. IET Circuits, Devices and Systems, 2004, 151, 399.	0.6	7
125	Analytical Drain Current Model of Nanoscale Strained-Si/SiGe MOSFETs for Analog Circuit Simulation. , 2007, , .		7
126	A novel Doping-less Bipolar Transistor with Schottky Collector. , 2011, , .		7

#	Article	IF	Citations
127	Compact Modeling of Partially Depleted Silicon-on-Insulator Drain-Extended MOSFET (DEMOSFET) Including High-Voltage and Floating-Body Effects. IEEE Transactions on Electron Devices, 2011, 58, 3485-3493.	3.0	7
128	Making Your Research Paper Discoverable: Title Plays the Winning Trick. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2013, 30, 361.	3.2	7
129	A Novel Cascade-Free 5-V ESD Clamp Using I-MOS: Proposal and Analysis. IEEE Transactions on Device and Materials Reliability, 2016, 16, 200-207.	2.0	7
130	In_{0.53}Ga_{0.47}As/InP Trench-Gate Power MOSFET Based on Impact Ionization for Improved Performance: Design and Analysis. IEEE Transactions on Electron Devices, 2017, 64, 4561-4567.	3.0	7
131	Collector recombination lifetime from the quasi-saturation analysis of high-voltage bipolar transistors. IEEE Transactions on Electron Devices, 1990, 37, 2395-2398.	3.0	6
132	Enhanced current gain in SiC power BJTs using a novel surface accumulation layer transistor concept. Microelectronic Engineering, 2005, 81, 90-95.	2.4	6
133	Special Issue on Nanowire Transistors: Modeling, Device Design, and Technology. IEEE Transactions on Electron Devices, 2008, 55, 2813-2819.	3.0	6
134	Drain current model for SOI TFET considering source and drain side tunneling. , 2014, , .		6
135	Miller's approximation in advanced bipolar transistors under nonlocal impact ionization conditions. IEEE Transactions on Electron Devices, 1994, 41, 2471-2473.	3.0	5
136	Lateral thin-film Schottky (LTFS) rectifier on SOI: a device with higher than plane parallel breakdown voltage. IEEE Transactions on Electron Devices, 2002, 49, 181-184.	3.0	5
137	A new, high-voltage 4H-SiC lateral dual sidewall schottky (LDSS) rectifier: theoretical investigation and analysis. IEEE Transactions on Electron Devices, 2003, 50, 1690-1693.	3.0	5
138	On the Parasitic Gate Capacitance of Small-Geometry MOSFETs. IEEE Transactions on Electron Devices, 2005, 52, 1676-1677.	3.0	5
139	On the dominant recombination level of platinum in silicon. Physica Status Solidi A, 1985, 87, 651-655.	1.7	4
140	Design tradeoffs for improved V/sub CE(sat/) versus I/sub C/ of bipolar transistors under forced gain conditions. IEEE Transactions on Electron Devices, 1994, 41, 398-402.	3.0	4
141	2D-simulation and analysis of lateral SiC N-emitter SiGe P-base Schottky metal-collector (NPM) HBT on SOI. Microelectronics Reliability, 2003, 43, 1145-1149.	1.7	4
142	A new lateral SiGe-base PNM Schottky collector bipolar transistor on SOI for non-saturating VLSI logic design. , 0, , .		4
143	Proposal and design of a new SiC-emitter lateral NPM Schottky collector bipolar transistor on SOI for VLSI applications. IET Circuits, Devices and Systems, 2004, 151, 63.	0.6	4
144	Guest Editorial Special Issue on Nanowire Transistors: Modeling, Device Design, and Technology. IEEE Nanotechnology Magazine, 2008, 7, 643-650.	2.0	4

#	Article	IF	Citations
145	Guest Editorial Special Issue on Light-Emitting Diodes. IEEE Transactions on Electron Devices, 2010, 57, 7-11.	3.0	4
146	Honestly speaking about academic dishonesty. IETE Technical Review (Institution of Electronics and) Tj ETQq0 0 0 rgBT /Overlock 10 Tf 5	3.2	4
147	Smart Cities with Massive Data Centric Living are Hard to Build Without 5G Networks. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2015, 32, 237-239.	3.2	4
148	Induced dielectric modulated tunnel field effect transistor biosensor (I-DMTFET): Proposal and investigation. , 2017, , .		4
149	Realising high-current gain p-n-p transistors using a novel surface accumulation layer transistor (SALTran) concept. IET Circuits, Devices and Systems, 2005, 152, 178.	0.6	3
150	The Simulation of a new asymmetrical double-gate poly-Si TFT with modified channel conduction mechanism for highly reduced OFF-state leakage current. IEEE Transactions on Device and Materials Reliability, 2005, 5, 675-682.	2.0	3
151	Being Wary of Plagiarism. IETE Technical Review (Institution of Electronics and Telecommunication) Tj ETQq1 1 0.784314 rgBT /Overl	3.2	3
152	Face Recognition by Machines: Is It an Effective Surveillance Tactic?. IETE Technical Review (Institution) Tj ETQq0 0 0 rgBT /Overlock 10 T	3.2	3
153	The Malady of Technology in Our Lives: Is Anyone Listening?. IETE Technical Review (Institution of) Tj ETQq1 1 0.784314 rgBT /Overlo	3.2	3
154	Schottky bipolar I-MOS: An I-MOS with Schottky electrodes and an open-base BJT configuration for reduced operating voltage. Superlattices and Microstructures, 2017, 104, 422-427.	3.1	3
155	Charge Plasma High Voltage PIN Diode Investigation. , 2018, , .		3
156	What is in store in January-February 2019 issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2019, 36, 1-2.	3.2	3
157	National Centre on Artificial Intelligence: India on the Move. IETE Technical Review (Institution of) Tj ETQq1 1 0.784314 rgBT /Overlo	3.2	3
158	Optimum collector EPI-thickness of advanced bipolar transistors for high speed and high current operation. Solid-State Electronics, 1994, 37, 1885-1887.	1.4	2
159	Inverse modeling of delta doped pseudomorphic high electron mobility transistors. Journal of Vacuum Science and Technology A: Vacuum, Surfaces and Films, 2004, 22, 1036.	2.1	2
160	A new Surface Accumulation Layer Transistor (SALTran) concept for current gain enhancement in bipolar transistors. , 0, , .		2
161	A High Current Gain Horizontal Current Bipolar Transistor (HCBT) Technology for the BiCMOS Integration with FinFETs. , 0, , .		2
162	New Silicon Carbide Schottky-gate Bipolar Mode Field Effect Transistor (SiC SBMFET) without PN Junction. , 2006, , .		2

#	Article	IF	Citations
163	Approaches to nanoscale MOSFET compact modeling using surface potential based models. , 2007, , .		2
164	A dc model for partially depleted SOI laterally diffused MOSFETs utilizing the HiSIM-HV compact model. Journal of Computational Electronics, 2013, 12, 460-468.	2.5	2
165	A Drain-side Gate-underlap I-MOS (DGI-MOS) transistor as a label-free biosensor for detection of charged biomolecules. , 2014, , .		2
166	Controlling the ON-resistance in SOI LDMOS using parasitic bipolar junction transistor. Journal of Computational Electronics, 2014, 13, 857-861.	2.5	2
167	Global University Rankings: What should India do?. IETE Technical Review (Institution of Electronics) Tj ETQq1 1 0.784314 rgBT /Overlock	3.2	2
168	Two dimensional analytical model for the threshold voltage of a Gate All Around Nanowire tunneling FET with localized charges. , 2015, , .		2
169	DC Drain Current Model for Tunnel FETs Considering Source and Drain Depletion Regions. , 2017, , .		2
170	Thin Capacitively-Coupled Thyristor as an Ultrasensitive Label-Free Nanogap Biosensor: Proposal and Investigation. , 2017, 1, 1-4.		2
171	COVID-19: How Institutions, Teachers and Students in India have geared up for Online Education?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2020, 37, 221-222.	3.2	2
172	Is India going to be a major hub of semiconductor chip manufacturing?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2021, 38, 279-281.	3.2	2
173	A new SiGe Stepped Gate (SSG) thin film SOI LDMOS for enhanced breakdown voltage and reduced delay. , 2009, , .		2
174	Digital University â€“ Indian Education Reaching out to Everyone. IETE Technical Review (Institution of) Tj ETQq0 0 0 rgBT /Overlock 10	3.2	2
175	Base etched selfaligned transistor technology for advanced polyemitter bipolar transistors. Electronics Letters, 1994, 30, 819-820.	1.0	1
176	Cjc and the output conductance of advanced bipolar junction transistors under nonlocal impact ionization conditions. Solid-State Electronics, 1996, 39, 1819-1821.	1.4	1
177	Optimum collector width of VLSI bipolar transistors for maximum f/sub max/ at high current densities. IEEE Transactions on Electron Devices, 1997, 44, 903-905.	3.0	1
178	Miller's approximation in VLSI and power bipolar transistors with reach-through collectors. IEEE Transactions on Electron Devices, 1997, 44, 2305-2307.	3.0	1
179	Enhanced current gain in SiC power BJTs using surface accumulation layer transistor (SALTran) concept. , 0, , .		1
180	Gate-induced barrier field effect transistor (GBFET) - a new thin film transistor for active matrix liquid crystal display systems. , 2006, , .		1

#	Article	IF	Citations
181	New Silicon Carbide (SiC) Hetero-Junction Darlington Transistor. , 2006, , .		1
182	A New Gate Induced Barrier Thin-Film Transistor (GIB-TFT) for Active Matrix Liquid Crystal Displays: Design and Performance Considerations. Journal of Display Technology, 2006, 2, 372-377.	1.2	1
183	Enhanced breakdown voltage and reduced self-heating effects in thin-film lateral bipolar transistors: Design and analysis using 2-D simulation. Microelectronic Engineering, 2006, 83, 303-311.	2.4	1
184	New Schottky-Gate Bipolar-Mode Field-Effect Transistor (SBMFET): Design and Analysis Using Two-Dimensional Simulation. IEEE Transactions on Electron Devices, 2006, 53, 2364-2369.	3.0	1
185	A new grounded lamination gate (GLG) for diminished fringe-capacitance effects in high-/spl kappa/ gate-dielectric MOSFETs. IEEE Transactions on Electron Devices, 2006, 53, 2578-2581.	3.0	1
186	Controlled deposition of aligned carbon nanotubes by floating electrodes dielectrophoresis. , 2012, , .		1
187	Literal and Intelligent Plagiarism: Students Beware!. IETE Technical Review (Institution of Electronics) Tj ETQq1 1 0.784314 rgBT /Over	3.2	1
188	Facing the Students on Facebook: Are You Game for It?. IETE Technical Review (Institution of) Tj ETQq0 0 0 rgBT /Overlock 10 Tf 50 462	3.2	1
189	Numerical study of the threshold voltage of TFETs with localized charges. , 2014, , .		1
190	Telling Lies to Describe Truth: Do we Emphasize the Importance of â€œThe Art of Approximationsâ€•to the Students?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2014, 31, 1-3.	3.2	1
191	A Compact Analytical Model for the drain current of a TFET with non-abrupt doping profile incorporating the effect of band-gap narrowing. , 2015, , .		1
192	Kudos to the Reviewers. IETE Technical Review (Institution of Electronics and Telecommunication) Tj ETQq0 0 0 rgBT /Overlock 10 Tf 50	3.2	1
193	Investigating the Doping Profiles in emerging Nanowire Junctionless Accumulation Mode FETs from the L-BTBT perspective. , 2019, , .		1
194	Controlling L-BTBT in the Ultra-short channel Nanowire Junctionless Accumulation FETs using Overlapping Gate-on- Drain. , 2019, , .		1
195	What is in store in the January-February 2020 issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2020, 37, 1-2.	3.2	1
196	A simple hole scattering length model for the solution of charge transport in bipolar transistors. IEEE Transactions on Electron Devices, 1999, 46, 1186-1188.	3.0	0
197	A novel collector-tub concept for realizing high-voltage lateral bipolar transistors on SOI. , 2003, , .		0
198	Two-dimensional analytical modeling of nanoscale electrically shallow junction (EJ) fully depleted SOI MESFET. , 0, , .		0

#	Article	IF	Citations
199	Development of a Monte Carlo Simulation Suite for Predicting the Electron Beam Interaction with Resist on Semiconductor Substrates. IETE Journal of Research, 2005, 51, 301-309.	2.6	0
200	Siliconâ€onâ€insulator lateral dual sidewall Schottky (SOIâ€LDSS) concept for improved rectifier performance: a twoâ€dimensional simulation study. Microelectronics International, 2006, 23, 16-18.	0.6	0
201	Writing Skills and Review Articles: "Walking the Path from Idea to Print". IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2009, 26, 225.	3.2	0
202	Spam Email: The Unwanted Guest at Your Doorstep!. IETE Technical Review (Institution of Electronics) Tj ETQq0 0 0 rgBT /Overlock 10 T	3.2	0
203	Guidelines for Theme-based Special Issues. IETE Technical Review (Institution of Electronics and) Tj ETQq1 1 0.784314 rgBT /Overlock	3.2	0
204	Reflections on Teaching a Large Class. IETE Technical Review (Institution of Electronics and) Tj ETQq0 0 0 rgBT /Overlock 10 Tf 50 542 T	3.2	0
205	Modeling of Partially Depleted SOI DEMOSFETs with a Sub-circuit Utilizing the HiSIM-HV Compact Model. , 2012, , .		0
206	Kudos to our reviewers. IETE Technical Review (Institution of Electronics and Telecommunication) Tj ETQq0 0 0 rgBT /Overlock 10 Tf 50	3.2	0
207	How does the power of "Suggestion" influence studentsâ€² performance?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2013, 30, 273.	3.2	0
208	Back to Basics: Why Every Student and Professor Should Ride a Bicycle on a University Campus?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2013, 30, 165.	3.2	0
209	Quantum Computing in India: An Opportunity that Should Not Be Missed. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2014, 31, 187-189.	3.2	0
210	We are Expanding the Editorial Board. IETE Technical Review (Institution of Electronics and) Tj ETQq0 0 0 rgBT /Overlock 10 Tf 50 302 T	3.2	0
211	The Pay or Perish Game: Why we should stand up against â€˜active discriminationâ€™ for the survival of net neutrality. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2015, 32, 161-163.	3.2	0
212	Call Drops in Mobile Wireless Networks: Calling your attention. IETE Technical Review (Institution of) Tj ETQq0 0 0 rgBT /Overlock 10 Tf	3.2	0
213	What is in Store in the November-December 2016 issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2016, 33, 571-572.	3.2	0
214	IETE Technical Reviewâ€" A Rising International Journal from India. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2016, 33, 91-92.	3.2	0
215	What is in Store in the Julyâ€"August issue of IETE Technical Review?. IETE Technical Review (Institution) Tj ETQq1 1 0.784314 rgBT /O	3.2	0
216	What is in Store in the Mayâ€"June issue of IETE Technical Review?. IETE Technical Review (Institution of) Tj ETQq0 0 0 rgBT /Overlock 1	3.2	0

#	Article	IF	Citations
217	What is in Store in the Septemberâ€“October 2016 Issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2016, 33, 453-454.	3.2	0
218	What is in Store in the January-February 2017 Issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2017, 34, 1-2.	3.2	0
219	What is in Store in the Mayâ€“June 2017 issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2017, 34, 221-222.	3.2	0
220	What is in Store in the Marchâ€“April 2017 issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2017, 34, 111-112.	3.2	0
221	What is in Store in the Julyâ€“August 2017 Issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2017, 34, 341-342.	3.2	0
222	What is in Store in the September-October 2017 Issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2017, 34, 461-462.	3.2	0
223	Happiness and Technological Advances: Where are we heading?. IETE Technical Review (Institution of) Tj ETQq1 1 0.784314 rgBT /Ove	3.2	0
224	What is in store in the November-December 2018 issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2018, 35, 549-550.	3.2	0
225	What is in store in store in September-October 2018 issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2018, 35, 439-440.	3.2	0
226	Coming Out of the Past: Time for Engineers to Work Alongside with Social Scientists. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2018, 35, 221-222.	3.2	0
227	What is in store in the May-June 2019 issue of IETE Technical Review?. IETE Technical Review (Institution) Tj ETQq1 1 0.784314 rgBT /Ov	3.2	0
228	What is in store in the September-October 2020 issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2020, 37, 439-440.	3.2	0
229	What is in store in the March-April 2021 issue of IETE Technical Review?. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2021, 38, 195-196.	3.2	0
230	COVID-19, Mathematical Models and Optimism. IETE Technical Review (Institution of Electronics and) Tj ETQq0 0 0 rgBT /Overlock 10 Tf	3.2	0
231	Transition to Online System and Thoughts on Peer Review Process. IETE Technical Review (Institution) Tj ETQq1 1 0.784314 rgBT /Ove	3.2	0
232	An academicianâ€²s reminiscences on giving interesting and effective public lectures. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2012, 29, 435.	3.2	0
233	Investigating the Scalability of Nanowire Junctionless Accumulation Mode FETs using an Intrinsic Pocket. , 2019, , .		0
234	Efforts of reviewers and editors need to be recognized for their service to the research community and scientific development. IETE Technical Review (Institution of Electronics and Telecommunication) Tj ETQq0 0 0 rgBT /Overlock 10 Tf	3.2	0