Johannes Schemmel

List of Publications by Year
in descending order

69	3,589	361413	254184
papers	citations	20 h-index	43 g-index

71	71	71	2620
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Emulating Dendritic Computing Paradigms on Analog Neuromorphic Hardware. Neuroscience, 2022, 489, 290-300.	2.3	22
2	The Heidelberg Spiking Data Sets for the Systematic Evaluation of Spiking Neural Networks. IEEE Transactions on Neural Networks and Learning Systems, 2022, 33, 2744-2757.	11.3	61
3	Spiking neuromorphic chip learns entangled quantum states. SciPost Physics, 2022, 12, .	4.9	5
4	Surrogate gradients for analog neuromorphic computing. Proceedings of the National Academy of Sciences of the United States of America, 2022, 119, .	7.1	37
5	The BrainScaleS-2 Accelerated Neuromorphic System With Hybrid Plasticity. Frontiers in Neuroscience, 2022, 16, 795876.	2.8	50
6	Accelerated Analog Neuromorphic Computing. , 2022, , 83-102.		13
7	Demonstrating BrainScaleS-2 Inter-Chip Pulse-Communication using EXTOLL. , 2022, , .		0
8	A Scalable Approach to Modeling on Accelerated Neuromorphic Hardware. Frontiers in Neuroscience, 2022, 16, .	2.8	9
9	The operating system of the neuromorphic BrainScaleS-1 system. Neurocomputing, 2022, 501, 790-810.	5.9	5
10	Neuromorphic Hardware, Large-Scale. , 2022, , 2322-2325.		0
11	Structural plasticity on an accelerated analog neuromorphic hardware system. Neural Networks, 2021, 133, 11-20.	5.9	10
12	Towards Addressing Noise andÂStatic Variations ofÂAnalog Computations Using Efficient Retraining. Communications in Computer and Information Science, 2021, , 409-420.	0.5	2
13	Verification and Design Methods for the BrainScaleS Neuromorphic Hardware System. Journal of Signal Processing Systems, 2020, 92, 1277-1292.	2.1	25
14	Control of criticality and computation in spiking neuromorphic networks with plasticity. Nature Communications, 2020, 11, 2853.	12.8	70
15	hxtorch: PyTorch for BrainScaleS-2. Communications in Computer and Information Science, 2020, , 189-200.	0.5	7
16	Inference with Artificial Neural Networks on Analog Neuromorphic Hardware. Communications in Computer and Information Science, 2020, , 201-212.	0.5	6
17	Stochasticity from function â€" Why the Bayesian brain may need no noise. Neural Networks, 2019, 119, 200-213.	5.9	19
18	Demonstrating Advantages of Neuromorphic Computation: A Pilot Study. Frontiers in Neuroscience, 2019, 13, 260.	2.8	83

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19	Deterministic networks for probabilistic computing. Scientific Reports, 2019, 9, 18303.	3.3	10
20	Accelerated Physical Emulation of Bayesian Inference in Spiking Neural Networks. Frontiers in Neuroscience, 2019, 13, 1201.	2.8	22
21	Brain-Inspired Hardware for Artificial Intelligence: Accelerated Learning in a Physical-Model Spiking Neural Network. Lecture Notes in Computer Science, 2019, , 119-122.	1.3	2
22	Large-Scale Neuromorphic Spiking Array Processors: A Quest to Mimic the Brain. Frontiers in Neuroscience, 2018, 12, 891.	2.8	177
23	An Accelerated LIF Neuronal Network Array for a Large-Scale Mixed-Signal Neuromorphic Architecture. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 4299-4312.	5.4	59
24	A Mixed-Signal Structured AdEx Neuron for Accelerated Neuromorphic Cores. IEEE Transactions on Biomedical Circuits and Systems, 2018, 12, 1027-1037.	4.0	38
25	Spiking neurons with short-term synaptic plasticity form superior generative networks. Scientific Reports, 2018, 8, 10651.	3.3	20
26	Demonstrating Hybrid Learning in a Flexible Neuromorphic Hardware System. IEEE Transactions on Biomedical Circuits and Systems, 2017, 11, 128-142.	4.0	87
27	Neuromorphic hardware in the loop: Training a deep spiking network on the BrainScaleS wafer-scale system. , 2017, , .		99
28	From LIF to AdEx neuron models: Accelerated analog 65 nm CMOS implementation. , 2017, , .		5
29	Full wafer redistribution and wafer embedding as key technologies for a multi-scale neuromorphic hardware cluster. , 2017, , .		4
30	An accelerated analog neuromorphic hardware system emulating NMDA- and calcium-based non-linear dendrites. , 2017, , .		50
31	Robustness from structure: Inference with hierarchical spiking networks on analog neuromorphic hardware. , 2017, , .		1
32	Effect of Heterogeneity on Decorrelation Mechanisms in Spiking Neural Networks: A Neuromorphic-Hardware Study. Physical Review X, 2016, 6, .	8.9	15
33	Stochastic inference with spiking neurons in the high-conductance state. Physical Review E, 2016, 94, 042312.	2.1	46
34	A highly tunable 65-nm CMOS LIF neuron for a large scale neuromorphic system. , 2016, , .		19
35	A highly tunable 65-nm CMOS LIF neuron for a large scale neuromorphic system. , 2016, , .		0
36	Deterministic neural networks as sources of uncorrelated noise for probabilistic computations. BMC Neuroscience, 2015, 16, .	1.9	2

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37	The high-conductance state enables neural sampling in networks of LIF neurons. BMC Neuroscience, 2015, 16, .	1.9	5
38	Probabilistic inference in discrete spaces can be implemented into networks of LIF neurons. Frontiers in Computational Neuroscience, 2015, 9, 13.	2.1	17
39	Characterization and Compensation of Network-Level Anomalies in Mixed-Signal Neuromorphic Modeling Platforms. PLoS ONE, 2014, 9, e108590.	2.5	42
40	Neuromorphic Hardware, Large Scale. , 2014, , 1-4.		0
41	An analog dynamic memory array for neuromorphic hardware. , 2013, , .		16
42	Neuromorphic learning towards nano second precision. , 2013, , .		8
43	A location-independent direct link neuromorphic interface. , 2013, , .		13
44	Six Networks on a Universal Neuromorphic Computing Substrate. Frontiers in Neuroscience, 2013, 7, 11.	2.8	131
45	Reward-based learning under hardware constraintsâ€"using a RISC processor embedded in a neuromorphic substrate. Frontiers in Neuroscience, 2013, 7, 160.	2.8	27
46	Live demonstration: A scaled-down version of the BrainScaleS wafer-scale neuromorphic system. , 2012, , .		41
47	Is a 4-Bit Synaptic Weight Resolution Enough? â€“ Constraints on Enabling Spike-Timing Dependent Plasticity in Neuromorphic Hardware. Frontiers in Neuroscience, 2012, 6, 90.	2.8	77
48	Neuromorphic Silicon Neuron Circuits. Frontiers in Neuroscience, 2011, 5, 73.	2.8	1,004
49	A comprehensive workflow for general-purpose neural modeling with highly configurable neuromorphic hardware systems. Biological Cybernetics, 2011, 104, 263-296.	1.3	72
50	Compensating Inhomogeneities of Neuromorphic VLSI Devices Via Short-Term Synaptic Plasticity. Frontiers in Computational Neuroscience, 2010, 4, 129.	2.1	23
51	Simulator-like exploration of cortical network architectures with a mixed-signal VLSI system. , 2010, , .		8
52	A wafer-scale neuromorphic hardware system for large-scale neural modeling. , 2010, , .		449
53	Live demonstration: Simulator-like exploration of cortical network architectures with a mixed-signal VLSI system. , 2010, , .		0
54	A computer controlled pendulum with position readout. American Journal of Physics, 2010, 78, 555-561.	0.7	5

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55	High-conductance states on a neuromorphic hardware system. , 2009, , .		4
56	A QoS network architecture to interconnect large-scale VLSI neural networks. , 2009, , .		8
57	Establishing a Novel Modeling Tool: A Python-based Interface for a Neuromorphic Hardware System. Frontiers in Neuroinformatics, 2009, 3, 17.	2.5	35
58	Wafer-scale integration of analog neural networks. , 2008, , .		175
59	Realizing biological spiking network models in a configurable wafer-scale hardware system. , 2008, , .		40
60	Spike-Frequency Adapting Neural Ensembles: Beyond Mean Adaptation and Renewal Theories. Neural Computation, 2007, 19, 2958-3010.	2.2	59
61	Modeling Synaptic Plasticity within Networks of Highly Accelerated I&F Neurons. , 2007, , .		56
62	Interconnecting VLSI Spiking Neural Networks Using Isochronous Connections. , 2007, , 471-478.		10
63	A Software Framework for Tuning the Dynamics of Neuromorphic Silicon Towards Biology. , 2007, , 479-486.		7
64	Operational Amplifiers: An Example for Multi-objective Optimization on an Analog Evolvable Hardware Platform. Lecture Notes in Computer Science, 2005, , 86-97.	1.3	9
65	A Mixed-Mode Analog Neural Network Using Current-Steering Synapses. Analog Integrated Circuits and Signal Processing, 2004, 38, 233-244.	1.4	17
66	A Scalable Switched Capacitor Realization of the Resistive Fuse Network. Analog Integrated Circuits and Signal Processing, 2002, 32, 135-148.	1.4	14
67	A self-calibrating single-chip CMOS camera with logarithmic response. IEEE Journal of Solid-State Circuits, 2001, 36, 586-596.	5.4	115
68	CMOS image sensor with logarithmic response and self-calibrating fixed pattern noise correction. , 1998, 3410, 117.		17
69	<title>Camera with adaptive photoreceptors in analog CMOS technology</title>. , 1996, , .		0