Peter Milder

List of Publications by Year in descending order

Source: https://exaly.com/author-pdf/7729717/publications.pdf

Version: 2024-02-01

33	1,080	7	10
papers	citations	h-index	g-index
33	33	33	858
all docs	docs citations	times ranked	citing authors

#	Article	IF	CITATIONS
1	Fused-layer CNN accelerators. , 2016, , .		374
2	Maximizing CNN Accelerator Efficiency Through Resource Partitioning., 2017,,.		150
3	Computer Generation of Hardware for Linear Digital Signal Processing Transforms. ACM Transactions on Design Automation of Electronic Systems, 2012, 17, 1-33.	2.6	97
4	Maximizing CNN Accelerator Efficiency Through Resource Partitioning. Computer Architecture News, 2017, 45, 535-547.	2.5	70
5	Escher: A CNN Accelerator with Flexible Buffering to Minimize Off-Chip Transfer. , 2017, , .		64
6	Generation of optical OFDM signals using 214 GS/s real time digital signal processing. Optics Express, 2009, 17, 17658.	3.4	63
7	Overcoming resource underutilization in spatial CNN accelerators. , 2016, , .		37
8	Streaming Sorting Networks. ACM Transactions on Design Automation of Electronic Systems, 2016, 21, 1-30.	2.6	31
9	Optical OFDM for the data center. , 2010, , .		28
10	Computer generation of streaming sorting networks. , 2012, , .		27
11	"Smart" design space sampling to predict Pareto-optimal solutions. , 2012, , .		18
12	Nautilus. , 2015, , .		18
13	Optimizing FFT Precision in Optical OFDM Transceivers. IEEE Photonics Technology Letters, 2011, 23, 1550-1552.	2.5	17
14	FPGA-Accelerated Samplesort for Large Data Sets. , 2020, , .		16
15	Design studies for ASIC implementations of 28 GS/s optical QPSK- and 16-QAM-OFDM transceivers. Optics Express, 2011, 19, 20857.	3.4	14
16	Design studies for an ASIC implementation of an optical OFDM transceiver. , 2010, , .		9
17	"Smart" design space sampling to predict Pareto-optimal solutions. ACM SIGPLAN Notices, 2012, 47, 119-128.	0.2	9
18	Argus: An End-to-End Framework for Accelerating CNNs on FPGAs. IEEE Micro, 2019, 39, 17-25.	1.8	7

#	Article	IF	Citations
19	FPGASwarm: High Throughput Model Checking on FPGAs. , 2018, , .		6
20	A Full-System VM-HDL Co-Simulation Framework for Servers with PCIe-Connected FPGAs., 2018,,.		5
21	Flick: Fast and Lightweight ISA-Crossing Call for Heterogeneous-ISA Environments. , 2020, , .		5
22	Error Probability Models for Voltage-Scaled Multiply-Accumulate Units. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1665-1675.	3.1	5
23	MEMOCODE 2014 design contest: k-Nearest Neighbors with Mahalanobis distance metric. , 2014, , .		2
24	Quantifying Energy and Latency Improvements of FPGA-Based Sensors for Low-Cost Spectrum Monitoring. , 2018, , .		2
25	Medusa: A Scalable Interconnect for Many-Port DNN Accelerators and Wide DRAM Controller Interfaces. , 2018, , .		2
26	Real-time DSP-based optical OFDM transmission. , 2010, , .		1
27	Trade-offs in execution signature compression for reliable processor systems. , 2014, , .		1
28	Practical Matlab experience in lecture-based signals and systems courses., 2017,,.		1
29	Area, Throughput, and Power Trade-Offs for FPGA- and ASIC-Based Execution Stream Compression. Transactions on Embedded Computing Systems, 2017, 16, 1-20.	2.9	1
30	Trade-offs in execution signature compression for reliable processor systems. , 2014, , .		0
31	MEMOCODE 2016 design contest: K-means clustering. , 2016, , .		0
32	Runtime-Programmable Pipelines for Model Checkers on FPGAs. , 2019, , .		0
33	Practical Model Checking on FPGAs. ACM Transactions on Reconfigurable Technology and Systems, 2021, 14, 1-18.	2.5	0