Dae-Hyun Kim

List of Publications by Year
in descending order

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48	898	933447 10	794594 19
papers	citations	h-index	g-index

48	48	48	581
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	An 8.5-Gb/s/Pin 12-Gb LPDDR5 SDRAM With a Hybrid-Bank Architecture, Low Power, and Speed-Boosting Techniques. IEEE Journal of Solid-State Circuits, 2021, 56, 212-224.	5.4	4
2	22.2 An 8.5Gb/s/pin 12Gb-LPDDR5 SDRAM with a Hybrid-Bank Architecture using Skew-Tolerant, Low-Power and Speed-Boosting Techniques in a 2nd generation 10nm DRAM Process. , 2020, , .		14
3	Optimization of Experimental Designs for System- Level Accelerated Life Test in a Memory System Degraded by Time-Dependent Dielectric Breakdown. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1640-1651.	3.1	5
4	Optimal Accelerated Test Regions for Time- Dependent Dielectric Breakdown Lifetime Parameters Estimation in FinFET Technology. , 2018, , .		2
5	A methodology for estimating memory lifetime using a system-level accelerated life test and error-correcting codes. , 2017, , .		1
6	An ECC-Assisted Postpackage Repair Methodology in Main Memory Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2045-2058.	3.1	5
7	Front-end of line and middle-of-line time-dependent dielectric breakdown reliability simulator for logic circuits. Microelectronics Reliability, 2017, 76-77, 81-86.	1.7	9
8	Analysis of errors in estimating wearout characteristics of time-dependent dielectric breakdown using system-level accelerated life test. Microelectronics Reliability, 2017, 76-77, 47-52.	1.7	2
9	Memory reliability estimation degraded by TDDB using circuit-level accelerated life test. , 2017, , .		2
10	Design for reliability: A duty-cycle management system for timing violations. , 2016, , .		1
11	TDDB-emerald: A methodology for estimating memory reliability degradation resulting from time-dependent dielectric breakdown. , 2016, , .		3
12	ECC-ASPIRIN: An ECC-assisted post-package repair scheme for aging errors in DRAMs. , 2016, , .		6
13	Built-In Self-Test Methodology With Statistical Analysis for Electrical Diagnosis of Wearout in a Static Random Access Memory Array. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2521-2534.	3.1	10
14	Built-in self-test for bias temperature instability, hot-carrier injection, and gate oxide breakdown in embedded DRAMs. Microelectronics Reliability, 2015, 55, 2113-2118.	1.7	5
15	Memory yield and lifetime estimation considering aging errors. , 2015, , .		5
16	Architectural Support for Mitigating Row Hammering in DRAM Memories. IEEE Computer Architecture Letters, 2015, 14, 9-12.	1.5	71
17	Design and Analysis of 3D-MAPS (3D Massively Parallel Processor with Stacked Memory). IEEE Transactions on Computers, 2015, 64, 112-125.	3.4	52
18	AVATAR: A Variable-Retention-Time (VRT) Aware Refresh for DRAM Systems. , 2015, , .		144

#	Article	IF	Citations
19	The die-to-die calibrated combined model of negative bias temperature instability and gate oxide breakdown from device to system. Microelectronics Reliability, 2015, 55, 1404-1411.	1.7	4
20	AVERT: An elaborate model for simulating variable retention time in DRAMs. Microelectronics Reliability, 2015, 55, 1313-1319.	1.7	3
21	Impact of die partitioning on reliability and yield of 3D DRAM. , 2014, , .		2
22	Backend Dielectric Reliability Full Chip Simulator. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1750-1762.	3.1	7
23	Study of Through-Silicon-Via Impact on the 3-D Stacked IC Layout. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 862-874.	3.1	70
24	ArchShield. Computer Architecture News, 2013, 41, 72-83.	2.5	29
25	Block-level designs of die-to-wafer bonded 3D ICs and their design quality tradeoffs. , 2013, , .		4
26	Design Quality Trade-Off Studies for 3-D ICs Built With Sub-Micron TSVs and Future Devices. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2012, 2, 240-248.	3.6	17
27	Block-level 3D IC design with through-silicon-via planning. , 2012, , .		25
28	Design quality tradeoff studies for 3D ICs built with nano-scale TSVs and devices. , 2012, , .		6
29	TSV density-driven global placement for 3D stacked ICs. , 2011, , .		5
30	Impact of nano-scale through-silicon vias on the quality of today and future 3D IC designs. , 2011, , .		18
31	Fast and Accurate Analytical Modeling of Through-Silicon-Via Capacitive Coupling. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2011, 1, 168-180.	2.5	71
32	Pre-Bond and Post-Bond Test and Signal Recovery Structure to Characterize and Repair TSV Defect Induced Signal Degradation in 3-D System. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2011, 1, 1718-1727.	2.5	50
33	Analysis of TSV-to-TSV coupling with high-impedance termination in 3D ICs. , 2011, , .		28
34	Impact of through-silicon-via scaling on the wirelength distribution of current and future 3D ICs. , 2011, , .		4
35	A 7 Gb/s/pin 1 Gbit GDDR5 SDRAM With 2.5 ns Bank to Bank Active Time and No Bank Group Restriction. IEEE Journal of Solid-State Circuits, 2011, 46, 107-118.	5.4	29
36	Backend low-k TDDB chip reliability simulator. , 2011, , .		20

#	Article	IF	Citations
37	A 40nm 2Gb 7Gb/s/pin GDDR5 SDRAM with a programmable DQ ordering crosstalk equalizer and adjustable clock-tracking BW. , 2011, , .		18
38	A 7Gb/s/pin GDDR5 SDRAM with 2.5ns bank-to-bank active time and no bank-group restriction. , 2010, , .		4
39	Design method and test structure to characterize and repair TSV defect induced signal degradation in 3D system. , 2010, , .		55
40	A 40nm 7Gb/s/pin single-ended transceiver with jitter and ISI reduction techniques for high-speed DRAM interface. , 2010, , .		5
41	TDDB chip reliability in copper interconnects. , 2010, , .		1
42	An 80 nm 4 Gb/s/pin 32 bit 512 Mb GDDR4 Graphics DRAM With Low Power and Low Noise Data Bus Inversion. IEEE Journal of Solid-State Circuits, 2008, 43, 121-131.	5.4	54
43	Global bus route optimization with application to microarchitectural design exploration. , 2008, , .		4
44	A 60nm 6Gb/s/pin GDDR5 Graphics DRAM with Multifaceted Clocking and ISI/SSN-Reduction Techniques. , 2008, , .		19
45	Bus-aware microarchitectural floorplanning. , 2008, , .		0
46	An 80nm 4Gb/s/pin 32b 512Mb GDDR4 Graphics DRAM with Low-Power and Low-Noise Data-Bus Inversion. , 2007, , .		4
47	Fabrication of nano-gap accelerometer using photo-assisted electrochemical etching. , 0, , .		0
48	Fabrication of mems structure with nano-gap using photo-assisted electrochemical etching. , 0, , .		1