Takashi Matsukawa

List of Publications by Year
in descending order

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176	1,825	361413	395702
papers	citations	20 h-index	33 g-index

176	176	176	1430
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Impact of Switching Voltage on Complementary Steep-Slope Tunnel Field Effect Transistor Circuits. IEEE Transactions on Electron Devices, 2020, 67, 3876-3882.	3.0	1
2	Process and device integration for silicon tunnel FETs utilizing isoelectronic trap technology to enhance the ON current. Japanese Journal of Applied Physics, 2018, 57, 04FA04.	1.5	4
3	Simulation study of short-channel effects of tunnel field-effect transistors. Japanese Journal of Applied Physics, 2018, 57, 04FD04.	1.5	3
4	Investigation of piezoresistive effect in p-channel metalâ€“oxideâ€“semiconductor field-effect transistors fabricated on circular silicon-on-insulator diaphragms using cost-effective minimal-fab process. Japanese Journal of Applied Physics, 2018, 57, 06HD03.	1.5	6
5	Steep switching in trimmed-gate tunnel FET. AIP Advances, 2018, 8, .	1.3	5
6	Enhancement of capacitance benefit by drain offset structure in tunnel field-effect transistor circuit speed associated with tunneling probability increase. Japanese Journal of Applied Physics, 2018, 57, 04FD13.	1.5	1
7	Fully Integrated, 100-mV Minimum Input Voltage Converter With Gate-Boosted Charge Pump Kick-Started by LC Oscillator for Energy Harvesting. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 392-396.	3.0	40
8	Structural and electrical characterization of epitaxial Ge thin films on Si(001) formed by sputtering. Japanese Journal of Applied Physics, 2017, 56, 04CB01.	1.5	0
9	On the drain bias dependence of long-channel silicon-on-insulator-based tunnel field-effect transistors. Japanese Journal of Applied Physics, 2017, 56, 04CD04.	1.5	2
10	A Closed-Form Expression for Minimum Operating Voltage of CMOS D Flip-Flop. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2007-2016.	3.1	4
11	Tunnel FinFET CMOS inverter with very low short-circuit current for ultralow-power Internet of Things application. Japanese Journal of Applied Physics, 2017, 56, 04CD19.	1.5	15
12	Impact of residual defects caused by extension ion implantation in FinFETs on parasitic resistance and its fluctuation. Solid-State Electronics, 2017, 132, 103-108.	1.4	3
13	Bias temperature instability in tunnel field-effect transistors. Japanese Journal of Applied Physics, 2017, 56, 04CA04.	1.5	2
14	A 0.3-V 1- $mu ext{W}$ Super-Regenerative Ultrasound Wake-Up Receiver With Power Scalability. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1027-1031.	3.0	22
15	Enhanced nickelidation rate in silicon nanowires with interfacial lattice disorder. Journal of Applied Physics, 2017, 122, .	2.5	6
16	An experimental study of solid source diffusion by spin on dopants and its application for minimal silicon-on-insulator CMOS fabrication. Japanese Journal of Applied Physics, 2017, 56, 06GG01.	1.5	10
17	Anomalous Seebeck coefficient observed in silicon nanowire micro thermoelectric generator. Applied Physics Letters, 2017, 111, .	3.3	19
18	Epitaxial growth of Ge thin film on Si (001) by DC magnetron sputtering. Materials Science in Semiconductor Processing, 2017, 70, 3-7.	4.0	4

#	Article	IF	Citations
19	Suppression of tunneling rate fluctuations in tunnel field-effect transistors by enhancing tunneling probability. Japanese Journal of Applied Physics, 2017, 56, 04CD02.	1.5	5
20	Fabrication of PVD-TiN metal-gate SOI-CMOS integrated circuits using minimal-fab and mega-fab hybrid process. , 2016, , .		1
21	Silicon optical switch monolithically integrated with driver electronics and its power efficient driving. , 2016, , .		0
22	ON current enhancement of nanowire Schottky barrier tunnel field effect transistors. Japanese Journal of Applied Physics, 2016, 55, 04ED07.	1.5	3
23	Impact of extension implantation conditions of fin field-effect transistors on gate-induced drain leakage. Japanese Journal of Applied Physics, 2016, 55, 04EB01.	1.5	3
24	(Invited) Floating Gate Type SOI-FinFET Flash Memories with Different Channel Shapes and Interpoly Dielectric Materials. ECS Transactions, 2016, 72, 11-24.	0.5	1
25	Introduction of SiGe/Si heterojunction into novel multilayer tunnel FinFET. Japanese Journal of Applied Physics, 2016, 55, 04EB06.	1.5	15
26	Closed-form analytical model of static noise margin for ultra-low voltage eight-transistor tunnel FET static random access memory. Japanese Journal of Applied Physics, 2016, 55, 04ED06.	1.5	4
27	Robust and compact key generator using physically unclonable function based on logic-transistor-compatible poly-crystalline-Si channel FinFET technology. , 2015, , .		5
28	Spatial variation of the work function in nano-crystalline TiN films measured by dual-mode scanning tunneling microscopy. Japanese Journal of Applied Physics, 2015, 54, 04DA03.	1.5	14
29	Heated ion implantation for high-performance and highly reliable silicon-on-insulator complementary metalâ€“oxideâ€“silicon fin field-effect transistors. Japanese Journal of Applied Physics, 2015, 54, 04DA06.	1.5	4
30	Impact of granular work function variation in a gate electrode on low-frequency noise for fin field-effect transistors. Applied Physics Express, 2015, 8, 044201.	2.4	7
31	Impact of fin length on threshold voltage modulation by back bias for Independent double-gate tunnel fin field-effect transistors. Solid-State Electronics, 2015, 111, 62-66.	1.4	3
32	Highly Vt tunable and low variability triangular fin-channel MOSFETs on SOTB. Microelectronic Engineering, 2015, 147, 290-293.	2.4	0
33	Improvement of epitaxial channel quality on heavily arsenic- and boron-doped Si surfaces and impact on performance of tunnel field-effect transistors. Solid-State Electronics, 2015, 113, 173-178.	1.4	6
34	Channel shape and interpoly dielectric material effects on electrical characteristics of floating-gate-type three-dimensional fin channel flash memories. Japanese Journal of Applied Physics, 2015, 54, 04DD04.	1.5	2
35	Comparative Study of Charge Trapping Type SOI-FinFET Flash Memories with Different Blocking Layer Materials. Journal of Low Power Electronics and Applications, 2014, 4, 153-167.	2.0	5
36	Scaling breakthrough for analog/digital circuits by suppressing variability and low-frequency noise for FinFETs by amorphous metal gate technology. , 2014, , .		4

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37	Ultra-compact 8 Ã— 8 strictly-non-blocking Si-wire PILOSS switch. Optics Express, 2014, 22, 3887.	3.4	105
38	Impact of thermal history of Si nanowire fabrication process on Ni silicidation rate. Japanese Journal of Applied Physics, 2014, 53, 085201.	1.5	4
39	Influence of work function variation of metal gates on fluctuation of sub-threshold drain current for fin field-effect transistors with undoped channels. Japanese Journal of Applied Physics, 2014, 53, 04EC11.	1.5	12
40	Experimental study of three-dimensional fin-channel charge trapping flash memories with titanium nitride and polycrystalline silicon gates. Japanese Journal of Applied Physics, 2014, 53, 04ED16.	1.5	2
41	Performance Enhancement of Tunnel Field-Effect Transistors by Synthetic Electric Field Effect. IEEE Electron Device Letters, 2014, 35, 792-794.	3.9	53
42	Performance evaluation of parallel electric field tunnel field-effect transistor by a distributed-element circuit model. Solid-State Electronics, 2014, 102, 82-86.	1.4	7
43	Experimental Demonstration of Ultrashort-Channel (3 nm) Junctionless FETs Utilizing Atomically Sharp V-Grooves on SOI. IEEE Nanotechnology Magazine, 2014, 13, 208-215.	2.0	59
44	Analysis of Threshold Voltage Flexibility in Ultrathin-BOX SOI FinFETs. Journal of Low Power Electronics and Applications, 2014, 4, 110-118.	2.0	1
45	Experimental study of charge trapping type FinFET flash memory. , 2014, , .		0
46	Variability of short channel junctionless field-effect transistors caused by fluctuation of dopant concentration. , 2013, , .		1
47	1/fNoise Characteristics of Fin-Type Field-Effect Transistors in Saturation Region. Japanese Journal of Applied Physics, 2013, 52, 04CC23.	1.5	0
48	Large current MOSFET on photonic silicon-on-insulator wafers and its monolithic integration with a thermoâ€“optic 2 Ã— 2 Machâ€“Zehnder switch. Optics Express, 2013, 21, 6889.	3.4	21
49	Gate Structure Dependence of Variability in Polycrystalline Silicon Fin-Channel Flash Memories. Japanese Journal of Applied Physics, 2013, 52, 06GE01.	1.5	3
50	Atomic Layer Deposition of SiO₂ for the Performance Enhancement of Fin Field Effect Transistors. Japanese Journal of Applied Physics, 2013, 52, 116503.	1.5	8
51	Suppression of threshold voltage variability of double-gate fin field-effect transistors using amorphous metal gate with uniform work function. Applied Physics Letters, 2013, 102, .	3.3	15
52	Independent-Double-Gate FinFET SRAM Technology. IEICE Transactions on Electronics, 2013, E96.C, 413-423.	0.6	1
53	Fabrication of Floating-Gate-Type Fin-Channel Double- and Tri-Gate Flash Memories and Comparative Study of Their Electrical Characteristics. Japanese Journal of Applied Physics, 2012, 51, 04DD03.	1.5	2
54	Fabrication and Characterization of NOR-Type Tri-Gate Flash Memory with Improved Inter-Poly Dielectric Layer by Rapid Thermal Oxidation. Japanese Journal of Applied Physics, 2012, 51, 06FE19.	1.5	6

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55	Experimental Study of Floating-Gate-Type Metalâ€“Oxideâ€“Semiconductor Capacitors with Nanosize Triangular Cross-Sectional Tunnel Areas for Low Operating Voltage Flash Memory Application. Japanese Journal of Applied Physics, 2012, 51, 06FF01.	1.5	2
56	Experimental Comparisons between Tetrakis(dimethylamino)titanium Precursor-Based Atomic-Layer-Deposited and Physical-Vapor-Deposited Titaniumâ€“Nitride Gate for High-Performance Fin-Type Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2012, 51, 04DA05.	1.5	0
57	(Invited) FinFET Flash Memory Technology. ECS Transactions, 2012, 45, 289-310.	0.5	2
58	(Invited) On-Current Variability Sources of FinFETs: Analysis and Perspective for 14nm-Lg Technology. ECS Transactions, 2012, 45, 231-242.	0.5	0
59	Suppressing V<inf>t</inf> and G<inf>m</inf> variability of FinFETs using amorphous metal gates for 14 nm and beyond. , 2012, , .		22
60	Enhancement of FinFET performance using 25-nm-thin sidewall spacer grown by atomic layer deposition. Solid-State Electronics, 2012, 74, 13-18.	1.4	13
61	Demonstration of Split-Gate Type Trigate Flash Memory With Highly Suppressed Over-Erase. IEEE Electron Device Letters, 2012, 33, 345-347.	3.9	10
62	Variability Origins of Parasitic Resistance in FinFETs With Silicided Source/Drain. IEEE Electron Device Letters, 2012, 33, 474-476.	3.9	15
63	Variability Analysis of Scaled Crystal Channel and Poly-Si Channel FinFETs. IEEE Transactions on Electron Devices, 2012, 59, 573-581.	3.0	12
64	Fin-Height Effect on Poly-Si/PVD-TiN Stacked-Gate FinFET Performance. IEEE Transactions on Electron Devices, 2012, 59, 647-653.	3.0	14
65	A Correlative Analysis Between Characteristics of FinFETs and SRAM Performance. IEEE Transactions on Electron Devices, 2012, 59, 1345-1352.	3.0	3
66	Decomposition of On-Current Variability of nMOS FinFETs for Prediction Beyond 20 nm. IEEE Transactions on Electron Devices, 2012, 59, 2003-2010.	3.0	27
67	High-Frequency Precise Characterization of Intrinsic FinFET Channel. IEICE Transactions on Electronics, 2012, E95.C, 752-760.	0.6	1
68	Fabrication and Characterization of NOR-Type Tri-Gate Flash Memory with Improved Inter-Poly Dielectric Layer by Rapid Thermal Oxidation. Japanese Journal of Applied Physics, 2012, 51, 06FE19.	1.5	2
69	A 0.7-V Opamp in Scaled Low-Standby-Power FinFET Technology. IEICE Transactions on Electronics, 2012, E95.C, 686-695.	0.6	0
70	Fabrication of Floating-Gate-Type Fin-Channel Double- and Tri-Gate Flash Memories and Comparative Study of Their Electrical Characteristics. Japanese Journal of Applied Physics, 2012, 51, 04DD03.	1.5	1
71	Experimental Comparisons between Tetrakis(dimethylamino)titanium Precursor-Based Atomic-Layer-Deposited and Physical-Vapor-Deposited Titaniumâ€“Nitride Gate for High-Performance Fin-Type Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2012, 51, 04DA05.	1.5	2
72	Experimental Study of Floating-Gate-Type Metalâ€“Oxideâ€“Semiconductor Capacitors with Nanosize Triangular Cross-Sectional Tunnel Areas for Low Operating Voltage Flash Memory Application. Japanese Journal of Applied Physics, 2012, 51, 06FF01.	1.5	1

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73	Variability origins of FinFETs and perspective beyond 20nm node. , 2011, , .		3
74	Independent double-gate FinFET SRAM technology. , 2011, , .		4
75	Static noise margin enhancement by flex-pass-gate SRAM. Electronics and Communications in Japan, 2011, 94, 57-64.	0.5	0
76	Correlative analysis between characteristics of 30-nm L<inf>G</inf> FinFETs and SRAM performance. , 2011, , .		1
77	Experimental Study of Physical-Vapor-Deposited Titanium Nitride Gate with An n⁺-Polycrystalline Silicon Capping Layer and Its Application to 20 nm Fin-Type Double-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2011, 50, 04DC14.	1.5	12
78	Experimental Study of Physical-Vapor-Deposited Titanium Nitride Gate with An n+-Polycrystalline Silicon Capping Layer and Its Application to 20 nm Fin-Type Double-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2011, 50, 04DC14.	1.5	6
79	(Invited) Advanced FinFET Technologies: Extension Doping, Vth Controllable CMOS Inverters and SRAM. ECS Transactions, 2010, 28, 385-401.	0.5	1
80	Investigation of Low-Energy Tilted Ion Implantation for Fin-Type Double-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistor Extension Doping. Japanese Journal of Applied Physics, 2010, 49, 04DC18.	1.5	22
81	High-Performance Three-Terminal Fin Field-Effect Transistors Fabricated by a Combination of Damage-Free Neutral-Beam Etching and Neutral-Beam Oxidation. Japanese Journal of Applied Physics, 2010, 49, 04DC17.	1.5	11
82	Minimization of Gate-Induced Drain Leakage by Controlling Gate Underlap Length for Low-Standby-Power Operation of 20-nm-Level Four-Terminal Silicon-on-Insulator Fin-Shaped Field Effect Transistor. Japanese Journal of Applied Physics, 2010, 49, 024203.	1.5	0
83	Investigation of Thermal Stability of TiN Film Formed by Atomic Layer Deposition Using Tetrakis(dimethylamino)titanium Precursor for Metal-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistor. Japanese Journal of Applied Physics, 2010, 49, 04DA16.	1.5	7
84	Variability Analysis of TiN Metal-Gate FinFETs. IEEE Electron Device Letters, 2010, 31, 546-548.	3.9	63
85	Variability analysis of TiN FinFET SRAM cell performance and its compensation using Vth-controllable independent double-gate FinFET. , 2010, , .		0
86	Variability Analysis of TiN FinFET SRAM Cells and Its Compensation by Independent-DG FinFETs. IEEE Electron Device Letters, 2010, 31, 1095-1097.	3.9	4
87	Nanoscale Wet Etching of Physical-Vapor-Deposited Titanium Nitride and Its Application to Sub-30-nm-Gate-Length Fin-Type Double-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistor Fabrication. Japanese Journal of Applied Physics, 2010, 49, 06GH18.	1.5	27
88	On the gate-stack origin threshold voltage variability in scaled FinFETs and multi-FinFETs. , 2010, , .		32
89	Independent-Double-Gate FINFET SRAM Cell for Drastic Leakage Current Reduction. Lecture Notes in Electrical Engineering, 2010, , 67-79.	0.4	0
90	Enhancing Noise Margins of Fin-Type Field Effect Transistor Static Random Access Memory Cell by Using Threshold Voltage-Controllable Flexible-Pass-Gates. Applied Physics Express, 2009, 2, 054502.	2.4	4

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91	Experimental evaluation of parallel transmission using optical ZCZ-CDMA system. , 2009, , .		2
92	Low Temperature, Beam-Orientation-Dependent, Lattice-Plane-Independent, and Damage-Free Oxidation for Three-Dimensional Structure by Neutral Beam Oxidation. Japanese Journal of Applied Physics, 2009, 48, 04C007.	1.5	21
93	A Comparative Study of Nitrogen Gas Flow Ratio Dependence on the Electrical Characteristics of Sputtered Titanium Nitride Gate Bulk Planar Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors and Fin-Type Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2009, 48, 05DC01.	1.5	23
94	Vertical ultrathinâ€channel multiâ€gate MOSFETs (MuGFETs): technological challenges and future developments. IEEJ Transactions on Electrical and Electronic Engineering, 2009, 4, 386-391.	1.4	2
95	Dual metal gate FinFET integration by Ta/Mo diffusion technology for Vt reduction and multi-Vt CMOS application. Solid-State Electronics, 2009, 53, 701-705.	1.4	3
96	Fluctuation Analysis of Parasitic Resistance in FinFETs With Scaled Fin Thickness. IEEE Electron Device Letters, 2009, 30, 407-409.	3.9	23
97	Metal-Gate FinFET Variation Analysis by Measurement and Compact Model. IEEE Electron Device Letters, 2009, 30, 556-558.	3.9	11
98	Independent-Double-Gate FinFET SRAM for Leakage Current Reduction. IEEE Electron Device Letters, 2009, 30, 757-759.	3.9	24
99	Vertical doubleâ€gate MOSFET device technology. Electronics and Communications in Japan, 2008, 91, 46-51.	0.5	4
100	Flex-pass-gate SRAM for static noise margin enhancement using FinFET-based technology. Solid-State Electronics, 2008, 52, 1694-1702.	1.4	1
101	Threshold-Voltage Reduction of FinFETs by Ta/Mo Interdiffusion Dual Metal-Gate Technology for Low-Operating-Power Application. IEEE Transactions on Electron Devices, 2008, 55, 2454-2461.	3.0	12
102	Independent-gate four-terminal FinFET SRAM for drastic leakage current reduction. , 2008, , .		1
103	Enhancing SRAM cell performance by using independent double-gate FinFET. , 2008, , .		30
104	Dual metal gate FinFET integration by Ta/Mo diffusion technology for Vt reduction and multi-Vt CMOS application. , 2008, , .		8
105	Variable-Threshold-Voltage FinFETs with a Control-Voltage Range within the Logic-Level Swing Using Asymmetric Work-Function Double Gates. International Power Modulator Symposium and High-Voltage Workshop, 2008, , .	0.0	0
106	Enhancing noise margins of FinFET SRAM by integrating V<inf>th</inf>-controllable flexible-pass-gates. , 2008, , .		3
107	Logic gate threshold voltage controllable single metal gate FinFET CMOS inverters implemented by using co-integration of 3T/4T-FinFETs. , 2008, , .		2
108	Impact of extension and source/drain resistance on FinFET performance. , 2008, , .		6

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109	A Ta/Mo Interdiffusion Dual Metal Gate Technology for Drivability Enhancement of FinFETs. IEEE Electron Device Letters, 2008, 29, 618-620.	3.9	9
110	Dual-Metal-Gate Transistors with Symmetrical Threshold Voltages Using Work-Function-Tuned Ta/Mo Bilayer Metal Gates. Japanese Journal of Applied Physics, 2008, 47, 2428-2432.	1.5	4
111	Nitrogen Gas Flow Ratio and Rapid Thermal Annealing Temperature Dependences of Sputtered Titanium Nitride Gate Work Function and Their Effect on Device Characteristics. Japanese Journal of Applied Physics, 2008, 47, 2433.	1.5	20
112	Static Noise Margin Enhancement by Flex-Pass-Gate SRAM. IEEJ Transactions on Electronics, Information and Systems, 2008, 128, 919-925.	0.2	0
113	FinFET-Based Flex-Vth SRAM Design for Drastic Standby-Leakage-Current Reduction. IEICE Transactions on Electronics, 2008, E91-C, 534-542.	0.6	2
114	Ta/Mo Stack Dual Metal Gate Technology Applicable to Gate-First Processes. Japanese Journal of Applied Physics, 2007, 46, 1825-1829.	1.5	4
115	Flex-Pass-Gate SRAM Design for Static Noise Margin Enhancement Using FinFET-Based Technology. , 2007, , .		13
116	Experimental Evaluation of Effects of Channel Doping on Characteristics of FinFETs. IEEE Electron Device Letters, 2007, 28, 1123-1125.	3.9	28
117	Cointegration of High-Performance Tied-Gate Three-Terminal FinFETs and Variable Threshold-Voltage Independent-Gate Four-Terminal FinFETs With Asymmetric Gate-Oxide Thicknesses. IEEE Electron Device Letters, 2007, 28, 517-519.	3.9	48
118	A Dynamical Power-Management Demonstration Using Four-Terminal Separated-Gate FinFETs. IEEE Electron Device Letters, 2007, 28, 452-454.	3.9	9
119	Four-Terminal FinFETs Fabricated Using an Etch-Back Gate Separation. IEEE Nanotechnology Magazine, 2007, 6, 201-205.	2.0	18
120	A novel approach to Au nanoparticle-based identification of DNA nanoarrays. Frontiers in Bioscience - Landmark, 2007, 12, 4773.	3.0	3
121	Investigation of the TiN Gate Electrode With Tunable Work Function and Its Application for FinFET Fabrication. IEEE Nanotechnology Magazine, 2006, 5, 723-730.	2.0	90
122	Fabrication of FinFETs by Damage-Free Neutral-Beam Etching Technology. IEEE Transactions on Electron Devices, 2006, 53, 1826-1833.	3.0	37
123	Investigation of N-Channel Triple-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors on (100) Silicon On Insulator Substrate. Japanese Journal of Applied Physics, 2006, 45, 3097-3100.	1.5	8
124	Demonstration and Analysis of Accumulation-Mode Double-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistor. Japanese Journal of Applied Physics, 2006, 45, 3079-3083.	1.5	5
125	Experimental Study of Effective Carrier Mobility of Multi-Fin-Type Double-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors with (111) Channel Surface Fabricated by Orientation-Dependent Wet Etching. Japanese Journal of Applied Physics, 2006, 45, 3084-3087.	1.5	18
126	New Fabrication Technology of Fin Field Effect Transistors Using Neutral-Beam Etching. Japanese Journal of Applied Physics, 2006, 45, 5513-5516.	1.5	5

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127	Fabrication of a Vertical-Channel Double-Gate Metal-Oxide-Semiconductor Field-Effect Transistor Using a Neutral Beam Etching. Japanese Journal of Applied Physics, 2006, 45, L279-L281.	1.5	9
128	Doping integrity diagnostics of planar transistor channel structures by scanning nonlinear dielectric microscopy. Journal of Vacuum Science & Technology B, 2006, 24, 237.	1.3	0
129	Advanced FinFET CMOS Technology: TiN-Gate, Fin-Height Control and Asymmetric Gate Insulator Thickness 4T-FinFETs. , 2006, , .		28
130	Fabrication and characterization of vertical-type double-gate metal-oxide-semiconductor field-effect transistor with ultrathin Si channel and self-aligned source and drain. Applied Physics Letters, 2006, 88, 072103.	3.3	7
131	Work function controllability of metal gates made by interdiffusing metal stacks with low and high work functions. Microelectronic Engineering, 2005, 80, 284-287.	2.4	12
132	Fabrication of HfC-Coated Si Field Emitter Arrays with Built-in Poly-Si Thin-Film Transistor. Japanese Journal of Applied Physics, 2005, 44, 5740-5743.	1.5	5
133	Device Design Consideration forVth-Controllable Four-Terminal Double-Gate Metal-Oxide-Semiconductor Field-Effect Transistor. Japanese Journal of Applied Physics, 2005, 44, 2351-2356.	1.5	1
134	Demonstration of Dopant Profiling in Ultrathin Channels of Vertical-Type Double-Gate Metal-Oxide-Semiconductor Field-Effect-Transistor by Scanning Nonlinear Dielectric Microscopy. Japanese Journal of Applied Physics, 2005, 44, 2400-2404.	1.5	2
135	Scanning tunneling microscopy observations of hafnium carbide thin films as a field emission material. Journal of Vacuum Science & Technology an Official Journal of the American Vacuum Society B, Microelectronics Processing and Phenomena, 2005, 23, 741.	1.6	7
136	Work function uniformity of Alâ€“Ni alloys obtained by scanning Maxwell-stress microscopy as an effective tool for evaluating metal transistor gates. Applied Physics Letters, 2005, 86, 094104.	3.3	9
137	Fabrication and characterization of vertical-type, self-aligned asymmetric double-gate metal-oxide-semiconductor field-effect-transistors. Applied Physics Letters, 2005, 86, 123512.	3.3	9
138	P-Channel Vertical Double-Gate MOSFET Fabricated by Utilizing Ion-Bombardment-Retarded Etching Processs. Japanese Journal of Applied Physics, 2004, 43, 2156-2159.	1.5	2
139	Fabrication of Polycrystalline Silicon Field Emitter Arrays with Hafnium Carbide Coating for Thin-Film-Transistor Controlled Field Emission Displays. Japanese Journal of Applied Physics, 2004, 43, 3919-3922.	1.5	15
140	Dopant profiling in vertical ultrathin channels of double-gate metalâ€“oxideâ€“semiconductor field-effect transistors by using scanning nonlinear dielectric microscopy. Applied Physics Letters, 2004, 85, 4139-4141.	3.3	22
141	Diagnostics of doping integrity in n+/p/n+ transistor-channel structure by scanning nonlinear dielectric microscopy. Applied Physics Letters, 2004, 84, 3169-3171.	3.3	6
142	Doping diagnosis by evaluation of the surface Fermi level using scanning Maxwell-stress microscopy. Applied Physics Letters, 2003, 82, 2166-2168.	3.3	3
143	Programmable Conductivity of Silicon Nanowires with Side Gates by Surface Charging. Japanese Journal of Applied Physics, 2003, 42, 2422-2425.	1.5	1
144	Fabrication of ultrathin Si Channel Wall For Vertical Double-Gate Metal-Oxide-Semiconductor Field-Effect Transistor (DG MOSFET) by Using Ion-Bombardment-Retarded Etching (IBRE). Japanese Journal of Applied Physics, 2003, 42, 1916-1918.	1.5	13

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145	Novel Process for Vertical Double-Gate (DG) Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) Fabrication. Japanese Journal of Applied Physics, 2003, 42, 4138-4141.	1.5	7
146	Silicon nanowire with programmable conductivity analyzed by scanning Maxwell-stress microscopy. Journal of Vacuum Science & Technology an Official Journal of the American Vacuum Society B, Microelectronics Processing and Phenomena, 2003, 21, 664.	1.6	3
147	Metalâ€“oxideâ€“semiconductor field-effect transistor-structured Si field emitter array with a built-in ring gate lens. Journal of Vacuum Science & Technology an Official Journal of the American Vacuum Society B, Microelectronics Processing and Phenomena, 2003, 21, 495.	1.6	3
148	Fabrication and characterization of HfC coated Si field emitter arrays. Journal of Vacuum Science & Technology an Official Journal of the American Vacuum Society B, Microelectronics Processing and Phenomena, 2003, 21, 1589.	1.6	51
149	Emission uniformity improvement of Si field emitter arrays by surface modification. Journal of Vacuum Science & Technology an Official Journal of the American Vacuum Society B, Microelectronics Processing and Phenomena, 2003, 21, 1581.	1.6	17
150	Mechanism of Tungsten Plug Corrosion during Chemical Stripping Process: Scanning Maxwell-Stress Microscopy and Electrochemical Potentiometry Studies. Japanese Journal of Applied Physics, 2002, 41, 5108-5112.	1.5	4
151	Fabrication of Si field emitter arrays integrated with metalâ€“oxideâ€“semiconductor field-effect transistor driving circuits. Journal of Vacuum Science & Technology an Official Journal of the American Vacuum Society B, Microelectronics Processing and Phenomena, 2002, 20, 2309.	1.6	24
152	Damageless vacuum sealing of Si field emitters with CHF[sub 3] plasma treatment. Journal of Vacuum Science & Technology an Official Journal of the American Vacuum Society B, Microelectronics Processing and Phenomena, 2001, 19, 920.	1.6	13
153	High-temperature real-time observation of surface defects induced by single ion irradiation using scanning-tunneling-microscope/ion-gun combined system. Journal of Vacuum Science & Technology an Official Journal of the American Vacuum Society B, Microelectronics Processing and Phenomena, 2001, 19, 1989.	1.6	9
154	Emission-uniformity improvement and work-function reduction of Si emitter tips by ethylene gas exposure. Journal of Vacuum Science & Technology an Official Journal of the American Vacuum Society B, Microelectronics Processing and Phenomena, 2001, 19, 1911.	1.6	9
155	Charging Damage of Silicon-on-Insulator (SOI) Wafer Determined by Scanning Maxwell-Stress Microscopy. Japanese Journal of Applied Physics, 2001, 40, 2907-2910.	1.5	2
156	Novel Process for High-Density Buried Nanopyramid Array Fabrication by Means of Dopant Ion Implantation and Wet Etching. Japanese Journal of Applied Physics, 2001, 40, 2837-2839.	1.5	18
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