Chung-Kuan Cheng

List of Publications by Year
in descending order

141	1,378	516710 16	501196 28
papers	citations	h-index	g-index

141	141	141	596
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	PROBE2.0: A Systematic Framework for Routability Assessment From Technology to Design in Advanced Nodes. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1495-1508.	2.7	7
2	Detection of Chronic Blast-Related Mild Traumatic Brain Injury with Diffusion Tensor Imaging and Support Vector Machines. Diagnostics, 2022, 12, 987.	2.6	6
3	Machine Learning Prediction for Design and System Technology Co-Optimization Sensitivity Analysis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 1059-1072.	3.1	2
4	Monolithic 3D Semiconductor Footprint Scaling Exploration Based on VFET Standard Cell Layout Methodology, Design Flow, and EDA Platform. IEEE Access, 2022, 10, 65971-65981.	4.2	3
5	SP&R: SMT-Based Simultaneous Place-and-Route for Standard Cell Synthesis of Advanced Nodes. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2142-2155.	2.7	10
6	SAT-Based On-Track Bus Routing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 735-747.	2.7	3
7	SMT-Based Contention-Free Task Mapping and Scheduling on SMART NoC. IEEE Embedded Systems Letters, 2021, 13, 158-161.	1.9	4
8	Arnoldi Algorithms with Structured Orthogonalization. SIAM Journal on Numerical Analysis, 2021, 59, 370-400.	2.3	0
9	GRA-LPO. , 2021, , .		6
10	Complementary-FET (CFET) Standard Cell Synthesis Framework for Design and System Technology Co-Optimization Using SMT. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1178-1191.	3.1	22
11	Many-Tier Vertical Gate-All-Around Nanowire FET Standard Cell Synthesis for Advanced Technology Nodes. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2021, 7, 52-60.	1.5	3
12	Multirow Complementary-FET (CFET) Standard Cell Synthesis Framework Using Satisfiability Modulo Theories (SMTs). IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2021, 7, 43-51.	1.5	5
13	Restingâ€state magnetoencephalography source magnitude imaging with deepâ€learning neural network for classification of symptomatic combatâ€related mild traumatic brain injury. Human Brain Mapping, 2021, 42, 1987-2004.	3.6	5
14	CoRe-ECO: Concurrent Refinement of Detailed Place-and-Route for an Efficient ECO Automation. , 2021, , .		2
15	Design and System Technology Co-Optimization Sensitivity Prediction for VLSI Technology Development using Machine Learning. , 2021, , .		2
16	Marked Increases in Resting-State MEG Gamma-Band Activity in Combat-Related Mild Traumatic Brain Injury. Cerebral Cortex, 2020, 30, 283-295.	2.9	24
17	A Parallel-in-Time Circuit Simulator for Power Delivery Networks with Nonlinear Load Models. , 2020, , .		1
18	Standard-Cell Scaling Framework with Guaranteed Pin-Accessibility. , 2020, , .		4

#	Article	IF	Citations
19	SP&R: Simultaneous Placement and Routing framework for standard cell synthesis in sub-7nm. , 2020, , .		11
20	Stability and Convergency Exploration of Matrix Exponential Integration on Power Delivery Network Transient Simulation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2735-2748.	2.7	4
21	Grid-Based Framework for Routability Analysis and Diagnosis With Conditional Design Rules. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 5097-5110.	2.7	11
22	A routability-driven complimentary-FET (CFET) standard cell synthesis framework using SMT. , 2020, , .		9
23	RePlAce: Advancing Solution Quality and Routability Validation in Global Placement. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1717-1730.	2.7	82
24	MEG Working Memory N-Back Task Reveals Functional Deficits in Combat-Related Mild Traumatic Brain Injury. Cerebral Cortex, 2019, 29, 1953-1968.	2.9	18
25	ROAD. , 2019, , .		10
26	Transient circuit simulation for differential algebraic systems using matrix exponential. , 2018, , .		5
27	Fast and precise routability analysis with conditional design rules. , 2018, , .		15
28	Exploring the exponential integrators with Krylov subspace algorithms for nonlinear circuit simulation. , 2017, , .		3
29	From Circuit Theory, Simulation to SPICE^{Diego}: A Matrix Exponential Approach for Time-Domain Analysis of Large-Scale Circuits. IEEE Circuits and Systems Magazine, 2016, 16, 16-34.	2.3	13
30	ePlace-3D. , 2016, , .		28
31	A fast timeâ€domain EMâ€“TCAD coupled simulation framework via matrix exponential with stiffness reduction. International Journal of Circuit Theory and Applications, 2016, 44, 833-850.	2.0	0
32	An Efficient Transient Electro-Thermal Simulation Framework for Power Integrated Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 832-843.	2.7	13
33	Simulation Algorithms With Exponential Integration for Time-Domain Analysis of Large-Scale Power Delivery Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1681-1694.	2.7	19
34	Dynamic analysis of power delivery network with nonlinear components using matrix exponential method. , 2015, , .		2
35	ePlace. ACM Transactions on Design Automation of Electronic Systems, 2015, 20, 1-34.	2.6	71
36	ePlace-MS: Electrostatics-Based Placement for Mixed-Size Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 685-698.	2.7	61

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37	Developing an EEG-based on-line closed-loop lapse detection and mitigation system. Frontiers in Neuroscience, 2014, 8, 321.	2.8	31
38	MATEX: A distributed framework for transient simulation of power distribution networks. , 2014, , .		0
39	ePlace. , 2014, , .		30
40	Ratio of the Worst Case Noise and the Impedance of Power Distribution Network. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2014, 4, 1325-1334.	2.5	0
41	Worst Case Noise Prediction With Nonzero Current Transition Times for Power Grid Planning. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 607-620.	3.1	0
42	Energy Efficiency Optimization Through Codesign of the Transmitter and Receiver in High-Speed On-Chip Interconnects. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 938-942.	3.1	10
43	Study of visual stimulus waveforms via forced van der Pol oscillator model for SSVEP-based brain-computer interfaces. , 2013, , .		0
44	Layer minimization in escape routing for staggered-pin-array PCBs. , 2013, , .		2
45	Performance-driven placement for design of rotation and right arithmetic shifters in monolithic 3D ICs. , 2013, , .		5
46	FFTPL: An analytic placement algorithm using fast fourier transform for density equalization. , 2013, , .		0
47	Modeling and Analysis of Power Distribution Networks in 3-D ICs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 354-366.	3.1	9
48	Novel Differential-Mode Equalizer With Broadband Common-Mode Filtering for Gb/s Differential-Signal Transmission. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2013, 3, 1578-1587.	2.5	16
49	Minimizing the worst-case voltage noise for power distribution network using time-varying equivalent serial resistance. , 2013, , .		0
50	Power grid simulation using matrix exponential method with rational Krylov subspaces. , 2013, , .		16
51	A Practical Regularization Technique for Modified Nodal Analysis in Large-Scale Time-Domain Circuit Simulation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1031-1040.	2.7	27
52	Time-Domain Analysis of Large-Scale Circuits by Matrix Exponential Method With Adaptive Control. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1180-1193.	2.7	31
53	Cell-phone based Drowsiness Monitoring and Management system. , 2012, , .		8
54	Eye prediction of digital driver with power distribution network noise. , 2012, , .		7

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55	Ultra-low power on-chip differential interconnects using high-resolution comparator. , 2012, , .		1
56	A Realistic Early-Stage Power Grid Verification Algorithm Based on Hierarchical Constraints. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 109-120.	2.7	14
57	A block-diagonal structured model reduction scheme for power grid networks. , 2011, , .		15
58	Circuit simulation using matrix exponential method. , 2011, , .		4
59	Analysis and Optimization of Low-Power Passive Equalizers for CPUâ€“Memory Links. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2011, 1, 1406-1420.	2.5	6
60	On-Chip Interconnect Analysis of Performance and Energy Metrics Under Different Design Goals. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 520-524.	3.1	7
61	Prediction and Comparison of High-Performance On-Chip Global Interconnection. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1154-1166.	3.1	14
62	Bus Matrix Synthesis Based on Steiner Graphs for Power Efficient System-on-Chip Communications. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 167-179.	2.7	1
63	A fast and stable explicit integration method by matrix exponential operator for large scale circuit simulation. , 2011, , .		5
64	High-speed and low-power on-chip global link using continuous-time linear equalizer. , 2010, , .		6
65	Efficient Power Network Analysis with Modeling of Inductive Effects. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2010, E93-A, 1196-1203.	0.3	2
66	Accurate Eye Diagram Prediction Based on Step Response and Its Aication to Low-Power Equalizer Design. IEICE Transactions on Electronics, 2009, E92-C, 444-452.	0.6	15
67	Parallel transistor level circuit simulation using domain decomposition methods. , 2009, , .		15
68	Enhancing Learning Effectiveness in Digital Design Courses Through the Use of Programmable Logic Boards. IEEE Transactions on Education, 2009, 52, 151-156.	2.4	37
69	Efficient power network analysis with complete inductive modeling. , 2009, , .		1
70	Parallel transistor level full-chip circuit simulation. , 2009, , .		6
71	Symmetrical buffer placement in clock trees for minimal skew immune to global on-chip variations. , 2009, , .		1
72	Efficient Partial Reluctance Extraction for Large-Scale Regular Power Grid Structures. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2009, E92-A, 1476-1484.	0.3	4

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73	Timing-power optimization for mixed-radix Ling adders by integer linear programming. , 2008, , .		1
74	Digital design and programmable logic boards: Do students actually learn more?. , 2008, , .		8
75	A novel fixed-outline floorplanner with zero deadspace for hierarchical design. , 2008, , .		5
76	Efficient frequency-dependent reluctance extraction for large-scale Power/Ground grid. , 2008, , .		1
77	High performance current-mode differential logic. , 2008, , .		0
78	Efficient and accurate eye diagram prediction for high speed signaling. , 2008, , .		30
79	Incremental Power Impedance Optimization Using Vector Fitting Modeling. , 2007, , .		2
80	Fast Transient Simulation of Lossy Transmission Lines. , 2007, , .		2
81	Efficient Thermal via Planning Approach and Its Application in 3-D Floorplanning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 645-658.	2.7	32
82	Exploring Cardioneural Signals from Noninvasive ECG Measurement. , 2007, , .		2
83	Optimum Prefix Adders in a Comprehensive Area, Timing and Power Design Space. , 2007, , .		20
84	Passive compensation for high performance inter-chip communication. , 2007, , .		1
85	Efficient timing analysis with known false paths using biclique covering. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 959-969.	2.7	0
86	Two-stage newtonâ€“raphson method for transistor-level simulation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 881-895.	2.7	2
87	Communication latency aware low power NoC synthesis. Proceedings - Design Automation Conference, 2006, , .	0.0	0
88	Noninvasive Study of the Human Heart using Independent Component Analysis. , 2006, , .		5
89	Layer Minimization of Escape Routing in Area Array Packaging. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	3
90	Corner Block List Representation and Its Application to Floorplan Optimization. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2004, 51, 228-233.	2.2	49

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91	Fast postplacement optimization using functional symmetries. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2004, 23, 102-118.	2.7	13
92	UTACO: A Unified Timing and Congestion Optimization Algorithm for Standard Cell Global Routing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2004, 23, 358-365.	2.7	8
93	Area Minimization of Power Distribution Network Using Efficient Nonlinear Programming Techniques. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2004, 23, 1086-1094.	2.7	59
94	An algorithmic approach for generic parallel adders. , 2003, , .		1
95	Reduced Order Modeling for RLC Interconnect Tree Using Hurwitz Polynomial. Analog Integrated Circuits and Signal Processing, 2002, 31, 193-208.	1.4	3
96	Empirical Study of Block Placement by Cluster Refinement. VLSI Design, 1999, 10, 71-86.	0.5	0
97	Timing optimization for multisource nets: characterization and optimal repeater insertion. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1999, 18, 322-331.	2.7	18
98	Routability improvement using dynamic interconnect architecture. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 1998, 6, 498-501.	3.1	4
99	Data flow partitioning with clock period and latency constraints. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 1997, 44, 210-220.	0.1	3
100	TIGER: an efficient timing-driven global router for gate array and standard cell layout design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1997, 16, 1323-1331.	2.7	36
101	A global router with a theoretical bound on the optimal solution. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1996, 15, 208-216.	2.7	56
102	A wire length estimation technique utilizing neighborhood density equations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1996, 15, 912-922.	2.7	18
103	EARLY FEASIBILITY AND COST ASSESSMENT FOR MULTICHIP MODULE TECHNOLOGIES. Selected Topics in Electornics and Systems, 1996, , 25-42.	0.2	0
104	EARLY FEASIBILITY AND COST ASSESSMENT FOR MULTICHIP MODULE TECHNOLOGIES. International Journal of High Speed Electronics and Systems, 1995, 06, 441-458.	0.7	1
105	Skew Sensitivity Minimization Of Buffered Clock Tree. , 0, , .		3
106	Finite state machine decomposition for I/O minimization. , 0, , .		6
107	Performance driven multiple-source bus synthesis using buffer insertion. , 0, , .		0
108	Optimal and efficient buffer insertion and wire sizing. , 0, , .		32

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109	New spectral linear placement and clustering approach. , 0, , .		8
110	Network partitioning into tree hierarchies. , 0, , .		0
111	Cluster Refinement For Block Placement. , 0, , .		0
112	A new layout-driven timing model for incremental layout optimization. , 0, , .		4
113	Design and implementation of a global router based on a new layout-driven timing model with three poles. , 0, , .		3
114	Extending moment computation to 2-port circuit representations. , 0, , .		0
115	RLC interconnect delay estimation via moments of amplitude and phase response. , 0, , .		2
116	A non-slicing floorplanning algorithm using corner block list topological representation. , 0, , .		7
117	Corner block list: an effective and efficient topological representation of non-slicing floorplan. , 0, , .		49
118	A new efficient waveform simulation method for RLC interconnect via amplitude and phase approximation. , 0, , .		0
119	VLSI floorplanning with boundary constraints based on corner block list. , 0, , .		1
120	A compact algorithm for placement design using corner block list representation. , 0, , .		0
121	Module placement with boundary constraints using O-tree representation. , 0, , .		1
122	Balancing the interconnect topology for arrays of processors between cost and power. , 0, , .		1
123	Stairway compaction using corner block list and its applications with rectilinear blocks. , 0, , .		0
124	Physical planning of on-chip interconnect architectures. , 0, , .		6
125	Arbitrary convex and concave rectilinear block packing based on corner block list. , 0, , .		4
126	A buffer planning algorithm based on dead space redistribution. , 0, , .		2

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127	Evaluating a bounded slice-line grid assignment in O(nlogn) time. , 0, , .		2
128	The Y-architecture: yet another on-chip interconnect solution. , 0, , .		3
129	RCLK-VJ network reduction with Hurwitz polynomial approximation. , 0, , .		0
130	Buffer allocation algorithm with consideration of routing congestion. , 0, , .		0
131	A buffer planning algorithm with congestion optimization. , 0, , .		0
132	A mulitple level network approach for clock skew minimization with process variations. , 0, , .		10
133	A multi-level transmission line network approach for multi-giga hertz clock distribution. , 0, , .		0
134	Floorplanning with Consideration of White Space Resource Distribution for Repeater Planning. , 0, , .		2
135	VLSI Block Placement with Alignment Constraints based on Corner Block List. , 0, , .		1
136	Efficient transient simulation for transistor-level analysis. , 0, , .		0
137	Buffer Planning Algorithm Based on Partial Clustered Floorplanning. , 0, , .		0
138	Integrated algorithmic logical and physical design of integer multiplier. , 0, , .		0
139	Physical synthesis of energy-efficient networks-on-chip through topology exploration and wire style optimization. , 0, , .		17
140	An unconditional stable general operator splitting method for transistor level. , 0, , .		0
141	Floorplanning with abutment constraints and L-shaped/T-shaped blocks based on corner block list. , 0, , .		1