Seongwook Park

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/7008043/publications.pdf

Version: 2024-02-01

29	238	1040056	1474206
papers	citations	9	9
		h-index	g-index

29	29	29	240
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A 34pJ/level pixel depth-estimation processor with shifter-based pipelined architecture for mobile user interface. , 2016, , .		0
2	An Energy-Efficient Embedded Deep Neural Network Processor for High Speed Visual Attention in Mobile Vision Recognition SoC. IEEE Journal of Solid-State Circuits, 2016, , 1-9.	5.4	14
3	An energy-efficient parallel multi-core ADAS processor with robust visual attention and workload-prediction DVFS for real-time HD stereo stream. , 2016, , .		1
4	An 8.3mW 1.6Msamples/s multi-modal event-driven speech enhancement processor for robust speech recognition in smart glasses. , 2016, , .		1
5	Low-power real-time intelligent SoCs for smart machines. , 2016, , .		0
6	A 0.5 V 54 Ultra-Low-Power Object Matching Processor for Micro Air Vehicle Navigation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 359-369.	5.4	10
7	A 2.71 nJ/Pixel Gaze-Activated Object Recognition System for Low-Power Mobile Smart Glasses. IEEE Journal of Solid-State Circuits, 2016, 51, 45-55.	5.4	15
8	A Vocabulary Forest Object Matching Processor With 2.07 M-Vector/s Throughput and 13.3 nJ/Vector Per-Vector Energy for Full-HD 60 fps Video Object Recognition. IEEE Journal of Solid-State Circuits, 2015, 50, 1059-1069.	5.4	14
9	A 1.9nJ/pixel embedded deep neural network processor for high speed visual attention in a mobile vision recognition SoC. , 2015, , .		2
10	An Impedance and Multi-Wavelength Near-Infrared Spectroscopy IC for Non-Invasive Blood Glucose Estimation. IEEE Journal of Solid-State Circuits, 2015, 50, 1025-1037.	5.4	75
11	A keypoint-level parallel pipelined object recognition processor with gaze activation image sensor for mobile smart glasses system. , 2015, , .		1
12	A 1.22 TOPS and 1.52 mW/MHz Augmented Reality Multicore Processor With Neural Network NoC for HMD Applications. IEEE Journal of Solid-State Circuits, 2015, 50, 113-124.	5.4	24
13	Intelligent Network-on-Chip With Online Reinforcement Learning for Portable HD Object Recognition Processor. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 476-484.	5.4	11
14	A 1.5nJ/pixel super-resolution enhanced FAST corner detection processor for high accuracy AR. , 2014, , .		3
15	A task-level pipelined many-SIMD augmented reality processor with congestion-aware network-on-chip scheduler. , 2014, , .		1
16	A 320 mW 342 GOPS Real-Time Dynamic Object Recognition Processor for HD 720p Video Streams. IEEE Journal of Solid-State Circuits, 2013, 48, 33-45.	5.4	23
17	A multi-modal and tunable Radial-Basis-Funtion circuit with supply and temperature compensation. , 2013, , .		2
18	A 34.1fps scale-space processor with two-dimensional cache for real-time object recognition. , 2013, , .		0

#	Article	IF	Citations
19	A 32.8mW 60fps cortical vision processor for spatio-temporal action recognition. , 2013, , .		0
20	A high-throughput 16× super resolution processor for real-time object recognition SoC. , 2013, , .		1
21	A dynamic resource controller with network-on-chip for a 10.5nJ/pixel object recognition processor. , 2012, , .		0
22	Online Reinforcement Learning NoC for portable HD object recognition processor. , 2012, , .		1
23	A simultaneous multithreading heterogeneous object recognition processor with machine learning based dynamic resource management. , 2012, , .		0
24	A 92-mW Real-Time Traffic Sign Recognition System With Robust Illumination Adaptation and Support Vector Machine. IEEE Journal of Solid-State Circuits, 2012, 47, 2711-2723.	5.4	11
25	A 92mW real-time traffic sign recognition system with robust light and dark adaptation. , 2011, , .		6
26	A low-energy hybrid radix-4/-8 multiplier for portable multimedia applications. , 2011, , .		0
27	A 30fps stereo matching processor based on belief propagation with disparity-parallel PE array architecture. , 2010, , .		10
28	Intelligent NoC with neuro-fuzzy bandwidth regulation for a 51 IP object recognition processor. , 2010, , .		6
29	A 92m W 76.8GOPS vector matching processor with parallel Huffman decoder and query re-ordering buffer for real-time object recognition. , 2010, , .		6