# Shin-ichi O'uchi

List of Publications by Year
in descending order

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| 98 | 952 | 567281 15 | 580821 25 |
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| papers | citations | h-index | g-index |

| 98 | 98 | 98 | 758 |
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| all docs | docs citations | times ranked | citing authors |

| # | Article | IF | Citations |
|---|---|---|---|
| 1 | Fully Integrated, 100-mV Minimum Input Voltage Converter With Gate-Boosted Charge Pump Kick-Started by LC Oscillator for Energy Harvesting. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 392-396. | 3.0 | 40 |
| 2 | Structural and electrical characterization of epitaxial Ge thin films on Si(001) formed by sputtering. Japanese Journal of Applied Physics, 2017, 56, 04CB01. | 1.5 | 0 |
| 3 | A Closed-Form Expression for Minimum Operating Voltage of CMOS D Flip-Flop. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2007-2016. | 3.1 | 4 |
| 4 | Tunnel FinFET CMOS inverter with very low short-circuit current for ultralow-power Internet of Things application. Japanese Journal of Applied Physics, 2017, 56, 04CD19. | 1.5 | 15 |
| 5 | Impact of residual defects caused by extension ion implantation in FinFETs on parasitic resistance and its fluctuation. Solid-State Electronics, 2017, 132, 103-108. | 1.4 | 3 |
| 6 | Bias temperature instability in tunnel field-effect transistors. Japanese Journal of Applied Physics, 2017, 56, 04CA04. | 1.5 | 2 |
| 7 | A 0.3-V 1- $mu ext{W}$ Super-Regenerative Ultrasound Wake-Up Receiver With Power Scalability. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1027-1031. | 3.0 | 22 |
| 8 | Epitaxial growth of Ge thin film on Si (001) by DC magnetron sputtering. Materials Science in Semiconductor Processing, 2017, 70, 3-7. | 4.0 | 4 |
| 9 | Suppression of tunneling rate fluctuations in tunnel field-effect transistors by enhancing tunneling probability. Japanese Journal of Applied Physics, 2017, 56, 04CD02. | 1.5 | 5 |
| 10 | Impact of extension implantation conditions of fin field-effect transistors on gate-induced drain leakage. Japanese Journal of Applied Physics, 2016, 55, 04EB01. | 1.5 | 3 |
| 11 | (Invited) Floating Gate Type SOI-FinFET Flash Memories with Different Channel Shapes and Interpoly Dielectric Materials. ECS Transactions, 2016, 72, 11-24. | 0.5 | 1 |
| 12 | Introduction of SiGe/Si heterojunction into novel multilayer tunnel FinFET. Japanese Journal of Applied Physics, 2016, 55, 04EB06. | 1.5 | 15 |
| 13 | Closed-form analytical model of static noise margin for ultra-low voltage eight-transistor tunnel FET static random access memory. Japanese Journal of Applied Physics, 2016, 55, 04ED06. | 1.5 | 4 |
| 14 | Robust and compact key generator using physically unclonable function based on logic-transistor-compatible poly-crystalline-Si channel FinFET technology. , 2015, , . | | 5 |
| 15 | Heated ion implantation for high-performance and highly reliable silicon-on-insulator complementary metalâ€“oxideâ€“silicon fin field-effect transistors. Japanese Journal of Applied Physics, 2015, 54, 04DA06. | 1.5 | 4 |
| 16 | Impact of granular work function variation in a gate electrode on low-frequency noise for fin field-effect transistors. Applied Physics Express, 2015, 8, 044201. | 2.4 | 7 |
| 17 | Impact of fin length on threshold voltage modulation by back bias for Independent double-gate tunnel fin field-effect transistors. Solid-State Electronics, 2015, 111, 62-66. | 1.4 | 3 |
| 18 | Highly Vt tunable and low variability triangular fin-channel MOSFETs on SOTB. Microelectronic Engineering, 2015, 147, 290-293. | 2.4 | 0 |

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| 19 | Improvement of epitaxial channel quality on heavily arsenic- and boron-doped Si surfaces and impact on performance of tunnel field-effect transistors. Solid-State Electronics, 2015, 113, 173-178. | 1.4 | 6 |
| 20 | Channel shape and interpoly dielectric material effects on electrical characteristics of floating-gate-type three-dimensional fin channel flash memories. Japanese Journal of Applied Physics, 2015, 54, 04DD04. | 1.5 | 2 |
| 21 | Unexpected equivalent-oxide-thickness dependence of the subthreshold swing in tunnel field-effect transistors. Applied Physics Express, 2014, 7, 024201. | 2.4 | 35 |
| 22 | Scaling breakthrough for analog/digital circuits by suppressing variability and low-frequency noise for FinFETs by amorphous metal gate technology. , 2014, , . | | 4 |
| 23 | Influence of work function variation of metal gates on fluctuation of sub-threshold drain current for fin field-effect transistors with undoped channels. Japanese Journal of Applied Physics, 2014, 53, 04EC11. | 1.5 | 12 |
| 24 | Experimental study of three-dimensional fin-channel charge trapping flash memories with titanium nitride and polycrystalline silicon gates. Japanese Journal of Applied Physics, 2014, 53, 04ED16. | 1.5 | 2 |
| 25 | (Invited) Charge Trapping Type SOI-FinFET Flash Memory. ECS Transactions, 2014, 61, 263-280. | 0.5 | 4 |
| 26 | Performance Enhancement of Tunnel Field-Effect Transistors by Synthetic Electric Field Effect. IEEE Electron Device Letters, 2014, 35, 792-794. | 3.9 | 53 |
| 27 | Performance evaluation of parallel electric field tunnel field-effect transistor by a distributed-element circuit model. Solid-State Electronics, 2014, 102, 82-86. | 1.4 | 7 |
| 28 | SOI CMOS Voltage Multiplier Circuits with Body Bias Control Technique for Battery-Less Wireless Sensor System. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2014, E97.A, 741-748. | 0.3 | 0 |
| 29 | 1/fNoise Characteristics of Fin-Type Field-Effect Transistors in Saturation Region. Japanese Journal of Applied Physics, 2013, 52, 04CC23. | 1.5 | 0 |
| 30 | (Invited) Independent-Double-Gate FinFET SRAM Technology. ECS Transactions, 2013, 50, 193-199. | 0.5 | 0 |
| 31 | Gate Structure Dependence of Variability in Polycrystalline Silicon Fin-Channel Flash Memories. Japanese Journal of Applied Physics, 2013, 52, 06GE01. | 1.5 | 3 |
| 32 | Atomic Layer Deposition of SiO<sub>2</sub> for the Performance Enhancement of Fin Field Effect Transistors. Japanese Journal of Applied Physics, 2013, 52, 116503. | 1.5 | 8 |
| 33 | Suppression of threshold voltage variability of double-gate fin field-effect transistors using amorphous metal gate with uniform work function. Applied Physics Letters, 2013, 102, . | 3.3 | 15 |
| 34 | Fabrication of Floating-Gate-Type Fin-Channel Double- and Tri-Gate Flash Memories and Comparative Study of Their Electrical Characteristics. Japanese Journal of Applied Physics, 2012, 51, 04DD03. | 1.5 | 2 |
| 35 | Fabrication and Characterization of NOR-Type Tri-Gate Flash Memory with Improved Inter-Poly Dielectric Layer by Rapid Thermal Oxidation. Japanese Journal of Applied Physics, 2012, 51, 06FE19. | 1.5 | 6 |
| 36 | Experimental Study of Floating-Gate-Type Metalâ€“Oxideâ€“Semiconductor Capacitors with Nanosize Triangular Cross-Sectional Tunnel Areas for Low Operating Voltage Flash Memory Application. Japanese Journal of Applied Physics, 2012, 51, 06FF01. | 1.5 | 2 |

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| 37 | Experimental Comparisons between Tetrakis(dimethylamino)titanium Precursor-Based Atomic-Layer-Deposited and Physical-Vapor-Deposited Titaniumâ€“Nitride Gate for High-Performance Fin-Type Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2012, 51, 04DA05. | 1.5 | 0 |
| 38 | (Invited) FinFET Flash Memory Technology. ECS Transactions, 2012, 45, 289-310. | 0.5 | 2 |
| 39 | (Invited) On-Current Variability Sources of FinFETs: Analysis and Perspective for 14nm-Lg Technology. ECS Transactions, 2012, 45, 231-242. | 0.5 | 0 |
| 40 | Enhancement of FinFET performance using 25-nm-thin sidewall spacer grown by atomic layer deposition. Solid-State Electronics, 2012, 74, 13-18. | 1.4 | 13 |
| 41 | Demonstration of Split-Gate Type Trigate Flash Memory With Highly Suppressed Over-Erase. IEEE Electron Device Letters, 2012, 33, 345-347. | 3.9 | 10 |
| 42 | Variability Origins of Parasitic Resistance in FinFETs With Silicided Source/Drain. IEEE Electron Device Letters, 2012, 33, 474-476. | 3.9 | 15 |
| 43 | Variability Analysis of Scaled Crystal Channel and Poly-Si Channel FinFETs. IEEE Transactions on Electron Devices, 2012, 59, 573-581. | 3.0 | 12 |
| 44 | Fin-Height Effect on Poly-Si/PVD-TiN Stacked-Gate FinFET Performance. IEEE Transactions on Electron Devices, 2012, 59, 647-653. | 3.0 | 14 |
| 45 | A Correlative Analysis Between Characteristics of FinFETs and SRAM Performance. IEEE Transactions on Electron Devices, 2012, 59, 1345-1352. | 3.0 | 3 |
| 46 | Decomposition of On-Current Variability of nMOS FinFETs for Prediction Beyond 20 nm. IEEE Transactions on Electron Devices, 2012, 59, 2003-2010. | 3.0 | 27 |
| 47 | High-Frequency Precise Characterization of Intrinsic FinFET Channel. IEICE Transactions on Electronics, 2012, E95.C, 752-760. | 0.6 | 1 |
| 48 | A 0.7-V Opamp in Scaled Low-Standby-Power FinFET Technology. IEICE Transactions on Electronics, 2012, E95.C, 686-695. | 0.6 | 0 |
| 49 | Experimental Comparisons between Tetrakis(dimethylamino)titanium Precursor-Based Atomic-Layer-Deposited and Physical-Vapor-Deposited Titaniumâ€“Nitride Gate for High-Performance Fin-Type Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2012, 51, 04DA05. | 1.5 | 2 |
| 50 | Variability origins of FinFETs and perspective beyond 20nm node. , 2011, , . | | 3 |
| 51 | Static noise margin enhancement by flex-pass-gate SRAM. Electronics and Communications in Japan, 2011, 94, 57-64. | 0.5 | 0 |
| 52 | Tunnel Field-Effect Transistors with Extremely Low Off-Current Using Shadowing Effect in Drain Implantation. Japanese Journal of Applied Physics, 2011, 50, 06GF14. | 1.5 | 7 |
| 53 | Correlative analysis between characteristics of 30-nm L<inf>G</inf> FinFETs and SRAM performance. , 2011, , . | | 1 |
| 54 | Experimental Study of Physical-Vapor-Deposited Titanium Nitride Gate with An n<sup>+</sup>-Polycrystalline Silicon Capping Layer and Its Application to 20 nm Fin-Type Double-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2011, 50, 04DC14. | 1.5 | 12 |

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| 55 | Design of SOI FinFET on 32nm technology node for low standby power (LSTP) operation considering gate-induced drain leakage (GIDL). Solid-State Electronics, 2010, 54, 1060-1065. | 1.4 | 7 |
| 56 | (Invited) Advanced FinFET Technologies: Extension Doping, Vth Controllable CMOS Inverters and SRAM. ECS Transactions, 2010, 28, 385-401. | 0.5 | 1 |
| 57 | Investigation of Low-Energy Tilted Ion Implantation for Fin-Type Double-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistor Extension Doping. Japanese Journal of Applied Physics, 2010, 49, 04DC18. | 1.5 | 22 |
| 58 | Minimization of Gate-Induced Drain Leakage by Controlling Gate Underlap Length for Low-Standby-Power Operation of 20-nm-Level Four-Terminal Silicon-on-Insulator Fin-Shaped Field Effect Transistor. Japanese Journal of Applied Physics, 2010, 49, 024203. | 1.5 | 0 |
| 59 | Investigation of Thermal Stability of TiN Film Formed by Atomic Layer Deposition Using Tetrakis(dimethylamino)titanium Precursor for Metal-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistor. Japanese Journal of Applied Physics, 2010, 49, 04DA16. | 1.5 | 7 |
| 60 | Variability Analysis of TiN Metal-Gate FinFETs. IEEE Electron Device Letters, 2010, 31, 546-548. | 3.9 | 63 |
| 61 | Variability analysis of TiN FinFET SRAM cell performance and its compensation using Vth-controllable independent double-gate FinFET. , 2010, , . | | 0 |
| 62 | Variability Analysis of TiN FinFET SRAM Cells and Its Compensation by Independent-DG FinFETs. IEEE Electron Device Letters, 2010, 31, 1095-1097. | 3.9 | 4 |
| 63 | Nanoscale Wet Etching of Physical-Vapor-Deposited Titanium Nitride and Its Application to Sub-30-nm-Gate-Length Fin-Type Double-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistor Fabrication. Japanese Journal of Applied Physics, 2010, 49, 06GH18. | 1.5 | 27 |
| 64 | On the gate-stack origin threshold voltage variability in scaled FinFETs and multi-FinFETs. , 2010, , . | | 32 |
| 65 | Rigorous Design of 22-nm Node 4-Terminal SOI FinFETs for Reliable Low Standby Power Operation with Semi-empirical Parameters. Journal of Semiconductor Technology and Science, 2010, 10, 265-275. | 0.4 | 5 |
| 66 | Enhancing Noise Margins of Fin-Type Field Effect Transistor Static Random Access Memory Cell by Using Threshold Voltage-Controllable Flexible-Pass-Gates. Applied Physics Express, 2009, 2, 054502. | 2.4 | 4 |
| 67 | Experimental evaluation of parallel transmission using optical ZCZ-CDMA system. , 2009, , . | | 2 |
| 68 | A Comparative Study of Nitrogen Gas Flow Ratio Dependence on the Electrical Characteristics of Sputtered Titanium Nitride Gate Bulk Planar Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors and Fin-Type Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2009, 48, 05DC01. | 1.5 | 23 |
| 69 | Dual metal gate FinFET integration by Ta/Mo diffusion technology for Vt reduction and multi-Vt CMOS application. Solid-State Electronics, 2009, 53, 701-705. | 1.4 | 3 |
| 70 | Fluctuation Analysis of Parasitic Resistance in FinFETs With Scaled Fin Thickness. IEEE Electron Device Letters, 2009, 30, 407-409. | 3.9 | 23 |
| 71 | Metal-Gate FinFET Variation Analysis by Measurement and Compact Model. IEEE Electron Device Letters, 2009, 30, 556-558. | 3.9 | 11 |
| 72 | Independent-Double-Gate FinFET SRAM for Leakage Current Reduction. IEEE Electron Device Letters, 2009, 30, 757-759. | 3.9 | 24 |

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| 73 | Flex-pass-gate SRAM for static noise margin enhancement using FinFET-based technology. Solid-State Electronics, 2008, 52, 1694-1702. | 1.4 | 1 |
| 74 | Threshold-Voltage Reduction of FinFETs by Ta/Mo Interdiffusion Dual Metal-Gate Technology for Low-Operating-Power Application. IEEE Transactions on Electron Devices, 2008, 55, 2454-2461. | 3.0 | 12 |
| 75 | Independent-gate four-terminal FinFET SRAM for drastic leakage current reduction. , 2008, , . | | 1 |
| 76 | Enhancing SRAM cell performance by using independent double-gate FinFET. , 2008, , . | | 30 |
| 77 | Dual metal gate FinFET integration by Ta/Mo diffusion technology for Vt reduction and multi-Vt CMOS application. , 2008, , . | | 8 |
| 78 | Variable-Threshold-Voltage FinFETs with a Control-Voltage Range within the Logic-Level Swing Using Asymmetric Work-Function Double Gates. International Power Modulator Symposium and High-Voltage Workshop, 2008, , . | 0.0 | 0 |
| 79 | Logic gate threshold voltage controllable single metal gate FinFET CMOS inverters implemented by using co-integration of 3T/4T-FinFETs. , 2008, , . | | 2 |
| 80 | Impact of extension and source/drain resistance on FinFET performance. , 2008, , . | | 6 |
| 81 | A Ta/Mo Interdiffusion Dual Metal Gate Technology for Drivability Enhancement of FinFETs. IEEE Electron Device Letters, 2008, 29, 618-620. | 3.9 | 9 |
| 82 | Static Noise Margin Enhancement by Flex-Pass-Gate SRAM. IEEJ Transactions on Electronics, Information and Systems, 2008, 128, 919-925. | 0.2 | 0 |
| 83 | FinFET-Based Flex-Vth SRAM Design for Drastic Standby-Leakage-Current Reduction. IEICE Transactions on Electronics, 2008, E91-C, 534-542. | 0.6 | 2 |
| 84 | Flex-Pass-Gate SRAM Design for Static Noise Margin Enhancement Using FinFET-Based Technology. , 2007, , . | | 13 |
| 85 | Experimental Evaluation of Effects of Channel Doping on Characteristics of FinFETs. IEEE Electron Device Letters, 2007, 28, 1123-1125. | 3.9 | 28 |
| 86 | Nitrogen gas flow ratio controlled PVD TiN metal gate technology for FinFET CMOS. , 2007, , . | | 0 |
| 87 | Cointegration of High-Performance Tied-Gate Three-Terminal FinFETs and Variable Threshold-Voltage Independent-Gate Four-Terminal FinFETs With Asymmetric Gate-Oxide Thicknesses. IEEE Electron Device Letters, 2007, 28, 517-519. | 3.9 | 48 |
| 88 | A Dynamical Power-Management Demonstration Using Four-Terminal Separated-Gate FinFETs. IEEE Electron Device Letters, 2007, 28, 452-454. | 3.9 | 9 |
| 89 | Four-Terminal FinFETs Fabricated Using an Etch-Back Gate Separation. IEEE Nanotechnology Magazine, 2007, 6, 201-205. | 2.0 | 18 |
| 90 | Fin-height controlled TiN-gate FinFET CMOS based on experimental mobility. Microelectronic Engineering, 2007, 84, 2101-2104. | 2.4 | 8 |

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| 91 | Optimum Gate Workfunction for $V_{m th}$-Controllable Four-Terminal-Driven Double-Gate MOSFETs (4T-XMOSFETs)â€”Band-Edge Workfunction Versus Midgap Workfunction. IEEE Nanotechnology Magazine, 2006, 5, 716-722. | 2.0 | 12 |
| 92 | Demonstration and Analysis of Accumulation-Mode Double-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistor. Japanese Journal of Applied Physics, 2006, 45, 3079-3083. | 1.5 | 5 |
| 93 | Experimental Study of Effective Carrier Mobility of Multi-Fin-Type Double-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors with (111) Channel Surface Fabricated by Orientation-Dependent Wet Etching. Japanese Journal of Applied Physics, 2006, 45, 3084-3087. | 1.5 | 18 |
| 94 | Advanced FinFET CMOS Technology: TiN-Gate, Fin-Height Control and Asymmetric Gate Insulator Thickness 4T-FinFETs. , 2006, , . | | 28 |
| 95 | Fabrication and characterization of vertical-type double-gate metal-oxide-semiconductor field-effect transistor with ultrathin Si channel and self-aligned source and drain. Applied Physics Letters, 2006, 88, 072103. | 3.3 | 7 |
| 96 | Fractally-Structured CMOS Processor for Quantum-Circuit Emulation. Japanese Journal of Applied Physics, 2002, 41, 2329-2334. | 1.5 | 1 |
| 97 | Charging and Retention Times in Silicon-Floating-Dot-Single-Electron Memory. Japanese Journal of Applied Physics, 2001, 40, 2041-2045. | 1.5 | 1 |
| 98 | An 8-qubit quantum-circuit processor. , 0, , . | | 7 |