Shin-ichi O'uchi

List of Publications by Year
in descending order

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98 papers	952 citations	567281 15 h-index	580821 25 g-index
98 all docs	98 docs citations	98 times ranked	758 citing authors

#	Article	IF	Citations
1	Variability Analysis of TiN Metal-Gate FinFETs. IEEE Electron Device Letters, 2010, 31, 546-548.	3.9	63
2	Performance Enhancement of Tunnel Field-Effect Transistors by Synthetic Electric Field Effect. IEEE Electron Device Letters, 2014, 35, 792-794.	3.9	53
3	Cointegration of High-Performance Tied-Gate Three-Terminal FinFETs and Variable Threshold-Voltage Independent-Gate Four-Terminal FinFETs With Asymmetric Gate-Oxide Thicknesses. IEEE Electron Device Letters, 2007, 28, 517-519.	3.9	48
4	Fully Integrated, 100-mV Minimum Input Voltage Converter With Gate-Boosted Charge Pump Kick-Started by <i>LC</i> Oscillator for Energy Harvesting. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 392-396.	3.0	40
5	Unexpected equivalent-oxide-thickness dependence of the subthreshold swing in tunnel field-effect transistors. Applied Physics Express, 2014, 7, 024201.	2.4	35
6	On the gate-stack origin threshold voltage variability in scaled FinFETs and multi-FinFETs. , 2010, , .		32
7	Enhancing SRAM cell performance by using independent double-gate FinFET. , 2008, , .		30
8	Advanced FinFET CMOS Technology: TiN-Gate, Fin-Height Control and Asymmetric Gate Insulator Thickness 4T-FinFETs. , 2006, , .		28
9	Experimental Evaluation of Effects of Channel Doping on Characteristics of FinFETs. IEEE Electron Device Letters, 2007, 28, 1123-1125.	3.9	28
10	Nanoscale Wet Etching of Physical-Vapor-Deposited Titanium Nitride and Its Application to Sub-30-nm-Gate-Length Fin-Type Double-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistor Fabrication. Japanese Journal of Applied Physics, 2010, 49, 06GH18.	1.5	27
11	Decomposition of On-Current Variability of nMOS FinFETs for Prediction Beyond 20 nm. IEEE Transactions on Electron Devices, 2012, 59, 2003-2010.	3.0	27
12	Independent-Double-Gate FinFET SRAM for Leakage Current Reduction. IEEE Electron Device Letters, 2009, 30, 757-759.	3.9	24
13	A Comparative Study of Nitrogen Gas Flow Ratio Dependence on the Electrical Characteristics of Sputtered Titanium Nitride Gate Bulk Planar Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors and Fin-Type Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2009, 48, 05DC01.	1.5	23
14	Fluctuation Analysis of Parasitic Resistance in FinFETs With Scaled Fin Thickness. IEEE Electron Device Letters, 2009, 30, 407-409.	3.9	23
15	Investigation of Low-Energy Tilted Ion Implantation for Fin-Type Double-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistor Extension Doping. Japanese Journal of Applied Physics, 2010, 49, 04DC18.	1.5	22
16	A 0.3-V 1- $mu ext{W}$ Super-Regenerative Ultrasound Wake-Up Receiver With Power Scalability. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1027-1031.	3.0	22
17	Experimental Study of Effective Carrier Mobility of Multi-Fin-Type Double-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors with (111) Channel Surface Fabricated by Orientation-Dependent Wet Etching. Japanese Journal of Applied Physics, 2006, 45, 3084-3087.	1.5	18
18	Four-Terminal FinFETs Fabricated Using an Etch-Back Gate Separation. IEEE Nanotechnology Magazine, 2007, 6, 201-205.	2.0	18

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19	Variability Origins of Parasitic Resistance in FinFETs With Silicided Source/Drain. IEEE Electron Device Letters, 2012, 33, 474-476.	3.9	15
20	Suppression of threshold voltage variability of double-gate fin field-effect transistors using amorphous metal gate with uniform work function. Applied Physics Letters, 2013, 102, .	3.3	15
21	Introduction of SiGe/Si heterojunction into novel multilayer tunnel FinFET. Japanese Journal of Applied Physics, 2016, 55, 04EB06.	1.5	15
22	Tunnel FinFET CMOS inverter with very low short-circuit current for ultralow-power Internet of Things application. Japanese Journal of Applied Physics, 2017, 56, 04CD19.	1.5	15
23	Fin-Height Effect on Poly-Si/PVD-TiN Stacked-Gate FinFET Performance. IEEE Transactions on Electron Devices, 2012, 59, 647-653.	3.0	14
24	Flex-Pass-Gate SRAM Design for Static Noise Margin Enhancement Using FinFET-Based Technology. , 2007, , .		13
25	Enhancement of FinFET performance using 25-nm-thin sidewall spacer grown by atomic layer deposition. Solid-State Electronics, 2012, 74, 13-18.	1.4	13
26	Optimum Gate Workfunction for $V_{m th}$-Controllable Four-Terminal-Driven Double-Gate MOSFETs (4T-XMOSFETs)â€"Band-Edge Workfunction Versus Midgap Workfunction. IEEE Nanotechnology Magazine, 2006, 5, 716-722.	2.0	12
27	Threshold-Voltage Reduction of FinFETs by Ta/Mo Interdiffusion Dual Metal-Gate Technology for Low-Operating-Power Application. IEEE Transactions on Electron Devices, 2008, 55, 2454-2461.	3.0	12
28	Experimental Study of Physical-Vapor-Deposited Titanium Nitride Gate with An n⁺-Polycrystalline Silicon Capping Layer and Its Application to 20 nm Fin-Type Double-Gate Metalâ€"Oxideâ€"Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2011, 50, 04DC14.	1.5	12
29	Variability Analysis of Scaled Crystal Channel and Poly-Si Channel FinFETs. IEEE Transactions on Electron Devices, 2012, 59, 573-581.	3.0	12
30	Influence of work function variation of metal gates on fluctuation of sub-threshold drain current for fin field-effect transistors with undoped channels. Japanese Journal of Applied Physics, 2014, 53, 04EC11.	1.5	12
31	Metal-Gate FinFET Variation Analysis by Measurement and Compact Model. IEEE Electron Device Letters, 2009, 30, 556-558.	3.9	11
32	Demonstration of Split-Gate Type Trigate Flash Memory With Highly Suppressed Over-Erase. IEEE Electron Device Letters, 2012, 33, 345-347.	3.9	10
33	A Dynamical Power-Management Demonstration Using Four-Terminal Separated-Gate FinFETs. IEEE Electron Device Letters, 2007, 28, 452-454.	3.9	9
34	A Ta/Mo Interdiffusion Dual Metal Gate Technology for Drivability Enhancement of FinFETs. IEEE Electron Device Letters, 2008, 29, 618-620.	3.9	9
35	Fin-height controlled TiN-gate FinFET CMOS based on experimental mobility. Microelectronic Engineering, 2007, 84, 2101-2104.	2.4	8
36	Dual metal gate FinFET integration by Ta/Mo diffusion technology for Vt reduction and multi-Vt CMOS application. , 2008, , .		8

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37	Atomic Layer Deposition of SiO₂ for the Performance Enhancement of Fin Field Effect Transistors. Japanese Journal of Applied Physics, 2013, 52, 116503.	1.5	8
38	An 8-qubit quantum-circuit processor. , 0, , .		7
39	Fabrication and characterization of vertical-type double-gate metal-oxide-semiconductor field-effect transistor with ultrathin Si channel and self-aligned source and drain. Applied Physics Letters, 2006, 88, 072103.	3.3	7
40	Design of SOI FinFET on 32nm technology node for low standby power (LSTP) operation considering gate-induced drain leakage (GIDL). Solid-State Electronics, 2010, 54, 1060-1065.	1.4	7
41	Investigation of Thermal Stability of TiN Film Formed by Atomic Layer Deposition Using Tetrakis(dimethylamino)titanium Precursor for Metal-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistor. Japanese Journal of Applied Physics, 2010, 49, 04DA16.	1.5	7
42	Tunnel Field-Effect Transistors with Extremely Low Off-Current Using Shadowing Effect in Drain Implantation. Japanese Journal of Applied Physics, 2011, 50, 06GF14.	1.5	7
43	Performance evaluation of parallel electric field tunnel field-effect transistor by a distributed-element circuit model. Solid-State Electronics, 2014, 102, 82-86.	1.4	7
44	Impact of granular work function variation in a gate electrode on low-frequency noise for fin field-effect transistors. Applied Physics Express, 2015, 8, 044201.	2.4	7
45	Impact of extension and source/drain resistance on FinFET performance. , 2008, , .		6
46	Fabrication and Characterization of NOR-Type Tri-Gate Flash Memory with Improved Inter-Poly Dielectric Layer by Rapid Thermal Oxidation. Japanese Journal of Applied Physics, 2012, 51, 06FE19.	1.5	6
47	Improvement of epitaxial channel quality on heavily arsenic- and boron-doped Si surfaces and impact on performance of tunnel field-effect transistors. Solid-State Electronics, 2015, 113, 173-178.	1.4	6
48	Demonstration and Analysis of Accumulation-Mode Double-Gate Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistor. Japanese Journal of Applied Physics, 2006, 45, 3079-3083.	1.5	5
49	Robust and compact key generator using physically unclonable function based on logic-transistor-compatible poly-crystalline-Si channel FinFET technology. , 2015, , .		5
50	Suppression of tunneling rate fluctuations in tunnel field-effect transistors by enhancing tunneling probability. Japanese Journal of Applied Physics, 2017, 56, 04CD02.	1.5	5
51	Rigorous Design of 22-nm Node 4-Terminal SOI FinFETs for Reliable Low Standby Power Operation with Semi-empirical Parameters. Journal of Semiconductor Technology and Science, 2010, 10, 265-275.	0.4	5
52	Enhancing Noise Margins of Fin-Type Field Effect Transistor Static Random Access Memory Cell by Using Threshold Voltage-Controllable Flexible-Pass-Gates. Applied Physics Express, 2009, 2, 054502.	2.4	4
53	Variability Analysis of TiN FinFET SRAM Cells and Its Compensation by Independent-DG FinFETs. IEEE Electron Device Letters, 2010, 31, 1095-1097.	3.9	4
54	Scaling breakthrough for analog/digital circuits by suppressing variability and low-frequency noise for FinFETs by amorphous metal gate technology. , 2014, , .		4

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55	(Invited) Charge Trapping Type SOI-FinFET Flash Memory. ECS Transactions, 2014, 61, 263-280.	0.5	4
56	Heated ion implantation for high-performance and highly reliable silicon-on-insulator complementary metalâ€“oxideâ€“silicon fin field-effect transistors. Japanese Journal of Applied Physics, 2015, 54, 04DA06.	1.5	4
57	Closed-form analytical model of static noise margin for ultra-low voltage eight-transistor tunnel FET static random access memory. Japanese Journal of Applied Physics, 2016, 55, 04ED06.	1.5	4
58	A Closed-Form Expression for Minimum Operating Voltage of CMOS D Flip-Flop. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2007-2016.	3.1	4
59	Epitaxial growth of Ge thin film on Si (001) by DC magnetron sputtering. Materials Science in Semiconductor Processing, 2017, 70, 3-7.	4.0	4
60	Dual metal gate FinFET integration by Ta/Mo diffusion technology for Vt reduction and multi-Vt CMOS application. Solid-State Electronics, 2009, 53, 701-705.	1.4	3
61	Variability origins of FinFETs and perspective beyond 20nm node. , 2011, , .		3
62	A Correlative Analysis Between Characteristics of FinFETs and SRAM Performance. IEEE Transactions on Electron Devices, 2012, 59, 1345-1352.	3.0	3
63	Gate Structure Dependence of Variability in Polycrystalline Silicon Fin-Channel Flash Memories. Japanese Journal of Applied Physics, 2013, 52, 06GE01.	1.5	3
64	Impact of fin length on threshold voltage modulation by back bias for Independent double-gate tunnel fin field-effect transistors. Solid-State Electronics, 2015, 111, 62-66.	1.4	3
65	Impact of extension implantation conditions of fin field-effect transistors on gate-induced drain leakage. Japanese Journal of Applied Physics, 2016, 55, 04EB01.	1.5	3
66	Impact of residual defects caused by extension ion implantation in FinFETs on parasitic resistance and its fluctuation. Solid-State Electronics, 2017, 132, 103-108.	1.4	3
67	Logic gate threshold voltage controllable single metal gate FinFET CMOS inverters implemented by using co-integration of 3T/4T-FinFETs. , 2008, , .		2
68	Experimental evaluation of parallel transmission using optical ZCZ-CDMA system. , 2009, , .		2
69	Fabrication of Floating-Gate-Type Fin-Channel Double- and Tri-Gate Flash Memories and Comparative Study of Their Electrical Characteristics. Japanese Journal of Applied Physics, 2012, 51, 04DD03.	1.5	2
70	Experimental Study of Floating-Gate-Type Metalâ€“Oxideâ€“Semiconductor Capacitors with Nanosize Triangular Cross-Sectional Tunnel Areas for Low Operating Voltage Flash Memory Application. Japanese Journal of Applied Physics, 2012, 51, 06FF01.	1.5	2
71	(Invited) FinFET Flash Memory Technology. ECS Transactions, 2012, 45, 289-310.	0.5	2
72	Experimental study of three-dimensional fin-channel charge trapping flash memories with titanium nitride and polycrystalline silicon gates. Japanese Journal of Applied Physics, 2014, 53, 04ED16.	1.5	2

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73	Bias temperature instability in tunnel field-effect transistors. Japanese Journal of Applied Physics, 2017, 56, 04CA04.	1.5	2
74	Channel shape and interpoly dielectric material effects on electrical characteristics of floating-gate-type three-dimensional fin channel flash memories. Japanese Journal of Applied Physics, 2015, 54, 04DD04.	1.5	2
75	FinFET-Based Flex-Vth SRAM Design for Drastic Standby-Leakage-Current Reduction. IEICE Transactions on Electronics, 2008, E91-C, 534-542.	0.6	2
76	Experimental Comparisons between Tetrakis(dimethylamino)titanium Precursor-Based Atomic-Layer-Deposited and Physical-Vapor-Deposited Titaniumâ€“Nitride Gate for High-Performance Fin-Type Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2012, 51, 04DA05.	1.5	2
77	Charging and Retention Times in Silicon-Floating-Dot-Single-Electron Memory. Japanese Journal of Applied Physics, 2001, 40, 2041-2045.	1.5	1
78	Fractally-Structured CMOS Processor for Quantum-Circuit Emulation. Japanese Journal of Applied Physics, 2002, 41, 2329-2334.	1.5	1
79	Flex-pass-gate SRAM for static noise margin enhancement using FinFET-based technology. Solid-State Electronics, 2008, 52, 1694-1702.	1.4	1
80	Independent-gate four-terminal FinFET SRAM for drastic leakage current reduction. , 2008, , .		1
81	(Invited) Advanced FinFET Technologies: Extension Doping, Vth Controllable CMOS Inverters and SRAM. ECS Transactions, 2010, 28, 385-401.	0.5	1
82	Correlative analysis between characteristics of 30-nm L<inf>G</inf> FinFETs and SRAM performance. , 2011, , .		1
83	(Invited) Floating Gate Type SOI-FinFET Flash Memories with Different Channel Shapes and Interpoly Dielectric Materials. ECS Transactions, 2016, 72, 11-24.	0.5	1
84	High-Frequency Precise Characterization of Intrinsic FinFET Channel. IEICE Transactions on Electronics, 2012, E95.C, 752-760.	0.6	1
85	Nitrogen gas flow ratio controlled PVD TiN metal gate technology for FinFET CMOS. , 2007, , .		0
86	Variable-Threshold-Voltage FinFETs with a Control-Voltage Range within the Logic-Level Swing Using Asymmetric Work-Function Double Gates. International Power Modulator Symposium and High-Voltage Workshop, 2008, , .	0.0	0
87	Minimization of Gate-Induced Drain Leakage by Controlling Gate Underlap Length for Low-Standby-Power Operation of 20-nm-Level Four-Terminal Silicon-on-Insulator Fin-Shaped Field Effect Transistor. Japanese Journal of Applied Physics, 2010, 49, 024203.	1.5	0
88	Variability analysis of TiN FinFET SRAM cell performance and its compensation using Vth-controllable independent double-gate FinFET. , 2010, , .		0
89	Static noise margin enhancement by flex-pass-gate SRAM. Electronics and Communications in Japan, 2011, 94, 57-64.	0.5	0
90	Experimental Comparisons between Tetrakis(dimethylamino)titanium Precursor-Based Atomic-Layer-Deposited and Physical-Vapor-Deposited Titaniumâ€“Nitride Gate for High-Performance Fin-Type Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2012, 51, 04DA05.	1.5	0

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91	(Invited) On-Current Variability Sources of FinFETs: Analysis and Perspective for 14nm-Lg Technology. ECS Transactions, 2012, 45, 231-242.	0.5	0
92	1/fNoise Characteristics of Fin-Type Field-Effect Transistors in Saturation Region. Japanese Journal of Applied Physics, 2013, 52, 04CC23.	1.5	0
93	(Invited) Independent-Double-Gate FinFET SRAM Technology. ECS Transactions, 2013, 50, 193-199.	0.5	0
94	Highly Vt tunable and low variability triangular fin-channel MOSFETs on SOTB. Microelectronic Engineering, 2015, 147, 290-293.	2.4	0
95	Structural and electrical characterization of epitaxial Ge thin films on Si(001) formed by sputtering. Japanese Journal of Applied Physics, 2017, 56, 04CB01.	1.5	0
96	Static Noise Margin Enhancement by Flex-Pass-Gate SRAM. IEEJ Transactions on Electronics, Information and Systems, 2008, 128, 919-925.	0.2	0
97	A 0.7-V Opamp in Scaled Low-Standby-Power FinFET Technology. IEICE Transactions on Electronics, 2012, E95.C, 686-695.	0.6	0
98	SOI CMOS Voltage Multiplier Circuits with Body Bias Control Technique for Battery-Less Wireless Sensor System. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2014, E97.A, 741-748.	0.3	0