James C Hoe

List of Publications by Year
in descending order

30	632	1163117 8	1372567 10
papers	citations	h-index	g-index

30	30	30	550
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Computer Generation of Hardware for Linear Digital Signal Processing Transforms. ACM Transactions on Design Automation of Electronic Systems, 2012, 17, 1-33.	2.6	97
2	Time-Multiplexed Multiple-Constant Multiplication. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1551-1563.	2.7	67
3	SPIRAL: Extreme Performance Portability. Proceedings of the IEEE, 2018, 106, 1935-1968.	21.3	58
4	Permuting streaming data using RAMs. Journal of the ACM, 2009, 56, 1-34.	2.2	44
5	Automatic generation of customized discrete fourier transform IPs. , 2005, , .		43
6	High Performance Stereo Vision Designed for Massively Data Parallel Platforms. IEEE Transactions on Circuits and Systems for Video Technology, 2010, 20, 1509-1519.	8.3	40
7	Formal datapath representation and manipulation for implementing DSP transforms. , 2008, , .		36
8	Optical OFDM for the data center. , 2010, , .		28
9	Memory Bandwidth Efficient Two-Dimensional Fast Fourier Transform Algorithm and Implementation for Large Problem Sizes. , 2012, , .		24
10	Generating FPGA-Accelerated DFT Libraries. , 2007, , .		23
11	Automatic Pipelining From Transactional Datapath Specifications. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 441-454.	2.7	20
12	Fast and accurate resource estimation of automatically generated custom DFT IP cores. , 2006, , .		19
13	Optimizing FFT Precision in Optical OFDM Transceivers. IEEE Photonics Technology Letters, 2011, 23, 1550-1552.	2.5	17
14	Processor Assisted Worklist Scheduling for FPGA Accelerated Graph Processing on a Shared-Memory Platform. , 2019, , .		15
15	Automatic generation of streaming datapaths for arbitrary fixed permutations. , 2009, , .		13
16	Hardware implementation of the discrete fourier transform with non-power-of-two problem size. , 2010, , .		12
17	High-Level Design and Validation of the BlueSPARC Multithreaded Processor. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1459-1470.	2.7	12
18	PageRank Acceleration for Large Graphs with Scalable Hardware and Two-Step SpMV. , 2018, , .		12

#	Article	IF	Citations
19	Domain-specific library generation for parallel software and hardware platforms. , 2008, , .		11
20	HAMLeT: Hardware accelerated memory layout transform within 3D-stacked DRAM. , 2014, , .		11
21	Design studies for an ASIC implementation of an optical OFDM transceiver. , 2010, , .		9
22	FFTs with Near-Optimal Memory Access Through Block Data Layouts: Algorithm, Architecture and Design Automation. Journal of Signal Processing Systems, 2016, 85, 67-82.	2.1	8
23	FFTS with near-optimal memory access through block data layouts. , 2014, , .		6
24	Algorithm/hardware co-optimized SAR image reconstruction with 3D-stacked logic in memory. , 2014, , .		3
25	High-Performance Memory Snapshotting for Real-Time, Consistent, Hypervisor-Based Monitors. IEEE Transactions on Dependable and Secure Computing, 2019, , 1-1.	5.4	3
26	Real-time DSP-based optical OFDM transmission. , 2010, , .		1
27	FFT Compiler: from math to efficient hardware HLDVT invited short paper. , 2007, , .		0
28	MEMOCODE 2006 guest editorsâ€™ introduction. Design Automation for Embedded Systems, 2008, 12, 95-95.	1.0	0
29	FPGA-based optical transmitters for electronic predistortion and advanced signal format generation. , 2009, , .		0
30	Predistortion and OFDM realizations. , 2011, , .		0