Michiel S J Steyaert

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/669193/publications.pdf

Version: 2024-02-01

363	10,187	36303	56724
papers	citations	51 h-index	83 g-index

388	388	388	3838
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	In the Pursuit of the Optimal Accuracyâ€“Speedâ€“Power Analog-to-Digital Converter Architecture: A mathematical framework. IEEE Solid-State Circuits Magazine, 2022, 14, 45-53.	0.4	3
2	A new feedback strategy to boost Q-factor of charge-sharing bandpass filters. Analog Integrated Circuits and Signal Processing, 2021, 106, 125-137.	1.4	1
3	A 5-GS/s 158.6-mW 9.4-ENOB Passive-Sampling Time-Interleaved Three-Stage Pipelined-SAR ADC With Analog-Digital Corrections in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2020, , 1-12.	5.4	39
4	Advanced Design of Schottky Photodiodes in Bulk CMOS for High Speed Optical Receivers. IEEE Journal of Quantum Electronics, 2020, 56, 1-8.	1.9	1
5	1310/1550 nm Optical Receivers With Schottky Photodiode in Bulk CMOS. IEEE Journal of Solid-State Circuits, 2020, 55, 1776-1784.	5.4	3
6	Stacking Isolated SC Cores for High-Voltage Wide Input Range Monolithic DCâ€“DC Conversion. IEEE Journal of Solid-State Circuits, 2020, 55, 2639-2648.	5.4	8
7	Advanced Multiphasing Switched-Capacitor DC-DC Converters. , 2020, , .		3
8	Advanced Multiphasing: Pushing the Limits of Fully Integrated Switched-Capacitor Converters. , 2020, , 109-124.		0
9	Continuously-Scalable Conversion Ratio Topologies. , 2020, , 121-144.		0
10	Scalable Parasitic Charge Redistribution. , 2020, , 51-73.		0
11	Stage Outphasing and Multiphase Soft-Charging. , 2020, , 95-120.		0
12	A 13.5-Gb/s 5-mV-Sensitivity 26.8-ps-CLKâ€“OUT Delay Triple-Latch Feedforward Dynamic Comparator in 28-nm CMOS. IEEE Solid-State Circuits Letters, 2019, 2, 167-170.	2.0	21
13	A Fully-Integrated 6:1 Cascaded Switched-Capacitor DC-DC Converter Achieving 74% Efficiency at 0.1W/mm2. , 2019, , .		1
14	An 11 GHz Dual-Sided Self-Calibrating Dynamic Comparator in 28 nm CMOS. Electronics (Switzerland), 2019, 8, 13.	3.1	9
15	A Fully Integrated Switched-Capacitor-Based ACâ€“DC Converter for a 120 V_{RMS} Mains Interface. IEEE Journal of Solid-State Circuits, 2019, 54, 2009-2018.	5.4	4
16	3.3 A 5GS/s 158.6mW 12b Passive-Sampling 8Ã—-Interleaved Hybrid ADC with 9.4 ENOB and 160.5dB FoM<inf>S</inf> in 28nm CMOS. , 2019, , .		11
17	A 7.5 - 42V Input High-VCR Monolithic DC-DC Converter Using Stacked Isolated SC Cores. , 2019, , .		0
18	A 13.5-Gb/s 5-mV-Sensitivity 26.8-ps-CLKâ€“OUT Delay Triple-Latch Feedforward Dynamic Comparator in 28-nm CMOS. , 2019, , .		11

#	Article	IF	Citations
19	Optical Receiver with Schottky Photodiode and TIA with High Gain Amplifier in 28nm Bulk CMOS. , 2019, , .		2
20	Design of Single-Topology Continuously Scalable-Conversion-Ratio Switched- Capacitor DCâ€“DC Converters. IEEE Journal of Solid-State Circuits, 2019, 54, 1039-1047.	5.4	24
21	A Wideband Low-Noise Variable-Gain Amplifier With a 3.4 dB NF and up to 45 dB Gain Tuning Range in 130-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1104-1108.	3.0	13
22	Radiation Hardened CMOS Integrated Circuits for Time-Based Signal Processing. Analog Circuits and Signal Processing Series, 2018, , .	0.3	2
23	40-nm CMOS Wideband High-IF Receiver Using a Modified Charge-Sharing Bandpass Filter to Boost Q-Factor. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 2581-2591.	5.4	8
24	A 2.56-GHz SEU Radiation Hard LC -Tank VCO for High-Speed Communication Links in 65-nm CMOS Technology. IEEE Transactions on Nuclear Science, 2018, 65, 407-412.	2.0	34
25	A 1.25-GS/s 7-b SAR ADC With 36.4-dB SNDR at 5 GHz Using Switch-Bootstrapping, USPC DAC and Triple-Tail Comparator in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2018, 53, 1889-1901.	5.4	66
26	Radiation Effects in CMOS Technology. Analog Circuits and Signal Processing Series, 2018, , 1-20.	0.3	5
27	A Charge-Sharing Bandpass Filter Topology with Boosted Q-Factor in 40-NM CMOS. , 2018, , .		1
28	A Single-Topology Continuously-Scalable-Conversion-Ratio Fully Integrated Switched-Capacitor DC-DC Converter with 0-to-2.22V Output and 93% Peak-Efficiency. , 2018, , .		3
29	Proof of General Switched-Capacitor DC-DC Converter Law using Voltage-Domain Analysis. , 2018, , .		2
30	A Fully Integrated Switched-Capacitor Based AC-DC Converter for a 120V<inf>RMS</inf> Mains Interface. , 2018, , .		0
31	A 1310/1550 nm Fully-Integrated Optical Receiver with Schottky Photodiode and Low-Noise Transimpedance Amplifier in 40 nm Bulk CMOS. , 2018, , .		4
32	Radiation Tolerant, Low Noise Phase Locked Loops in 65 nm CMOS Technology. EPJ Web of Conferences, 2018, 170, 01021.	0.3	1
33	Time-Domain Signal Processing. Analog Circuits and Signal Processing Series, 2018, , 21-42.	0.3	0
34	Schottky Photodiodes in Bulk CMOS for High-Speed 1310/1550 nm Optical Receivers. IEEE Journal of Selected Topics in Quantum Electronics, 2018, 24, 1-8.	2.9	10
35	Low Jitter Clock Generators. Analog Circuits and Signal Processing Series, 2018, , 97-121.	0.3	0
36	Clock Synthesizers. Analog Circuits and Signal Processing Series, 2018, , 43-70.	0.3	0

#	Article	IF	Citations
37	A capacitive DC-DC converter for stacked loads with wide range DVS achieving 98.2% peak efficiency in 40nm CMOS. , 2018, , .		2
38	Single Shot Time-to-Digital Converters. Analog Circuits and Signal Processing Series, 2018, , 71-96.	0.3	0
39	Monolithic 1310nm 1Gb/s Optical Receiver with Schottky Photodiode in 40nm Bulk CMOS. , 2018, , .		1
40	Radiation Experiments on CMOS PLLs. Analog Circuits and Signal Processing Series, 2018, , 123-143.	0.3	0
41	Radiation Hard Frequency Synthesizers. Analog Circuits and Signal Processing Series, 2018, , 145-154.	0.3	0
42	10.1 A 1.1W/mm²-power-density 82%-efficiency fully integrated 3â¶1 Switched-Capacitor DC-DC converter in baseline 28nm CMOS using Stage Outphasing and Multiphase Soft-Charging. , 2017, , .		14
43	MIMO Switched-Capacitor DCâ€“DC Converters Using Only Parasitic Capacitances Through Scalable Parasitic Charge Redistribution. IEEE Journal of Solid-State Circuits, 2017, 52, 1814-1824.	5.4	9
44	Comparison of a 65 nm CMOS Ring- and LC-Oscillator Based PLL in Terms of TID and SEU Sensitivity. IEEE Transactions on Nuclear Science, 2017, 64, 245-252.	2.0	46
45	Design of Soft-Charging Switched-Capacitor DCâ€“DC Converters Using Stage Outphasing and Multiphase Soft-Charging. IEEE Journal of Solid-State Circuits, 2017, 52, 3132-3141.	5.4	42
46	Fully integrated power management: The missing link?. , 2017, , .		2
47	Modelling, design and characterization of Schottky diodes in 28nm bulk CMOS for 850/1310/1550nm fully integrated optical receivers. , 2017, , .		3
48	Highly integrated wavelength-locked Si photonic ring transmitter using direct monitoring of drop-port OMA. , 2017, , .		1
49	A 36.4dB SNDR @ 5GHz 1.25GS/s 7b 3.56mW single-channel SAR ADC in 28nm bulk CMOS. , 2017, , .		6
50	A true two-quadrant fully integrated switched capacitor DC-DC converter supporting vertically stacked DVS-loads with up to 99.6% efficiency. , 2017, , .		5
51	Schottky diodes in 40nm bulk CMOS for 1310nm high-speed optical receivers. , 2017, , .		1
52	A single-event upset robust, 2.2 GHz to 3.2 GHz, 345 fs jitter PLL with triple-modular redundant phase detector in 65 nm CMOS. , 2016, , .		18
53	A low noise clock generator for high-resolution time-to-digital convertors. Journal of Instrumentation, 2016, 11, C02038-C02038.	1.2	4
54	High-Ratio Voltage Conversion in CMOS for Efficient Mains-Connected Standby. Analog Circuits and Signal Processing Series, 2016, , .	0.3	1

#	Article	IF	Citations
55	Wavelength Locking of a Si Ring Modulator Using an Integrated Drop-Port OMA Monitoring Circuit. IEEE Journal of Solid-State Circuits, 2016, 51, 2328-2344.	5.4	29
56	A modelling and design approach for push/pull switched capacitor DC-DC converters. , 2016, , .		3
57	MIMO Switched-Capacitor converter using only parasitic capacitance with Scalable Parasitic Charge Redistribution. , 2016, , .		4
58	Scalable Parasitic Charge Redistribution: Design of High-Efficiency Fully Integrated Switched-Capacitor DCâ€“DC Converters. IEEE Journal of Solid-State Circuits, 2016, 51, 2843-2853.	5.4	52
59	12.2 A 94.6%-efficiency fully integrated switched-capacitor DC-DC converter in baseline 40nm CMOS using scalable parasitic charge redistribution. , 2016, , .		41
60	A Self-Calibrated Bangâ€“Bang Phase Detector for Low-Offset Time Signal Processing. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 453-457.	3.0	10
61	An 11/1 Switched-Capacitor DCâ€“DC Converter for Low Power from the Mains. Analog Circuits and Signal Processing Series, 2016, , 85-104.	0.3	0
62	Two-Stage Approach for Compact and Efficient Low Power from the Mains. Analog Circuits and Signal Processing Series, 2016, , 67-83.	0.3	0
63	Toward Monolithic Integration of Mains Interfaces. Analog Circuits and Signal Processing Series, 2016, , 41-48.	0.3	0
64	Switched-Capacitor DCâ€“DC in Bulk CMOS for On-Chip Power Granularization. Analog Circuits and Signal Processing Series, 2016, , 11-39.	0.3	0
65	Monolithic SC DCâ€“DC Toward Even Higher Voltage Conversion Ratios. Analog Circuits and Signal Processing Series, 2016, , 105-119.	0.3	0
66	A Single-Stage Monolithic Mains Interface in 0.35 Î¼m CMOS. Analog Circuits and Signal Processing Series, 2016, , 49-65.	0.3	0
67	When hardware is free, power is expensive! Is integrated power management the solution?. , 2015, , .		19
68	A MGy, Low-Offset Programmable Instrumentation Amplifier IC for Nuclear Applications. , 2015, , .		3
69	MGy Radiation Assessment of a Space-Graded Amplifier and ADC. , 2015, , .		2
70	Wavelength locking of a Si ring modulator using an integrated drop-port OMA monitoring circuit. , 2015, , .		2
71	A folding dickson-based fully integrated wide input range capacitive DC-DC converter achieving Vout/2-resolution and 71% average efficiency. , 2015, , .		12
72	Fast switch bootstrapping for GS/s high-resolution analog-to-digital converter. , 2015, , .		8

#	Article	IF	Citations
73	22.5 A 4×20Gb/s WDM ring-based hybrid CMOS silicon photonics transceiver. , 2015, , .		14
74	A 1 MGy TID Radiation-Tolerant 56 µW CMOS Temperature Sensor with ±1.7°C Accuracy. , 2015, , .		0
75	A 120ÂGHz QVCO with 16.2ÂGHz tuning range resistent against VCO pulling in 45Ânm CMOS. Analog Integrated Circuits and Signal Processing, 2015, 82, 359-368.	1.4	3
76	High voltage DCâ€“AC conversion in standard 1.2ÂV CMOS technology. Analog Integrated Circuits and Signal Processing, 2015, 84, 237-245.	1.4	0
77	A single shot TDC with 4.8 ps resolution in 40 nm CMOS for high energy physics applications. Journal of Instrumentation, 2015, 10, C01031-C01031.	1.2	9
78	Qualification method for a 1 MGy-tolerant front-end chip designed in 65 nm CMOS for the read-out of remotely operated sensors and actuators during maintenance in ITER. Fusion Engineering and Design, 2015, 96-97, 1002-1005.	1.9	9
79	20.1 A light-load-efficient 11/1 switched-capacitor DC-DC converter with 94.7% efficiency while delivering 100mW at 3.3V. , 2015, , .		8
80	Fully Integrated Wide Input Voltage Range Capacitive DC-DC Converters: The Folding Dickson Converter. IEEE Journal of Solid-State Circuits, 2015, 50, 1560-1570.	5.4	58
81	A Light-Load-Efficient 11/1 Switched-Capacitor DC-DC Converter With 94.7% Efficiency While Delivering 100 mW at 3.3 V. IEEE Journal of Solid-State Circuits, 2015, 50, 2849-2860.	5.4	41
82	The folding dickson converter: A step towards fully integrated wide input range capacitive DC-DC converters. , 2014, , .		4
83	Efficient optimization of fully-integrated inductive DCâ€“DC converters comprising tapered inductor layout synthesis and temperature effects. Analog Integrated Circuits and Signal Processing, 2014, 78, 111-121.	1.4	1
84	Highly sensitive, low-power, 10-20Gb/s transimpedance amplifier based on cascaded CMOS inverter gain stages. , 2014, , .		6
85	Monolithic switched-capacitor DC-DC towards high voltage conversion ratios. , 2014, , .		16
86	Design of a frequency reference based on a PVT-independent transmission line delay. , 2014, , .		0
87	A remotely-powered, 20ÂMb/s, 5.35ÂpJ/bit impulse-UWB WSN tag for cm-accurate-localization sensor networks. Analog Integrated Circuits and Signal Processing, 2014, 80, 531-540.	1.4	1
88	From AC to DC and Reverse, the Next Fully Integrated Power Management Challenge. , 2014, , 103-128.		0
89	CMOS Integrated Capacitive DC-DC Converters. , 2013, , .		38
90	Analog Organic Electronics. , 2013, , .		14

#	Article	IF	Citations
91	A 265 V<formula formulatype="inline"><tex Notation="TeX">$_{m RMS}$</tex></formula> Mains Interface Integrated in 0.35 <formula formulatype="inline"><tex Notation="TeX">mu</tex></formula>m CMOS. IEEE Journal of Solid-State Circuits, 2013, 48, 1558-1564.	5.4	9
92	A 63,000 Q-factor relaxation oscillator with switched-capacitor integrated error feedback. , 2013, , .		42
93	Monolithic power management front end with high voltage dense energy storage for wireless powering. , 2013, , .		0
94	Electronic dispersion correction circuit for Plastic Optical Fiber channels. , 2013, , .		0
95	Linear equalization filter for PMMA fiber channels. , 2013, , .		1
96	A 120GHz quadrature frequency generator with 16.2GHz tuning range in 45nm CMOS. , 2013, , .		9
97	A monolithic stacked Class-D approach for high voltage DC-AC conversion in standard CMOS. , 2013, , .		0
98	Analog Circuit Design in Organic Thin-Film Transistor Technologies on Foil: An Overview. , 2013, , 269-279.		1
99	A stacked full-bridge topology for high voltage DC-AC conversion in standard CMOS technology. , 2013, , .		1
100	A 4.5 MGy TID-Tolerant CMOS Bandgap Reference Circuit Using a Dynamic Base Leakage Compensation Technique. IEEE Transactions on Nuclear Science, 2013, 60, 2819-2824.	2.0	22
101	17 bit 4.35mW 1kHz Delta Sigma ADC and 256-to-1 multiplexer for remote handling instrumentation equipment. Fusion Engineering and Design, 2013, 88, 1942-1946.	1.9	9
102	A 1.65 W fully integrated 90 nm bulk cmos capacitive DC-DC converter with intrinsic charge recycling. IEEE Transactions on Power Electronics, 2013, 28, 4327-4334.	7.9	26
103	A > 4 MGy radiation tolerant 8 THzOhm transimpedance amplifier with 50 dB dynamic range. Journal of Instrumentation, 2013, 8, C02052-C02052.	1.2	1
104	EMI resisting voltage regulator with large signal PSR up to 1GHz. , 2013, , .		1
105	A 120GHz fully integrated 10Gb/s wireless transmitter with on-chip antenna in 45nm low power CMOS. , 2013, , .		5
106	A/D Conversion. , 2013, , 93-109.		0
107	Organic Thin-Film Transistor Technology: Properties and Functionality. , 2013, , 15-57.		0
108	Conceptual design of a MGy tolerant integrated signal conditioning circuit in 130nm and 700nm CMOS. Journal of Instrumentation, 2012, 7, C01017-C01017.	1.2	4

#	Article	IF	Citations
109	A 265V<inf>RMS</inf> mains interface integrated in 0.35μm CMOS. , 2012, , .		1
110	Analog Building Blocks for Organic Smart Sensor Systems in Organic Thin-Film Transistor Technology on Flexible Plastic Foil. IEEE Journal of Solid-State Circuits, 2012, 47, 1712-1720.	5.4	48
111	A 186 to 212ÂGHz Downconverter in 90Ânm CMOS. Journal of Infrared, Millimeter, and Terahertz Waves, 2012, 33, 1085-1103.	2.2	8
112	Optimization of fully-integrated power converter circuits comprising tapered inductor layout and temperature effects. , 2012, , .		3
113	Low-Power, 10-Gbps 1.5-Vpp differential CMOS driver for a silicon electro-optic ring modulator. , 2012, , .		8
114	The tapered matrix amplifier: a low-power high-gain broadband amplifier. Analog Integrated Circuits and Signal Processing, 2012, 73, 961-972.	1.4	3
115	Dual-output capacitive DC-DC converter with power distribution regulator in 90 nm CMOS. , 2012, , .		13
116	Ultra low voltage ΔΣ modulation using biased inverters in 130nm CMOS. , 2012, , .		1
117	Monolithic integration of a class DE inverter for on-chip resonant DC-DC converters. , 2012, , .		1
118	On the Other Applications of Organic Electronics on Foil. IEEE Solid-State Circuits Magazine, 2012, 4, 43-49.	0.4	8
119	Design and Assessment of a 6 ps-Resolution Time-to-Digital Converter With 5 MGy Gamma-Dose Tolerance for LIDAR Application. IEEE Transactions on Nuclear Science, 2012, 59, 1382-1389.	2.0	23
120	An Ultra-Low-Power, Batteryless Microsystem for Wireless Sensor Networks. Procedia Engineering, 2012, 47, 1406-1409.	1.2	1
121	1D and 2D analog 1.5kHz air-stable organic capacitive touch sensors on plastic foil. , 2012, , .		4
122	On-chip gain reconfigurable 1.2V 24μW chopping instrumentation amplifier with automatic resistor matching in 0.13μm CMOS. , 2012, , .		9
123	1-1-1 MASH $Delta Sigma$ Time-to-Digital Converters With 6 ps Resolution and Third-Order Noise-Shaping. IEEE Journal of Solid-State Circuits, 2012, 47, 2093-2106.	5.4	50
124	Accuracy improvement of the output impedance model for capacitive down-converters. Analog Integrated Circuits and Signal Processing, 2012, 72, 271-277.	1.4	8
125	A 250 mV 7.5 Î¼W 61 dB SNDR SC Î”Î£ Modulator Using Near-Threshold-Voltage-Biased Inverter Amplifiers in 130 nm CMOS. IEEE Journal of Solid-State Circuits, 2012, 47, 709-721.	5.4	101
126	A mathematical steady-state design model for fully-integrated boost and buck DCâ€“DC converters. Analog Integrated Circuits and Signal Processing, 2012, 70, 369-375.	1.4	2

#	Article	IF	Citations
127	Spatially oversampled TDC with digital resolution enhancement. Analog Integrated Circuits and Signal Processing, 2012, 70, 311-322.	1.4	0
128	A standard cell based all-digital Time-to-Digital Converter with reconfigurable resolution and on-line background calibration. , 2011, , .		7
129	DC-DC converter assisted two-stage amplifier in organic thin-film transistor technology on foil. , 2011, , .		19
130	Differential input topologies with immunity to electromagnetic interference. , 2011, , .		7
131	Design of a MGy tolerant instrumentation amplifier using a correlated double sampling technique in 130 nm CMOS. , 2011, , .		2
132	Design and assessment of a 6 ps-resolution time-to-digital converter with 5 MGy gamma-dose tolerance for nuclear instrumentation. , 2011, , .		1
133	An active guarding technique for substrate noise suppression on LC-tank oscillators. , 2011, , .		0
134	A 200GHz downconverter in 90nm CMOS. , 2011, , .		2
135	A 0.7mW 13b temperature-stable MASH ΔΣ TDC with delay-line assisted calibration. , 2011, , .		7
136	A 1.65W fully integrated 90nm Bulk CMOS Intrinsic Charge Recycling capacitive DC-DC converter: Design & techniques for high power density. , 2011, , .		20
137	A Fully Integrated CMOS 800-mW Four-Phase Semiconstant ON/OFF-Time Step-Down Converter. IEEE Transactions on Power Electronics, 2011, 26, 326-333.	7.9	69
138	Multiple Event Time-to-Digital Conversion-Based Pulse Digitization for a 250 MHz Pulse Radio Ranging Application. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 2614-2622.	5.4	7
139	A 250mV 7.5μW 61dB SNDR CMOS SC ΔΣ modulator using a near-threshold-voltage-biased CMOS inverter technique. , 2011, , .		4
140	A 1.7mW 11b 1–1–1 MASH ΔΣ time-to-digital converter. , 2011, , .		15
141	118GHz fundamental VCO with 7.8% tuning range in 65nm CMOS. , 2011, , .		17
142	A colpitts LC VCO with Miller-capacitance gm enhancing and phase noise reduction techniques. , 2011, , .		10
143	Radiation effects upon the mismatch of identically laid out transistor pairs. , 2011, , .		8
144	A Fully Integrated $Delta Sigma$ ADC in Organic Thin-Film Transistor Technology on Flexible Plastic Foil. IEEE Journal of Solid-State Circuits, 2011, 46, 276-284.	5.4	142

#	Article	IF	Citations
145	Monolithic Capacitive DC-DC Converter With Single Boundaryâ€“Multiphase Control and Voltage Domain Stacking in 90 nm CMOS. IEEE Journal of Solid-State Circuits, 2011, 46, 1715-1727.	5.4	83
146	Design and assessment of a robust voltage amplifier with 2.5 GHz GBW and >100 kGy total dose tolerance. Journal of Instrumentation, 2011, 6, C01076-C01076.	1.2	3
147	Trustworthy Genetic Programming-Based Synthesis of Analog Circuit Topologies Using Hierarchical Domain-Specific Building Blocks. IEEE Transactions on Evolutionary Computation, 2011, 15, 557-570.	10.0	45
148	A 60-GHz CMOS VCO Using Capacitance-Splitting and Gateâ€“Drain Impedance-Balancing Techniques. IEEE Transactions on Microwave Theory and Techniques, 2011, 59, 406-413.	4.6	54
149	A Bandwidth Enhanced Transimpedance Amplifier with Improved Noise Performance. Analog Integrated Circuits and Signal Processing, 2011, 66, 277-283.	1.4	1
150	A monolithic 0.77W/mm² power dense capacitive DC-DC step-down converter in 90nm Bulk CMOS. , 2011, , .		11
151	Organic dual DC-DC upconverter on foil for improved circuit reliability. Electronics Letters, 2011, 47, 278.	1.0	12
152	Comparator-Based Switched-Capacitor Delta-Sigma A/D Converters. , 2011, , 157-176.		3
153	Basic DC-DC Converter Theory. , 2011, , 27-63.		4
154	Implementations. , 2011, , 213-259.		0
155	Control Systems. , 2011, , 169-212.		0
156	Energy Supply and ULP Detection Circuits for an RFID Localization System in 130 nm CMOS. IEEE Journal of Solid-State Circuits, 2010, 45, 1273-1285.	5.4	22
157	Comparison of high impedance input topologies with low EMI susceptibility. Analog Integrated Circuits and Signal Processing, 2010, 65, 299-309.	1.4	6
158	Analog techniques for reliable organic circuit design on foil applied to an 18dB single-stage differential amplifier. Organic Electronics, 2010, 11, 1357-1362.	2.6	37
159	An analog organic first-order CT ΔΣ ADC on a flexible plastic substrate with 26.5dB precision. , 2010, , .		20
160	A high-speed POF receiver with 1 mm integrated photodiode in 180 nm CMOS. , 2010, , .		19
161	A fully integrated 74% efficiency 3.6V to 1.5V 150mW capacitive point-of-load DC/DC-converter. , 2010, , .		15
162	An organic integrated capacitive DC-DC up-converter. , 2010, , .		10

#	Article	IF	Citations
163	Power efficient distributed low-noise amplifier in 90 nm CMOS. , 2010, , .		12
164	A/D Conversion Using Asynchronous Delta-Sigma Modulation and Time-to-Digital Conversion. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 2404-2412.	5.4	65
165	All-digital differential VCO-based A/D conversion. , 2010, , .		25
166	A 0.02mm² 65nm CMOS 30MHz BW all-digital differential VCO-based ADC with 64dB SNDR. , 2010, , .		40
167	A fully integrated gearbox capacitive DC/DC-converter in 90nm CMOS: Optimization, control and measurements. , 2010, , .		27
168	A 90nm CMOS 5-bit 2GS/s DAC for UWB transceivers. , 2010, , .		2
169	A 5.5 Gbit/s optical receiver in 130 nm CMOS with speed-enhanced integrated photodiode. , 2010, , .		11
170	Kuijk Bandgap Voltage Reference With High Immunity to EMI. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 75-79.	3.0	21
171	A Single-Bit 500 kHz-10 MHz Multimode Power-Performance Scalable 83-to-67 dB DR CTÎ”Î£ for SDR in 90 nm Digital CMOS. IEEE Journal of Solid-State Circuits, 2010, 45, 1159-1171.	5.4	51
172	A 10â€“Bit 1.6-GS/s 27-mW Current-Steering D/A Converter With 550-MHz 54-dB SFDR Bandwidth in 130-nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 2870-2879.	5.4	71
173	EMC of Analog Integrated Circuits. Analog Circuits and Signal Processing Series, 2010, , .	0.3	87
174	A 60GHz 15.7mW static frequency divider in 90nm CMOS. , 2010, , .		24
175	Compact Model for Organic Thin-Film Transistor. IEEE Electron Device Letters, 2010, 31, 210-212.	3.9	44
176	EMI-Resistant CMOS Differential Input Stages. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 323-331.	5.4	34
177	A 500 mV 650 pW random number generator in 130 nm CMOS for a UWB localization system. , 2010, , .		8
178	A DMOS integrated 320mW capacitive 12V to 70V DC/DC-converter for LIDAR applications. , 2009, , .		8
179	Massively multi-topology sizing of analog integrated circuits. , 2009, , .		19
180	Distortion in polar modulated CMOS RF power amplifiers. Analog Integrated Circuits and Signal Processing, 2009, 59, 13-20.	1.4	1

#	Article	IF	Citations
181	High-Speed Optical Receivers With Integrated Photodiode in 130 nm CMOS. IEEE Journal of Solid-State Circuits, 2009, 44, 2856-2867.	5.4	64
182	Ultra low power detection circuits in 130nm CMOS for a wireless UWB localization system. , 2009, , .		5
183	A low power mm-wave oscillator using power matching techniques. , 2009, , .		14
184	A single bit 6.8mW 10MHz power-optimized continuous-time ΔΣ with 67dB DR in 90nm CMOS. , 2009, , .		7
185	A Fully Integrated Pinless Long-Range Power Supply with On-Chip Antenna for Scavenging-Based RFID Tag Powering. , 2009, , .		5
186	A gated ring oscillator based parallel-TDC system with digital resolution enhancement. , 2009, , .		3
187	Analysis of fractional spur reduction using ΣΔ-noise cancellation in digital-PLL. , 2009, , .		1
188	An 800mW fully-integrated 130nm CMOS DC-DC step-down multi-phase converter, with on-chip spiral inductors and capacitors. , 2009, , .		24
189	A 1-V 84-dB DR 1-MHz bandwidth cascade 3–1 Delta-Sigma ADC in 65-nm CMOS. , 2009, , .		7
190	A 0.1–5GHz Dual-VCO software-defined ∑Δ frequency synthesizer in 45nm digital CMOS. , 2009, , .		11
191	Ultra-Wideband Pulse-based Radio. , 2009, , .		7
192	Variation-Aware Analog Structural Synthesis. , 2009, , .		19
193	Modeling, Design, Assessment of a 0.4 $mu{hbox {m}}$ SiGe Bipolar VCSEL Driver IC Under $gamma $-Radiation. IEEE Transactions on Nuclear Science, 2009, 56, 1920-1925.	2.0	3
194	An integrated 10A, 2.2ns rise-time laser-diode driver for LIDAR applications. , 2009, , .		15
195	A low power, area efficient limiting amplifier in 90nm CMOS. , 2009, , .		3
196	Design and Analysis of a 90 nm mm-Wave Oscillator Using Inductive-Division LC Tank. IEEE Journal of Solid-State Circuits, 2009, 44, 1950-1958.	5.4	75
197	A 66 muW 86 ppm$/^{circ}$C Fully-Integrated 6 MHz Wienbridge Oscillator With a 172 dB Phase Noise FOM. IEEE Journal of Solid-State Circuits, 2009, 44, 1990-2001.	5.4	54
198	Erratum to â€œA 66 muW 86 ppm/^{circ}C Fully-Integrated 6 MHz Wienbridge Oscillator With a 172 dB Phase Noise FOMâ€•[Jul 09 1990-2001]. IEEE Journal of Solid-State Circuits, 2009, 44, 2868-2868.	5.4	1

#	Article	IF	Citations
199	Erratum to "A 1-V 140-Î¼W 88-dB Audio Sigma-Delta Modulator in 90-nm CMOS". IEEE Journal of Solid-State Circuits, 2009, 44, 3211-3211.	5.4	6
200	A 2mm² 0.1-to-5GHz SDR receiver in 45nm digital CMOS. , 2009, , .		8
201	Power Efficient Reconfigurable Baseband Filters for Multimode Radios. Integrated Circuits and Systems, 2009, , 223-248.	0.2	1
202	A continuous-time delta-sigma modulator for 802.11a/b/g WLAN implemented with a hierarchical bottom-up optimization methodology. Analog Integrated Circuits and Signal Processing, 2008, 55, 37-45.	1.4	5
203	A high speed, low voltage to high voltage level shifter in standard 1.2ÂV 0.13ÂÎ¼m CMOS. Analog Integrated Circuits and Signal Processing, 2008, 55, 85-91.	1.4	15
204	A fully-integrated 0.18μm CMOS DC-DC step-down converter, using a bondwire spiral inductor. , 2008, , .		33
205	An Externally Trimmed Integrated DC Current Regulator Insensitive to Conducted EMI. IEEE Transactions on Electromagnetic Compatibility, 2008, 50, 63-70.	2.2	4
206	A 350-MHz combined TDC-DTC With 61 ps resolution for asynchronous ΔΣ ADC applications. , 2008, , .		6
207	A 11 mW 68dB SFDR 100 MHz bandwidth ΔΣ-DAC based on a 5-bit 1GS/s core in 130nm. , 2008, , .		8
208	A Polar Modulator Using Self-Oscillating Amplifiers and an Injection-Locked Upconversion Mixer. IEEE Journal of Solid-State Circuits, 2008, 43, 460-467.	5.4	9
209	A 130 nm CMOS 6-bit Full Nyquist 3 GS/s DAC. IEEE Journal of Solid-State Circuits, 2008, 43, 2396-2403.	5.4	76
210	Design Considerations for Cascade $Delta Sigma $ ADC's. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 389-393.	3.0	11
211	An instrumentation amplifier input circuit with a high immunity to EMI. , 2008, , .		5
212	A CMOS source-buffered differential input stage with high EMI suppression. , 2008, , .		11
213	A fully-integrated Wienbridge topology for ultra-low-power 86ppm/°C 65nm CMOS 6MHz clock reference with amplitude regulation. , 2008, , .		7
214	A fully-integrated 130nm CMOS DC-DC step-down converter, regulated by a constant on/off-time control system. , 2008, , .		20
215	A 90nm CMOS mm-wave VCO using an LC tank with inductive division. , 2008, , .		6
216	Power efficient 4.5Gbit/s optical receiver in 130nm CMOS with integrated photodiode. , 2008, , .		17

#	Article	IF	Citations
217	Automated extraction of expert knowledge in analog topology selection and sizing. , 2008, , .		7
218	20â€“850â€…MHz low-distortion baseband amplifier in digital CMOS process. Electronics Letters, 2008, 44, 1167.	1.0	1
219	EMI resisting smart-power integrated LIN driver with reduced slope pumping. , 2008, , .		3
220	Area-driven optimisation of switched-capacitor DC/DC converters. Electronics Letters, 2008, 44, 1488.	1.0	25
221	A low-power mixing DAC IR-UWB-receiver. , 2008, , .		2
222	A 100-kHz to 20-MHz Reconfigurable Power-Linearity Optimized G_mâ€“C Biquad in 0.13-mum CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 224-228.	3.0	20
223	A/D conversion using an Asynchronous Delta-Sigma Modulator and a time-to-digital converter. , 2008, , .		27
224	A high-speed fully integrated optical receiver in standard 130nm CMOS. , 2008, , .		2
225	Switched RF Transmitters. , 2008, , 145-162.		0
226	High Voltage xDSL Line Drivers in Nanometer Technologies. , 2008, , 179-203.		2
227	Genetic Programmingwith Reuse of Known Designs for Industrially Scalable, Novel Circuit Design. , 2008, , 159-184.		3
228	Measurement of EMI induced input offset voltage of an operational amplifier. Electronics Letters, 2007, 43, 1088.	1.0	11
229	A 237mW aDSL2+ CO Line Driver in Standard 1.2V 0.13Â¿m CMOS. Digest of Technical Papers - IEEE International Solid-State Circuits Conference, 2007, , .	0.0	12
230	Analysis and Performance Comparison of a Cascade 3-1 Delta-Sigma Topology. , 2007, , .		0
231	Simultaneous Multi-Topology Multi-Objective Sizing Across Thousands of Analog Circuit Topologies. Proceedings - Design Automation Conference, 2007, , .	0.0	3
232	A 8 GHz 77 % efficient discrete quarter-wavelength transmission line integrated in 0.13 Î¼m CMOS. , 2007, , .		0
233	A Design-Optimized Continuous-Time Delta–Sigma ADC for WLAN Applications. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2007, 54, 209-217.	0.1	58
234	A 2.45-GHz 0.13-$mu{hbox {m}}$ CMOS PA With Parallel Amplification. IEEE Journal of Solid-State Circuits, 2007, 42, 551-562.	5.4	69

#	Article	IF	Citations
235	An EMI Resisting LIN Driver in 0.35-micron High-Voltage CMOS. IEEE Journal of Solid-State Circuits, 2007, 42, 1574-1582.	5.4	24
236	Linearity guidelines for g<inf>m</inf>-C biquad filter design using architecture optimization with Volterra analysis. , 2007, , .		1
237	A 130 nm CMOS 6-bit full nyquist 3GS/s DAC. , 2007, , .		4
238	Design and Assessment of a Circuit and Layout Level Radiation Hardened CMOS VCSEL Driver. IEEE Transactions on Nuclear Science, 2007, 54, 1055-1060.	2.0	13
239	A fully integrated wireless power supply for pinless active RFID-devices in 130nm CMOS. , 2007, , .		17
240	A 100kHz – 20MHz reconfigurable nauta g<inf>m</inf>-C biquad low-pass filter in 0.13µm CMOS. , 2007, , .		7
241	A power amplifier driver using self-oscillating pulse-width modulators. Solid-State Circuits Conference, 2008 ESSCIRC 2008 34th European, 2007, , .	0.0	2
242	A linearity and power efficient design strategy for architecture optimization of gm-C biquadratic filters. , 2007, , .		2
243	An integrated DC current regulator with high EMI suppression. Solid-State Circuits Conference, 2008 ESSCIRC 2008 34th European, 2007, , .	0.0	2
244	Pulse based Wideband Radio: Synchronization and Channel Monitoring. , 2007, , .		0
245	An Efficient Methodology for Hierarchical Synthesis of Mixed-Signal Systems with Fully Integrated Building Block Topology Selection. , 2007, , .		11
246	A fully-integrated 0.18µm CMOS DC-DC step-up converter, using a bondwire spiral inductor. Solid-State Circuits Conference, 2008 ESSCIRC 2008 34th European, 2007, , .	0.0	18
247	Transimpedance Amplifier Design. , 2007, , 61-105.		2
248	Optical Receiver Fundamentals. , 2007, , 13-26.		0
249	Standard CMOS Photodiodes. , 2007, , 27-60.		0
250	Post-Amplifier Design. , 2007, , 107-131.		0
251	CMOS Realizations. , 2007, , 133-166.		0
252	A Novel Bootstrapped Switch Design, Applied in a 400 MHz Clocked ΔΣ ADC. , 2006, , .		4

#	Article	IF	Citations
253	Interference and Distortion in Pulsed Ultra Wideband Receivers. , 2006, , .		0
254	A Continuous-Time Delta-Sigma Modulator for 802.11a/b/g WLAN Implemented with a Hierarchical Bottom-up Optimization Methodology. , 2006, , .		2
255	A 10-bit 250-MS/s Binary-Weighted Current-Steering DAC. IEEE Journal of Solid-State Circuits, 2006, 41, 320-329.	5.4	134
256	Introduction to the Special Issue on the 2005 European Solid State Circuits Conference (ESSCIRC). IEEE Journal of Solid-State Circuits, 2006, 41, 1500-1502.	5.4	0
257	A High-Speed 850-nm Optical Receiver Front-End in 0.18-<tex>$muhbox m$</tex>CMOS. IEEE Journal of Solid-State Circuits, 2006, 41, 1606-1614.	5.4	59
258	Application of High-Speed, High-Accuracy Dacs for Generation of Multiple Channels. Analog Integrated Circuits and Signal Processing, 2006, 47, 33-38.	1.4	0
259	Hierarchical bottom--up analog optimization methodology validated by a delta--sigma A/D converter design for the 802.11a/b/g standard. , 2006, , .		10
260	A Gigabit Optical Receiver with Monolithically Integrated Photodiode in 0.18 Â¿m CMOS. Solid-State Circuits Conference, 2008 ESSCIRC 2008 34th European, 2006, , .	0.0	9
261	An EMI resisting LIN driver. , 2006, , .		2
262	<title>A G<formula><inf><roman>m</roman></inf></formula>C filter design methodology for high-speed continuous-time sigma-delta A/D converters in a deep sub-micron technology</title>. , 2005, , .		4
263	ESDâ€“RF co-design methodology for the state of the art RF-CMOS blocks. Microelectronics Reliability, 2005, 45, 255-268.	1.7	11
264	Design of a Class E Power Amplifier with LDMOS in Standard CMOS. Analog Integrated Circuits and Signal Processing, 2005, 44, 17-23.	1.4	1
265	A Fully Integrated Class 1 Bluetooth 0.25 Î¼m CMOS PA. Analog Integrated Circuits and Signal Processing, 2005, 42, 103-112.	1.4	3
266	Current mirror structure insensitive to conducted EMI. Electronics Letters, 2005, 41, 1145.	1.0	36
267	A high-voltage output driver in a 2.5-V 0.25-/spl mu/m CMOS technology. IEEE Journal of Solid-State Circuits, 2005, 40, 576-583.	5.4	71
268	A Fully Integrated CMOS RF Power Amplifier with Parallel Power Combining and Power Control. , 2005, , .		3
269	A 1.75-GHz polar modulated CMOS RF power amplifier for GSM-EDGE. IEEE Journal of Solid-State Circuits, 2005, 40, 2598-2608.	5.4	248
270	<title>CMOS implementation of ultra-wideband systems</title>. , 2005, , .		0

#	Article	IF	Citations
271	Architectures for low power ultra-wideband radio receivers in the 3.1-5GHz band for data rates < 10Mbps. , 2004, , .		28
272	A CAD assisted design and optimisation methodology for over-voltage ESD protection circuits. Microelectronics Reliability, 2004, 44, 1885-1890.	1.7	1
273	A 1-V 140-/spl mu/W 88-dB audio sigma-delta modulator in 90-nm CMOS. IEEE Journal of Solid-State Circuits, 2004, 39, 1809-1818.	5.4	186
274	Parallel-path digital-to-analog converters for Nyquist signal generation. IEEE Journal of Solid-State Circuits, 2004, 39, 1073-1082.	5.4	32
275	High frequency characterization and modelling of the parasitic RC performance of two terminal ESD CMOS protection devices. Microelectronics Reliability, 2003, 43, 1011-1020.	1.7	3
276	High ESD performance, low power CMOS LNA for GPS applications. Journal of Electrostatics, 2003, 59, 179-192.	1.9	7
277	Highly efficient xDSL line drivers in 0.35-Î¼m CMOS using a self-oscillating power amplifier. IEEE Journal of Solid-State Circuits, 2003, 38, 22-29.	5.4	20
278	Design techniques and implementation of an 8-bit 200-MS/s interpolating/averaging CMOS A/D converter. IEEE Journal of Solid-State Circuits, 2003, 38, 483-494.	5.4	34
279	A 1.8-V 6-bit 1.3-GHz flash ADC in 0.25-Î¼m CMOS. IEEE Journal of Solid-State Circuits, 2003, 38, 1115-1122.	5.4	136
280	RF-ESD Co-Design for High Performance CMOS LNAs. , 2003, , 207-226.		3
281	Single-Loop Multi-Bit Sigma-Delta Modulators. , 2003, , 277-306.		0
282	Circuit Design Aspects of Multi-Bit Delta-Sigma Converters. , 2002, , 181-203.		8
283	CMOS. Proceedings - Design Automation Conference, 2002, , .	0.0	11
284	A 700-MHz 1-W fully differential CMOS class-E power amplifier. IEEE Journal of Solid-State Circuits, 2002, 37, 137-141.	5.4	88
285	A 0.8-dB NF ESD-Protected 9-mW CMOS LNA operating at 1.23 GHz [for GPS receiver]. IEEE Journal of Solid-State Circuits, 2002, 37, 760-765.	5.4	71
286	A CMOS monolithic Î”Î£-controlled fractional-N frequency synthesizer for DCS-1800. IEEE Journal of Solid-State Circuits, 2002, 37, 835-844.	5.4	147
287	Low-voltage low-power CMOS-RF transceiver design. IEEE Transactions on Microwave Theory and Techniques, 2002, 50, 281-287.	4.6	72
288	Title is missing!. Analog Integrated Circuits and Signal Processing, 2002, 31, 31-37.	1.4	3

#	Article	IF	Citations
289	Optimizing the Dimensions of Driver and Power Transistor in Switching CMOS RF Amplifiers. Analog Integrated Circuits and Signal Processing, 2002, 32, 177-182.	1.4	3
290	A 2.5 V, 10 GHz Fully Integrated LC-VCO with Integrated High-Q Inductor and 30% Tuning Range. Analog Integrated Circuits and Signal Processing, 2002, 33, 137-144.	1.4	11
291	A 10-bit 1-GSample/s Nyquist current-steering CMOS D/A converter. IEEE Journal of Solid-State Circuits, 2001, 36, 315-324.	5.4	311
292	An Accurate Statistical Yield Model for CMOS Current-Steering D/A Converters. Analog Integrated Circuits and Signal Processing, 2001, 29, 173-180.	1.4	31
293	Title is missing!. Analog Integrated Circuits and Signal Processing, 2001, 28, 141-148.	1.4	1
294	A Single-Chip CMOS Transceiver Front-End for DCS-1800 Wireless Communications. Analog Integrated Circuits and Signal Processing, 2000, 24, 83-99.	1.4	4
295	Fully Integrated Low Phase-Noise VCOs: From Special Processing to Standard CMOS. Analog Integrated Circuits and Signal Processing, 2000, 23, 17-30.	1.4	2
296	Phase noise up-conversion reduction for integrated CMOS VCOs. Electronics Letters, 2000, 36, 857.	1.0	13
297	A high-density, matched hexagonal transistor structure in standard CMOS technology for high-speed applications. IEEE Transactions on Semiconductor Manufacturing, 2000, 13, 167-172.	1.7	23
298	A 2-GHz low-phase-noise integrated LC-VCO set with flicker-noise upconversion minimization. IEEE Journal of Solid-State Circuits, 2000, 35, 1034-1038.	5.4	126
299	A high-performance multibit /spl Delta//spl Sigma/ CMOS ADC. IEEE Journal of Solid-State Circuits, 2000, 35, 1829-1840.	5.4	105
300	A 2-V CMOS cellular transceiver front-end. IEEE Journal of Solid-State Circuits, 2000, 35, 1895-1907.	5.4	103
301	Fully Integrated CMOS Frequency Synthesizers for Wireless Communications. , 2000, , 287-323.		12
302	Optimum MOS power matching by exploiting non-quasistatic effect. Electronics Letters, 1999, 35, 672.	1.0	5
303	MOS noise performance under impedance matching constraints. Electronics Letters, 1999, 35, 1278.	1.0	11
304	A 14-bit intrinsic accuracy Q/sup 2/ random walk CMOS DAC. IEEE Journal of Solid-State Circuits, 1999, 34, 1708-1718.	5.4	252
305	A 1-Gb/s, 0.7-Î¼m CMOS optical receiver with full rail-to-rail output swing. IEEE Journal of Solid-State Circuits, 1999, 34, 971-977.	5.4	87
306	A CMOS dual-channel, 100-MHz to 1.1-GHz transmitter for cable applications. IEEE Journal of Solid-State Circuits, 1999, 34, 1904-1913.	5.4	13

#	Article	IF	Citations
307	Design of Low-Voltage Low-Power CMOS Delta-Sigma A/D Converters. , 1999, , .		40
308	Analog VLSI Design Constraints of Programmable Cellular Neural Networks. Analog Integrated Circuits and Signal Processing, 1998, 15, 251-262.	1.4	2
309	A 2-V, low distortion, 1-GHz CMOS up-conversion mixer. IEEE Journal of Solid-State Circuits, 1998, 33, 359-366.	5.4	19
310	A 15-b resolution 2-MHz Nyquist rate Î”Î£ ADC in a 1-Î¼m CMOS technology. IEEE Journal of Solid-State Circuits, 1998, 33, 1065-1075.	5.4	63
311	A 900-mV low-power Î”Î£ A/D converter with 77-dB dynamic range. IEEE Journal of Solid-State Circuits, 1998, 33, 1887-1897.	5.4	182
312	A 12-bit intrinsic accuracy high-speed CMOS DAC. IEEE Journal of Solid-State Circuits, 1998, 33, 1959-1969.	5.4	274
313	A fully integrated CMOS DCS-1800 frequency synthesizer. IEEE Journal of Solid-State Circuits, 1998, 33, 2054-2065.	5.4	218
314	Analog VLSI Design Constraints of Programmable Cellular Neural Networks. , 1998, , 27-38.		0
315	Influence of die attachment on MOS transistor matching. IEEE Transactions on Semiconductor Manufacturing, 1997, 10, 209-218.	1.7	27
316	A 1-GHz CMOS up-conversion mixer. IEEE Journal of Solid-State Circuits, 1997, 32, 370-376.	5.4	36
317	A 1.8-GHz low-phase-noise CMOS VCO using optimized hollow spiral inductors. IEEE Journal of Solid-State Circuits, 1997, 32, 736-744.	5.4	399
318	A 1.5-V-100-Î¼W Î”Î£ modulator with 12-b dynamic range using the switched-opamp technique. IEEE Journal of Solid-State Circuits, 1997, 32, 943-952.	5.4	71
319	A 50-MHz standard CMOS pulse equalizer for hard disk read channels. IEEE Journal of Solid-State Circuits, 1997, 32, 977-988.	5.4	34
320	Design strategies and decoupling techniques for reducing the effects of electrical interference in mixed-mode IC's. IEEE Journal of Solid-State Circuits, 1997, 32, 1136-1141.	5.4	71
321	High-frequency measurement procedure for fully differential building blocks. IEEE Transactions on Instrumentation and Measurement, 1997, 46, 1039-1043.	4.7	1
322	900 mV differential class AB OTA for switched opamp applications. Electronics Letters, 1997, 33, 1455.	1.0	100
323	Mismatch Characterization of Submicron MOS Transistors. Analog Integrated Circuits and Signal Processing, 1997, 12, 95-106.	1.4	52
324	A 175 Ms/s, 6 b, 160 mW, 3.3 V CMOS A/D converter. IEEE Journal of Solid-State Circuits, 1996, 31, 938-944.	5.4	22

#	Article	IF	Citations
325	A 1.75-GHz/3-V dual-modulus divide-by-128/129 prescaler in 0.7-Î¼m CMOS. IEEE Journal of Solid-State Circuits, 1996, 31, 890-897.	5.4	206
326	EVALUATION OF CNN TEMPLATE ROBUSTNESS TOWARDS VLSI IMPLEMENTATION. International Journal of Circuit Theory and Applications, 1996, 24, 111-120.	2.0	9
327	An oscillator circuit for electrostatically driven silicon-based one-port resonators. Sensors and Actuators A: Physical, 1996, 52, 179-186.	4.1	17
328	A 1.8-GHz CMOS low-phase-noise voltage-controlled oscillator with prescaler. IEEE Journal of Solid-State Circuits, 1995, 30, 1474-1482.	5.4	166
329	A single-chip 900 MHz CMOS receiver front-end with a high performance low-IF topology. IEEE Journal of Solid-State Circuits, 1995, 30, 1483-1492.	5.4	337
330	A programmable analog cellular neural network CMOS chip for high speed image processing. IEEE Journal of Solid-State Circuits, 1995, 30, 235-243.	5.4	99
331	A 1.5 GHz highly linear CMOS downconversion mixer. IEEE Journal of Solid-State Circuits, 1995, 30, 736-742.	5.4	110
332	A CMOS rectifier-integrator for amplitude detection in hard disk servo loops. IEEE Journal of Solid-State Circuits, 1995, 30, 743-751.	5.4	39
333	1.1 GHz oscillator using bondwire inductance. Electronics Letters, 1994, 30, 244-245.	1.0	21
334	A CMOS 18 THzÎ© 248 Mb/s transimpedance amplifier and 155 Mb/s LED-driver for low cost optical fiber links. IEEE Journal of Solid-State Circuits, 1994, 29, 1552-1559.	5.4	88
335	Switched-opamp: an approach to realize full CMOS switched-capacitor circuits at very low power supply voltages. IEEE Journal of Solid-State Circuits, 1994, 29, 936-942.	5.4	263
336	CMOS LED-driver and PIN-receiver for fiber optical communication at 155 Mbit/s. Annales Des Telecommunications/Annals of Telecommunications, 1993, 48, 148-152.	2.5	1
337	Full CMOS continuous time filters for GSM applications. Annales Des Telecommunications/Annals of Telecommunications, 1993, 48, 224-232.	2.5	2
338	CMOS LED driver and PIN receiver for fiber optical communication at 150 mbit/sec. Analog Integrated Circuits and Signal Processing, 1993, 4, 31-35.	1.4	6
339	High-Performance CMOS Continuous-Time Filters. , 1993, , .		66
340	High-Performance Realizations of Continuous-Time Filters. , 1993, , 177-220.		1
341	A 1-GHz single-chip quadrature modulator. IEEE Journal of Solid-State Circuits, 1992, 27, 1194-1197.	5.4	39
342	A 10.7-MHz 68-dB SNR CMOS continuous-time filter with on-chip automatic tuning. IEEE Journal of Solid-State Circuits, 1992, 27, 1843-1853.	5.4	129

#	Article	IF	Citations
343	Design techniques for high-performance full-CMOS OTA-RC continuous-time filters. IEEE Journal of Solid-State Circuits, 1992, 27, 993-1001.	5.4	40
344	Full analog CMOS integration of very large time constants for synaptic transfer in neural networks. Analog Integrated Circuits and Signal Processing, 1992, 2, 281-295.	1.4	31
345	ECL-CMOS and CMOS-ECL interface in 1.2- mu m CMOS for 150-MHz digital ECL data transmission systems. IEEE Journal of Solid-State Circuits, 1991, 26, 18-24.	5.4	20
346	A first-order current-steering sigma-delta modulator. IEEE Journal of Solid-State Circuits, 1991, 26, 176-183.	5.4	29
347	A large-signal very low-distortion transconductor for high-frequency continuous-time filters. IEEE Journal of Solid-State Circuits, 1991, 26, 946-955.	5.4	79
348	Design considerations of high-dynamic-range wide-band amplifiers in BiCMOS technology. IEEE Journal of Solid-State Circuits, 1991, 26, 1681-1688.	5.4	8
349	Low-noise monolithic amplifier design: Bipolar versus CMOS. Analog Integrated Circuits and Signal Processing, 1991, 1, 9-19.	1.4	16
350	High frequency saturated CMOS floating resistor for fully-differential analogue signal processors. Electronics Letters, 1991, 27, 1609.	1.0	11
351	Power supply rejection ratio in operational transconductance amplifiers. IEEE Transactions on Circuits and Systems, 1990, 37, 1077-1084.	0.9	65
352	Performance of ECL-compatible 75Î© line driver/receiver realised in a 1.2Î¼m CMOS technology. Electronics Letters, 1990, 26, 764-766.	1.0	1
353	Low-power monolithic signal-conditioning system. IEEE Journal of Solid-State Circuits, 1990, 25, 609-612.	5.4	15
354	Very linear CMOS floating resistor. Electronics Letters, 1990, 26, 1610.	1.0	14
355	Design and implementation of a CMOS VCXO for FM stereo decoders. IEEE Journal of Solid-State Circuits, 1988, 23, 784-793.	5.4	8
356	A CMOS temperature-compensated current reference. IEEE Journal of Solid-State Circuits, 1988, 23, 821-824.	5.4	111
357	High-speed accurate CMOS comparator. Electronics Letters, 1988, 24, 1027.	1.0	11
358	High accuracy pipeline D/A convertor configuration. Electronics Letters, 1988, 24, 272.	1.0	6
359	A micropower fourth-order elliptical switched-capacitor low-pass filter. IEEE Journal of Solid-State Circuits, 1987, 22, 164-173.	5.4	11
360	A high-dynamic-range CMOS op amp with low-distortion output structure. IEEE Journal of Solid-State Circuits, 1987, 22, 1204-1207.	5.4	32

#	Article	IF	Citations
361	A micropower low-noise monolithic instrumentation amplifier for medical purposes. IEEE Journal of Solid-State Circuits, 1987, 22, 1163-1168.	5.4	450
362	Noise power spectrum density analysis of planar Ag/AgCl electrodes. Sensors and Actuators, 1987, 12, 185-192.	1.7	7
363	Mixed-Signal CMOS RF Integrated Circuits. , 0, , .		0