Michiel S J Steyaert

List of Publications by Year
in descending order

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363	10,187	36303	56724
papers	citations	51 h-index	83 g-index

388	388	388	3838
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A micropower low-noise monolithic instrumentation amplifier for medical purposes. IEEE Journal of Solid-State Circuits, 1987, 22, 1163-1168.	5.4	450
2	A 1.8-GHz low-phase-noise CMOS VCO using optimized hollow spiral inductors. IEEE Journal of Solid-State Circuits, 1997, 32, 736-744.	5.4	399
3	A single-chip 900 MHz CMOS receiver front-end with a high performance low-IF topology. IEEE Journal of Solid-State Circuits, 1995, 30, 1483-1492.	5.4	337
4	A 10-bit 1-GSample/s Nyquist current-steering CMOS D/A converter. IEEE Journal of Solid-State Circuits, 2001, 36, 315-324.	5.4	311
5	A 12-bit intrinsic accuracy high-speed CMOS DAC. IEEE Journal of Solid-State Circuits, 1998, 33, 1959-1969.	5.4	274
6	Switched-opamp: an approach to realize full CMOS switched-capacitor circuits at very low power supply voltages. IEEE Journal of Solid-State Circuits, 1994, 29, 936-942.	5.4	263
7	A 14-bit intrinsic accuracy Q/sup 2/ random walk CMOS DAC. IEEE Journal of Solid-State Circuits, 1999, 34, 1708-1718.	5.4	252
8	A 1.75-GHz polar modulated CMOS RF power amplifier for GSM-EDGE. IEEE Journal of Solid-State Circuits, 2005, 40, 2598-2608.	5.4	248
9	A fully integrated CMOS DCS-1800 frequency synthesizer. IEEE Journal of Solid-State Circuits, 1998, 33, 2054-2065.	5.4	218
10	A 1.75-GHz/3-V dual-modulus divide-by-128/129 prescaler in 0.7-Î¼m CMOS. IEEE Journal of Solid-State Circuits, 1996, 31, 890-897.	5.4	206
11	A 1-V 140-/spl mu/W 88-dB audio sigma-delta modulator in 90-nm CMOS. IEEE Journal of Solid-State Circuits, 2004, 39, 1809-1818.	5.4	186
12	A 900-mV low-power Î”Î£ A/D converter with 77-dB dynamic range. IEEE Journal of Solid-State Circuits, 1998, 33, 1887-1897.	5.4	182
13	A 1.8-GHz CMOS low-phase-noise voltage-controlled oscillator with prescaler. IEEE Journal of Solid-State Circuits, 1995, 30, 1474-1482.	5.4	166
14	A CMOS monolithic Î”Î£-controlled fractional-N frequency synthesizer for DCS-1800. IEEE Journal of Solid-State Circuits, 2002, 37, 835-844.	5.4	147
15	A Fully Integrated $Delta Sigma$ ADC in Organic Thin-Film Transistor Technology on Flexible Plastic Foil. IEEE Journal of Solid-State Circuits, 2011, 46, 276-284.	5.4	142
16	A 1.8-V 6-bit 1.3-GHz flash ADC in 0.25-Î¼m CMOS. IEEE Journal of Solid-State Circuits, 2003, 38, 1115-1122.	5.4	136
17	A 10-bit 250-MS/s Binary-Weighted Current-Steering DAC. IEEE Journal of Solid-State Circuits, 2006, 41, 320-329.	5.4	134
18	A 10.7-MHz 68-dB SNR CMOS continuous-time filter with on-chip automatic tuning. IEEE Journal of Solid-State Circuits, 1992, 27, 1843-1853.	5.4	129

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19	A 2-GHz low-phase-noise integrated LC-VCO set with flicker-noise upconversion minimization. IEEE Journal of Solid-State Circuits, 2000, 35, 1034-1038.	5.4	126
20	A CMOS temperature-compensated current reference. IEEE Journal of Solid-State Circuits, 1988, 23, 821-824.	5.4	111
21	A 1.5 GHz highly linear CMOS downconversion mixer. IEEE Journal of Solid-State Circuits, 1995, 30, 736-742.	5.4	110
22	A high-performance multibit /spl Delta//spl Sigma/ CMOS ADC. IEEE Journal of Solid-State Circuits, 2000, 35, 1829-1840.	5.4	105
23	A 2-V CMOS cellular transceiver front-end. IEEE Journal of Solid-State Circuits, 2000, 35, 1895-1907.	5.4	103
24	A 250 mV 7.5 Î¼W 61 dB SNDR SC Î”Î£ Modulator Using Near-Threshold-Voltage-Biased Inverter Amplifiers in 130 nm CMOS. IEEE Journal of Solid-State Circuits, 2012, 47, 709-721.	5.4	101
25	900 mV differential class AB OTA for switched opamp applications. Electronics Letters, 1997, 33, 1455.	1.0	100
26	A programmable analog cellular neural network CMOS chip for high speed image processing. IEEE Journal of Solid-State Circuits, 1995, 30, 235-243.	5.4	99
27	A CMOS 18 THzÎ© 248 Mb/s transimpedance amplifier and 155 Mb/s LED-driver for low cost optical fiber links. IEEE Journal of Solid-State Circuits, 1994, 29, 1552-1559.	5.4	88
28	A 700-MHz 1-W fully differential CMOS class-E power amplifier. IEEE Journal of Solid-State Circuits, 2002, 37, 137-141.	5.4	88
29	A 1-Gb/s, 0.7-Î¼m CMOS optical receiver with full rail-to-rail output swing. IEEE Journal of Solid-State Circuits, 1999, 34, 971-977.	5.4	87
30	EMC of Analog Integrated Circuits. Analog Circuits and Signal Processing Series, 2010, , .	0.3	87
31	Monolithic Capacitive DC-DC Converter With Single Boundaryâ€“Multiphase Control and Voltage Domain Stacking in 90 nm CMOS. IEEE Journal of Solid-State Circuits, 2011, 46, 1715-1727.	5.4	83
32	A large-signal very low-distortion transconductor for high-frequency continuous-time filters. IEEE Journal of Solid-State Circuits, 1991, 26, 946-955.	5.4	79
33	A 130 nm CMOS 6-bit Full Nyquist 3 GS/s DAC. IEEE Journal of Solid-State Circuits, 2008, 43, 2396-2403.	5.4	76
34	Design and Analysis of a 90 nm mm-Wave Oscillator Using Inductive-Division LC Tank. IEEE Journal of Solid-State Circuits, 2009, 44, 1950-1958.	5.4	75
35	Low-voltage low-power CMOS-RF transceiver design. IEEE Transactions on Microwave Theory and Techniques, 2002, 50, 281-287.	4.6	72
36	A 1.5-V-100-Î¼W Î”Î£ modulator with 12-b dynamic range using the switched-opamp technique. IEEE Journal of Solid-State Circuits, 1997, 32, 943-952.	5.4	71

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37	Design strategies and decoupling techniques for reducing the effects of electrical interference in mixed-mode IC's. IEEE Journal of Solid-State Circuits, 1997, 32, 1136-1141.	5.4	71
38	A 0.8-dB NF ESD-Protected 9-mW CMOS LNA operating at 1.23 GHz [for GPS receiver]. IEEE Journal of Solid-State Circuits, 2002, 37, 760-765.	5.4	71
39	A high-voltage output driver in a 2.5-V 0.25-/spl mu/m CMOS technology. IEEE Journal of Solid-State Circuits, 2005, 40, 576-583.	5.4	71
40	A 10â€“Bit 1.6-GS/s 27-mW Current-Steering D/A Converter With 550-MHz 54-dB SFDR Bandwidth in 130-nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 2870-2879.	5.4	71
41	A 2.45-GHz 0.13-$mu{hbox {m}}$ CMOS PA With Parallel Amplification. IEEE Journal of Solid-State Circuits, 2007, 42, 551-562.	5.4	69
42	A Fully Integrated CMOS 800-mW Four-Phase Semiconstant ON/OFF-Time Step-Down Converter. IEEE Transactions on Power Electronics, 2011, 26, 326-333.	7.9	69
43	A 1.25-GS/s 7-b SAR ADC With 36.4-dB SNDR at 5 GHz Using Switch-Bootstrapping, USPC DAC and Triple-Tail Comparator in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2018, 53, 1889-1901.	5.4	66
44	High-Performance CMOS Continuous-Time Filters. , 1993, , .		66
45	Power supply rejection ratio in operational transconductance amplifiers. IEEE Transactions on Circuits and Systems, 1990, 37, 1077-1084.	0.9	65
46	A/D Conversion Using Asynchronous Delta-Sigma Modulation and Time-to-Digital Conversion. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 2404-2412.	5.4	65
47	High-Speed Optical Receivers With Integrated Photodiode in 130 nm CMOS. IEEE Journal of Solid-State Circuits, 2009, 44, 2856-2867.	5.4	64
48	A 15-b resolution 2-MHz Nyquist rate Î”Î£ ADC in a 1-Î¼m CMOS technology. IEEE Journal of Solid-State Circuits, 1998, 33, 1065-1075.	5.4	63
49	A High-Speed 850-nm Optical Receiver Front-End in 0.18-<tex>$muhbox m$</tex>CMOS. IEEE Journal of Solid-State Circuits, 2006, 41, 1606-1614.	5.4	59
50	A Design-Optimized Continuous-Time Delta–Sigma ADC for WLAN Applications. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2007, 54, 209-217.	0.1	58
51	Fully Integrated Wide Input Voltage Range Capacitive DC-DC Converters: The Folding Dickson Converter. IEEE Journal of Solid-State Circuits, 2015, 50, 1560-1570.	5.4	58
52	A 66 muW 86 ppm$/^{circ}$C Fully-Integrated 6 MHz Wienbridge Oscillator With a 172 dB Phase Noise FOM. IEEE Journal of Solid-State Circuits, 2009, 44, 1990-2001.	5.4	54
53	A 60-GHz CMOS VCO Using Capacitance-Splitting and Gateâ€“Drain Impedance-Balancing Techniques. IEEE Transactions on Microwave Theory and Techniques, 2011, 59, 406-413.	4.6	54
54	Mismatch Characterization of Submicron MOS Transistors. Analog Integrated Circuits and Signal Processing, 1997, 12, 95-106.	1.4	52

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55	Scalable Parasitic Charge Redistribution: Design of High-Efficiency Fully Integrated Switched-Capacitor DCâ€“DC Converters. IEEE Journal of Solid-State Circuits, 2016, 51, 2843-2853.	5.4	52
56	A Single-Bit 500 kHz-10 MHz Multimode Power-Performance Scalable 83-to-67 dB DR CTÎ”Î£ for SDR in 90 nm Digital CMOS. IEEE Journal of Solid-State Circuits, 2010, 45, 1159-1171.	5.4	51
57	1-1-1 MASH $Delta Sigma$ Time-to-Digital Converters With 6 ps Resolution and Third-Order Noise-Shaping. IEEE Journal of Solid-State Circuits, 2012, 47, 2093-2106.	5.4	50
58	Analog Building Blocks for Organic Smart Sensor Systems in Organic Thin-Film Transistor Technology on Flexible Plastic Foil. IEEE Journal of Solid-State Circuits, 2012, 47, 1712-1720.	5.4	48
59	Comparison of a 65 nm CMOS Ring- and LC-Oscillator Based PLL in Terms of TID and SEU Sensitivity. IEEE Transactions on Nuclear Science, 2017, 64, 245-252.	2.0	46
60	Trustworthy Genetic Programming-Based Synthesis of Analog Circuit Topologies Using Hierarchical Domain-Specific Building Blocks. IEEE Transactions on Evolutionary Computation, 2011, 15, 557-570.	10.0	45
61	Compact Model for Organic Thin-Film Transistor. IEEE Electron Device Letters, 2010, 31, 210-212.	3.9	44
62	A 63,000 Q-factor relaxation oscillator with switched-capacitor integrated error feedback. , 2013, , .		42
63	Design of Soft-Charging Switched-Capacitor DCâ€“DC Converters Using Stage Outphasing and Multiphase Soft-Charging. IEEE Journal of Solid-State Circuits, 2017, 52, 3132-3141.	5.4	42
64	A Light-Load-Efficient 11/1 Switched-Capacitor DC-DC Converter With 94.7% Efficiency While Delivering 100 mW at 3.3 V. IEEE Journal of Solid-State Circuits, 2015, 50, 2849-2860.	5.4	41
65	12.2 A 94.6%-efficiency fully integrated switched-capacitor DC-DC converter in baseline 40nm CMOS using scalable parasitic charge redistribution. , 2016, , .		41
66	Design techniques for high-performance full-CMOS OTA-RC continuous-time filters. IEEE Journal of Solid-State Circuits, 1992, 27, 993-1001.	5.4	40
67	A 0.02mm² 65nm CMOS 30MHz BW all-digital differential VCO-based ADC with 64dB SNDR. , 2010, , .		40
68	Design of Low-Voltage Low-Power CMOS Delta-Sigma A/D Converters. , 1999, , .		40
69	A 1-GHz single-chip quadrature modulator. IEEE Journal of Solid-State Circuits, 1992, 27, 1194-1197.	5.4	39
70	A CMOS rectifier-integrator for amplitude detection in hard disk servo loops. IEEE Journal of Solid-State Circuits, 1995, 30, 743-751.	5.4	39
71	A 5-GS/s 158.6-mW 9.4-ENOB Passive-Sampling Time-Interleaved Three-Stage Pipelined-SAR ADC With Analog-Digital Corrections in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2020, , 1-12.	5.4	39
72	CMOS Integrated Capacitive DC-DC Converters. , 2013, , .		38

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73	Analog techniques for reliable organic circuit design on foil applied to an 18dB single-stage differential amplifier. Organic Electronics, 2010, 11, 1357-1362.	2.6	37
74	A 1-GHz CMOS up-conversion mixer. IEEE Journal of Solid-State Circuits, 1997, 32, 370-376.	5.4	36
75	Current mirror structure insensitive to conducted EMI. Electronics Letters, 2005, 41, 1145.	1.0	36
76	A 50-MHz standard CMOS pulse equalizer for hard disk read channels. IEEE Journal of Solid-State Circuits, 1997, 32, 977-988.	5.4	34
77	Design techniques and implementation of an 8-bit 200-MS/s interpolating/averaging CMOS A/D converter. IEEE Journal of Solid-State Circuits, 2003, 38, 483-494.	5.4	34
78	EMI-Resistant CMOS Differential Input Stages. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 323-331.	5.4	34
79	A 2.56-GHz SEU Radiation Hard LC -Tank VCO for High-Speed Communication Links in 65-nm CMOS Technology. IEEE Transactions on Nuclear Science, 2018, 65, 407-412.	2.0	34
80	A fully-integrated 0.18μm CMOS DC-DC step-down converter, using a bondwire spiral inductor. , 2008, , .		33
81	A high-dynamic-range CMOS op amp with low-distortion output structure. IEEE Journal of Solid-State Circuits, 1987, 22, 1204-1207.	5.4	32
82	Parallel-path digital-to-analog converters for Nyquist signal generation. IEEE Journal of Solid-State Circuits, 2004, 39, 1073-1082.	5.4	32
83	Full analog CMOS integration of very large time constants for synaptic transfer in neural networks. Analog Integrated Circuits and Signal Processing, 1992, 2, 281-295.	1.4	31
84	An Accurate Statistical Yield Model for CMOS Current-Steering D/A Converters. Analog Integrated Circuits and Signal Processing, 2001, 29, 173-180.	1.4	31
85	A first-order current-steering sigma-delta modulator. IEEE Journal of Solid-State Circuits, 1991, 26, 176-183.	5.4	29
86	Wavelength Locking of a Si Ring Modulator Using an Integrated Drop-Port OMA Monitoring Circuit. IEEE Journal of Solid-State Circuits, 2016, 51, 2328-2344.	5.4	29
87	Architectures for low power ultra-wideband radio receivers in the 3.1-5GHz band for data rates < 10Mbps. , 2004, , .		28
88	Influence of die attachment on MOS transistor matching. IEEE Transactions on Semiconductor Manufacturing, 1997, 10, 209-218.	1.7	27
89	A/D conversion using an Asynchronous Delta-Sigma Modulator and a time-to-digital converter. , 2008, , .		27
90	A fully integrated gearbox capacitive DC/DC-converter in 90nm CMOS: Optimization, control and measurements. , 2010, , .		27

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91	A 1.65 W fully integrated 90 nm bulk cmos capacitive DC-DC converter with intrinsic charge recycling. IEEE Transactions on Power Electronics, 2013, 28, 4327-4334.	7.9	26
92	Area-driven optimisation of switched-capacitor DC/DC converters. Electronics Letters, 2008, 44, 1488.	1.0	25
93	All-digital differential VCO-based A/D conversion. , 2010, , .		25
94	An EMI Resisting LIN Driver in 0.35-micron High-Voltage CMOS. IEEE Journal of Solid-State Circuits, 2007, 42, 1574-1582.	5.4	24
95	An 800mW fully-integrated 130nm CMOS DC-DC step-down multi-phase converter, with on-chip spiral inductors and capacitors. , 2009, , .		24
96	A 60GHz 15.7mW static frequency divider in 90nm CMOS. , 2010, , .		24
97	Design of Single-Topology Continuously Scalable-Conversion-Ratio Switched- Capacitor DCâ€“DC Converters. IEEE Journal of Solid-State Circuits, 2019, 54, 1039-1047.	5.4	24
98	A high-density, matched hexagonal transistor structure in standard CMOS technology for high-speed applications. IEEE Transactions on Semiconductor Manufacturing, 2000, 13, 167-172.	1.7	23
99	Design and Assessment of a 6 ps-Resolution Time-to-Digital Converter With 5 MGy Gamma-Dose Tolerance for LIDAR Application. IEEE Transactions on Nuclear Science, 2012, 59, 1382-1389.	2.0	23
100	A 175 Ms/s, 6 b, 160 mW, 3.3 V CMOS A/D converter. IEEE Journal of Solid-State Circuits, 1996, 31, 938-944.	5.4	22
101	Energy Supply and ULP Detection Circuits for an RFID Localization System in 130 nm CMOS. IEEE Journal of Solid-State Circuits, 2010, 45, 1273-1285.	5.4	22
102	A 4.5 MGy TID-Tolerant CMOS Bandgap Reference Circuit Using a Dynamic Base Leakage Compensation Technique. IEEE Transactions on Nuclear Science, 2013, 60, 2819-2824.	2.0	22
103	1.1 GHz oscillator using bondwire inductance. Electronics Letters, 1994, 30, 244-245.	1.0	21
104	Kuijk Bandgap Voltage Reference With High Immunity to EMI. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 75-79.	3.0	21
105	A 13.5-Gb/s 5-mV-Sensitivity 26.8-ps-CLKâ€“OUT Delay Triple-Latch Feedforward Dynamic Comparator in 28-nm CMOS. IEEE Solid-State Circuits Letters, 2019, 2, 167-170.	2.0	21
106	ECL-CMOS and CMOS-ECL interface in 1.2- mu m CMOS for 150-MHz digital ECL data transmission systems. IEEE Journal of Solid-State Circuits, 1991, 26, 18-24.	5.4	20
107	Highly efficient xDSL line drivers in 0.35-Î¼m CMOS using a self-oscillating power amplifier. IEEE Journal of Solid-State Circuits, 2003, 38, 22-29.	5.4	20
108	A fully-integrated 130nm CMOS DC-DC step-down converter, regulated by a constant on/off-time control system. , 2008, , .		20

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109	A 100-kHz to 20-MHz Reconfigurable Power-Linearity Optimized G_mâ€“C Biquad in 0.13-mum CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 224-228.	3.0	20
110	An analog organic first-order CT ΔΣ ADC on a flexible plastic substrate with 26.5dB precision. , 2010, , .		20
111	A 1.65W fully integrated 90nm Bulk CMOS Intrinsic Charge Recycling capacitive DC-DC converter: Design & techniques for high power density. , 2011, , .		20
112	A 2-V, low distortion, 1-GHz CMOS up-conversion mixer. IEEE Journal of Solid-State Circuits, 1998, 33, 359-366.	5.4	19
113	Massively multi-topology sizing of analog integrated circuits. , 2009, , .		19
114	Variation-Aware Analog Structural Synthesis. , 2009, , .		19
115	A high-speed POF receiver with 1 mm integrated photodiode in 180 nm CMOS. , 2010, , .		19
116	DC-DC converter assisted two-stage amplifier in organic thin-film transistor technology on foil. , 2011, , .		19
117	When hardware is free, power is expensive! Is integrated power management the solution?. , 2015, , .		19
118	A fully-integrated 0.18µm CMOS DC-DC step-up converter, using a bondwire spiral inductor. Solid-State Circuits Conference, 2008 ESSCIRC 2008 34th European, 2007, , .	0.0	18
119	A single-event upset robust, 2.2 GHz to 3.2 GHz, 345 fs jitter PLL with triple-modular redundant phase detector in 65 nm CMOS. , 2016, , .		18
120	An oscillator circuit for electrostatically driven silicon-based one-port resonators. Sensors and Actuators A: Physical, 1996, 52, 179-186.	4.1	17
121	A fully integrated wireless power supply for pinless active RFID-devices in 130nm CMOS. , 2007, , .		17
122	Power efficient 4.5Gbit/s optical receiver in 130nm CMOS with integrated photodiode. , 2008, , .		17
123	118GHz fundamental VCO with 7.8% tuning range in 65nm CMOS. , 2011, , .		17
124	Low-noise monolithic amplifier design: Bipolar versus CMOS. Analog Integrated Circuits and Signal Processing, 1991, 1, 9-19.	1.4	16
125	Monolithic switched-capacitor DC-DC towards high voltage conversion ratios. , 2014, , .		16
126	Low-power monolithic signal-conditioning system. IEEE Journal of Solid-State Circuits, 1990, 25, 609-612.	5.4	15

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127	A high speed, low voltage to high voltage level shifter in standard 1.2ÂV 0.13ÂÎ¼m CMOS. Analog Integrated Circuits and Signal Processing, 2008, 55, 85-91.	1.4	15
128	An integrated 10A, 2.2ns rise-time laser-diode driver for LIDAR applications. , 2009, , .		15
129	A fully integrated 74% efficiency 3.6V to 1.5V 150mW capacitive point-of-load DC/DC-converter. , 2010, , .		15
130	A 1.7mW 11b 1–1–1 MASH ΔΣ time-to-digital converter. , 2011, , .		15
131	Very linear CMOS floating resistor. Electronics Letters, 1990, 26, 1610.	1.0	14
132	A low power mm-wave oscillator using power matching techniques. , 2009, , .		14
133	Analog Organic Electronics. , 2013, , .		14
134	22.5 A 4×20Gb/s WDM ring-based hybrid CMOS silicon photonics transceiver. , 2015, , .		14
135	10.1 A 1.1W/mm²-power-density 82%-efficiency fully integrated 3âˆ¶1 Switched-Capacitor DC-DC converter in baseline 28nm CMOS using Stage Outphasing and Multiphase Soft-Charging. , 2017, , .		14
136	A CMOS dual-channel, 100-MHz to 1.1-GHz transmitter for cable applications. IEEE Journal of Solid-State Circuits, 1999, 34, 1904-1913.	5.4	13
137	Phase noise up-conversion reduction for integrated CMOS VCOs. Electronics Letters, 2000, 36, 857.	1.0	13
138	Design and Assessment of a Circuit and Layout Level Radiation Hardened CMOS VCSEL Driver. IEEE Transactions on Nuclear Science, 2007, 54, 1055-1060.	2.0	13
139	Dual-output capacitive DC-DC converter with power distribution regulator in 90 nm CMOS. , 2012, , .		13
140	A Wideband Low-Noise Variable-Gain Amplifier With a 3.4 dB NF and up to 45 dB Gain Tuning Range in 130-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1104-1108.	3.0	13
141	A 237mW aDSL2+ CO Line Driver in Standard 1.2V 0.13Â¿m CMOS. Digest of Technical Papers - IEEE International Solid-State Circuits Conference, 2007, , .	0.0	12
142	Power efficient distributed low-noise amplifier in 90 nm CMOS. , 2010, , .		12
143	Organic dual DC-DC upconverter on foil for improved circuit reliability. Electronics Letters, 2011, 47, 278.	1.0	12
144	A folding dickson-based fully integrated wide input range capacitive DC-DC converter achieving Vout/2-resolution and 71% average efficiency. , 2015, , .		12

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145	Fully Integrated CMOS Frequency Synthesizers for Wireless Communications. , 2000, , 287-323.		12
146	A micropower fourth-order elliptical switched-capacitor low-pass filter. IEEE Journal of Solid-State Circuits, 1987, 22, 164-173.	5.4	11
147	High-speed accurate CMOS comparator. Electronics Letters, 1988, 24, 1027.	1.0	11
148	High frequency saturated CMOS floating resistor for fully-differential analogue signal processors. Electronics Letters, 1991, 27, 1609.	1.0	11
149	MOS noise performance under impedance matching constraints. Electronics Letters, 1999, 35, 1278.	1.0	11
150	CMOS. Proceedings - Design Automation Conference, 2002, , .	0.0	11
151	A 2.5 V, 10 GHz Fully Integrated LC-VCO with Integrated High-Q Inductor and 30% Tuning Range. Analog Integrated Circuits and Signal Processing, 2002, 33, 137-144.	1.4	11
152	ESDâ€“RF co-design methodology for the state of the art RF-CMOS blocks. Microelectronics Reliability, 2005, 45, 255-268.	1.7	11
153	Measurement of EMI induced input offset voltage of an operational amplifier. Electronics Letters, 2007, 43, 1088.	1.0	11
154	An Efficient Methodology for Hierarchical Synthesis of Mixed-Signal Systems with Fully Integrated Building Block Topology Selection. , 2007, , .		11
155	Design Considerations for Cascade $Delta Sigma $ ADC's. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 389-393.	3.0	11
156	A CMOS source-buffered differential input stage with high EMI suppression. , 2008, , .		11
157	A 0.1–5GHz Dual-VCO software-defined ∑Δ frequency synthesizer in 45nm digital CMOS. , 2009, , .		11
158	A 5.5 Gbit/s optical receiver in 130 nm CMOS with speed-enhanced integrated photodiode. , 2010, , .		11
159	A monolithic 0.77W/mm² power dense capacitive DC-DC step-down converter in 90nm Bulk CMOS. , 2011, , .		11
160	3.3 A 5GS/s 158.6mW 12b Passive-Sampling 8Ã—-Interleaved Hybrid ADC with 9.4 ENOB and 160.5dB FoM<inf>S</inf> in 28nm CMOS. , 2019, , .		11
161	A 13.5-Gb/s 5-mV-Sensitivity 26.8-ps-CLKâ€“OUT Delay Triple-Latch Feedforward Dynamic Comparator in 28-nm CMOS. , 2019, , .		11
162	Hierarchical bottom-up analog optimization methodology validated by a delta-sigma A/D converter design for the 802.11a/b/g standard. , 2006, , .		10

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163	An organic integrated capacitive DC-DC up-converter. , 2010, , .		10
164	A colpitts LC VCO with Miller-capacitance gm enhancing and phase noise reduction techniques. , 2011, , .		10
165	A Self-Calibrated Bangâ€“Bang Phase Detector for Low-Offset Time Signal Processing. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 453-457.	3.0	10
166	Schottky Photodiodes in Bulk CMOS for High-Speed 1310/1550 nm Optical Receivers. IEEE Journal of Selected Topics in Quantum Electronics, 2018, 24, 1-8.	2.9	10
167	EVALUATION OF CNN TEMPLATE ROBUSTNESS TOWARDS VLSI IMPLEMENTATION. International Journal of Circuit Theory and Applications, 1996, 24, 111-120.	2.0	9
168	A Gigabit Optical Receiver with Monolithically Integrated Photodiode in 0.18 Â¿m CMOS. Solid-State Circuits Conference, 2008 ESSCIRC 2008 34th European, 2006, , .	0.0	9
169	A Polar Modulator Using Self-Oscillating Amplifiers and an Injection-Locked Upconversion Mixer. IEEE Journal of Solid-State Circuits, 2008, 43, 460-467.	5.4	9
170	On-chip gain reconfigurable 1.2V 24μW chopping instrumentation amplifier with automatic resistor matching in 0.13μm CMOS. , 2012, , .		9
171	A 265 V<formula formulatype="inline"><tex Notation="TeX">$_{m RMS}$</tex></formula> Mains Interface Integrated in 0.35 <formula formulatype="inline"><tex Notation="TeX">mu</tex></formula>m CMOS. IEEE Journal of Solid-State Circuits, 2013, 48, 1558-1564.	5.4	9
172	A 120GHz quadrature frequency generator with 16.2GHz tuning range in 45nm CMOS. , 2013, , .		9
173	17 bit 4.35mW 1kHz Delta Sigma ADC and 256-to-1 multiplexer for remote handling instrumentation equipment. Fusion Engineering and Design, 2013, 88, 1942-1946.	1.9	9
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