Chip-Hong Chang

List of Publications by Year
in descending order

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288 papers	4,803 citations	126907 33 h-index	149698 56 g-index
292 all docs	292 docs citations	292 times ranked	2185 citing authors

#	Article	IF	Citations
1	A New Energy-Efficient and High Throughput Two-Phase Multi-Bit per Cycle Ring Oscillator-Based True Random Number Generator. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 272-283.	5.4	27
2	An Efficient Full Hardware Implementation of Extended Merkle Signature Scheme. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 682-693.	5.4	6
3	A New PUF Based Lock and Key Solution for Secure In-Field Testing of Cryptographic Chips. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 1095-1105.	4.6	25
4	Stealthy and Robust Glitch Injection Attack on Deep Learning Accelerator for Target With Variational Viewpoint. IEEE Transactions on Information Forensics and Security, 2021, 16, 1928-1942.	6.9	5
5	Live Demonstration: Event-Driven Physical Unclonable Function for Proactive Monitoring System by Dynamic Vision Sensor. , 2021, , .		0
6	Secure Mutual Authentication and Key-Exchange Protocol between PUF-Embedded IoT Endpoints. , 2021, , .		19
7	Fingerprinting Deep Neural Networks - a DeepFool Approach. , 2021, , .		12
8	Two Sides of the Same Coin: Boons and Banes of Machine Learning in Hardware Security. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 228-251.	3.6	4
9	An Overview of Hardware Security and Trust: Threats, Countermeasures, and Design Tools. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1010-1038.	2.7	56
10	A New Lightweight In Situ Adversarial Sample Detector for Edge Deep Neural Network. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 252-266.	3.6	4
11	Hardware Security in Emerging Technologies: Vulnerabilities, Attacks, and Solutions. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 223-227.	3.6	2
12	A Modeling Attack Resistant Deception Technique for Securing Lightweight-PUF-Based Authentication. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1183-1196.	2.7	34
13	Halide perovskite memristors as flexible and reconfigurable physical unclonable functions. Nature Communications, 2021, 12, 3681.	12.8	107
14	The ASHES 2019 special issue at JCEN. Journal of Cryptographic Engineering, 2021, 11, 199-200.	1.8	0
15	A large-scale comprehensive evaluation of single-slice ring oscillator and PicoPUF bit cells on 28-nm Xilinx FPGAs. Journal of Cryptographic Engineering, 2021, 11, 227-238.	1.8	14
16	A Forward Error Compensation Approach for Fault Resilient Deep Neural Network Accelerator Design. , 2021, , .		1
17	Identification of FSM State Registers by Analytics of Scan-Dump Data. IEEE Transactions on Information Forensics and Security, 2021, 16, 5138-5153.	6.9	0
18	An Ultra-Low Power 3-T Chaotic Map based True Random Number Generator. , 2021, , .		1

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19	A PUF-Based Data-Device Hash for Tampered Image Detection and Source Camera Identification. IEEE Transactions on Information Forensics and Security, 2020, 15, 620-634.	6.9	34
20	Fired Neuron Rate Based Decision Tree for Detection of Adversarial Examples in DNNs. , 2020, , .		3
21	Imperceptible Misclassification Attack on Deep Learning Accelerator by Glitch Injection. , 2020, , .		22
22	Reducing Temperature Induced Unreliability in Sub-Threshold Strong PUFs through Circuit Modeling. , 2020, , .		0
23	A New Polarization Image Demosaicking Algorithm by Exploiting Inter-Channel Correlations With Guided Filtering. IEEE Transactions on Image Processing, 2020, 29, 7076-7089.	9.8	26
24	Ed-PUF: Event-Driven Physical Unclonable Function for Camera Authentication in Reactive Monitoring System. IEEE Transactions on Information Forensics and Security, 2020, 15, 2824-2839.	6.9	14
25	A 1036-F²/Bit High Reliability Temperature Compensated Cross-Coupled Comparator-Based PUF. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1449-1460.	3.1	17
26	Analysis of Circuit Aging on Accuracy Degradation of Deep Neural Network Accelerator. , 2019, , .		2
27	An Energy-Efficient Current-Starved Inverter Based Strong Physical Unclonable Function With Enhanced Temperature Stability. IEEE Access, 2019, 7, 105287-105297.	4.2	18
28	An In-Pixel Gain Amplifier Based Event-Driven Physical Unclonable Function for CMOS Dynamic Vision Sensors. , 2019, , .		3
29	ASHES 2019. , 2019, , .		0
30	A Reliable Physical Unclonable Function Based on Differential Charging Capacitors. , 2019, , .		0
31	UDhashing: Physical Unclonable Function-Based User-Device Hash for Endpoint Authentication. IEEE Transactions on Industrial Electronics, 2019, 66, 9559-9570.	7.9	21
32	Editorial TVLSI Positioningâ€"Continuing and Accelerating an Upward Trajectory. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 253-280.	3.1	6
33	High-Speed True Random Number Generator Based on Differential Current Starved Ring Oscillators with Improved Thermal Stability. , 2019, , .		8
34	Emerging Attacks and Solutions for Secure Hardware in the Internet of Things. IEEE Transactions on Dependable and Secure Computing, 2019, 16, 373-375.	5.4	2
35	Area- and Power-Efficient Nearly-Linear Phase Response IIR Filter by Iterative Convex Optimization. IEEE Access, 2019, 7, 22952-22965.	4.2	5
36	Identification of State Registers of FSM Through Full Scan by Data Analytics. , 2019, , .		2

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37	Vulnerability Analysis on Noise-Injection Based Hardware Attack on Deep Neural Networks. , 2019, , .		3
38	A Modeling Attack Resistant Deception Technique for Securing PUF based Authentication. , 2019, , .		18
39	Detecting Adversarial Examples for Deep Neural Networks via Layer Directed Discriminative Noise Injection. , 2019, , .		5
40	A Large Scale Comprehensive Evaluation of Single-Slice Ring Oscillator and PicoPUF Bit Cells on 28nm Xilinx FPGAs. , 2019, , .		1
41	Reliable and Modeling Attack Resistant Authentication of Arbiter PUF in FPGA Implementation With Trinary Quadruple Response. IEEE Transactions on Information Forensics and Security, 2019, 14, 1109-1123.	6.9	75
42	Facial biohashing based user-device physical unclonable function for bring your own device security. , 2018, , .		12
43	Current Mirror Array: A Novel Circuit Topology for Combining Physical Unclonable Function and Machine Learning. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1314-1326.	5.4	36
44	New Hardware and Power Efficient Sporadic Logarithmic Shifters for DSP Applications. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 896-900.	2.7	6
45	Securing IoT Monitoring Device using PUF and Physical Layer Authentication. , 2018, , .		13
46	A New Accurate and Fast Homography Computation Algorithm for Sports and Traffic Video Analysis. IEEE Transactions on Circuits and Systems for Video Technology, 2018, 28, 2993-3006.	8.3	10
47	A Current Comparator Based Physical Unclonable Function with High Reliability and Energy Efficiency. , 2018, , .		4
48	A Low-power Reliability Enhanced Arbiter Physical Unclonable Function Based on Current Starved Multiplexers. , 2018, , .		3
49	ASHES 2018- Workshop on Attacks and Solutions in Hardware Security. , 2018, , .		1
50	Towards Ideal Lattice-Based Cryptography on ASIC: A Custom Implementation of Number Theoretic Transform. , 2018, , .		2
51	A Fully Digital Physical Unclonable Function Based Temperature Sensor for Secure Remote Sensing. , 2018, , .		3
52	Active IC Metering of Digital Signal Processing Subsystem with Two-Tier Activation for Secure Split Test. , 2018, , .		0
53	A Low Power Diode-Clamped Inverter-Based Strong Physical Unclonable Function for Robust and Lightweight Authentication. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3864-3873.	5.4	44
54	A Sub-pico Joules Per Bit Robust Physical Unclonable Function Based on Subthreshold Voltage References. , 2018, , .		6

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55	Tap Delay-and-Accumulate Cost Aware Coefficient Synthesis Algorithm for the Design of Area-Power Efficient FIR Filters. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 712-722.	5.4	13
56	Cyclic resistance change in perpendicularly magnetized Co/Ni nanowire induced by alternating current pulse injection. Current Applied Physics, 2017, 17, 98-102.	2.4	2
57	FPGA implementation of modeling attack resistant arbiter PUF with enhanced reliability. , 2017, , .		10
58	Asymmetrical domain wall propagation in bifurcated PMA wire structure due to the Dzyaloshinskii-Moriya interaction. Applied Physics Letters, 2017, 110, 232402.	3.3	4
59	Double-Base Number System and Its Application in FIR Filter Design. , 2017, , 277-310.		1
60	Design and Evaluation of Booth-Encoded Multipliers in Redundant Binary Representation. , 2017, , 113-147.		4
61	A Retrospective and a Look Forward: Fifteen Years of Physical Unclonable Function Advancement. IEEE Circuits and Systems Magazine, 2017, 17, 32-62.	2.3	125
62	A Scaling-Assisted Signed Integer Comparator for the Balanced Five-Moduli Set RNS ${2^{n}-1, 2^{n}, 2^{n}+ 1, 2^{n+1}- 1, 2^{n-1}- 1}$. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 3521-3533.	3.1	4
63	ACRO-PUF: A Low-power, Reliable and Aging-Resilient Current Starved Inverter-Based Ring Oscillator Physical Unclonable Function. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 3138-3149.	5.4	60
64	Low-cost fortification of arbiter PUF against modeling attack. , 2017, , .		12
65	New Algorithm for Signed Integer Comparison in ${2^{n+k},2^{n}-1,2^{n}+1,2^{npm 1}-1}$ and Its Efficient Hardware Implementation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 1481-1493.	5.4	11
66	Static and Dynamic Obfuscations of Scan Data Against Scan-Based Side-Channel Attacks. IEEE Transactions on Information Forensics and Security, 2017, 12, 363-376.	6.9	55
67	A New Cost-Aware Sensitivity-Driven Algorithm for the Design of FIR Filters. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 1588-1598.	5.4	15
68	20 Years of research on intellectual property protection. , 2017, , .		9
69	ASHES 2017. , 2017, , .		0
70	Current mirror array: A novel lightweight strong PUF topology with enhanced reliability. , 2017, , .		7
71	A novel scheme for information hiding at physical layer of wireless communications. , 2017, , .		1
72	An energy-efficient true random number generator based on current starved ring oscillators. , 2017, , .		12

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73	A new write-contention based dual-port SRAM PUF with multiple response bits per cell. , 2017, , .		8
74	A new watermarking scheme on scan chain ordering for hard IP protection. , 2017, , .		6
75	Sizing of SRAM Cell with Voltage Biasing Techniques for Reliability Enhancement of Memory and PUF Functions. Journal of Low Power Electronics and Applications, 2016, 6, 16.	2.0	8
76	A new scheme for secret-hiding in DSP circuits. , 2016, , .		0
77	Low-power, lightweight and reliability-enhanced current starved inverter based RO PUFs. , 2016, , .		5
78	Accelerating residue-to-binary conversion of very high cardinality moduli set for fully homomorphic encryption. , 2016, , .		0
79	Using image sensor PUF as root of trust for birthmarking of perceptual image hash. , 2016, , .		9
80	A new event-driven Dynamic Vision Sensor based Physical Unclonable Function for camera authentication in reactive monitoring system. , 2016, , .		12
81	Multi-valued Arbiters for quality enhancement of PUF responses on FPGA implementation. , 2016, , .		27
82	A VLSI-efficient signed magnitude comparator for { 2n-1, 2n, 2n +2n+1-1} RNS. , 2016, , .		2
83	A low-voltage, low power STDP synapse implementation using domain-wall magnets for spiking neural networks. , 2016, , .		6
84	DW-AES: A Domain-Wall Nanowire-Based AES for High Throughput and Energy-Efficient Data Encryption in Non-Volatile Memory. IEEE Transactions on Information Forensics and Security, 2016, 11, 2426-2440.	6.9	40
85	A non-iterative multiple residue digit error detection and correction algorithm in RRNS. IEEE Transactions on Computers, 2016, 65, 396-408.	3.4	28
86	A New Fast and Area-Efficient Adder-Based Sign Detector for RNS {<inline-formula> <tex-math notation="LaTeX">$2^{n}-1, 2^{n}, 2^{n}+1$ </tex-math> </inline-formula>}. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2608-2612.	3.1	23
87	A New Paradigm of Common Subexpression Elimination by Unification of Addition and Subtraction. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1605-1617.	2.7	21
88	Hypergraph Based Minimum Arborescence Algorithm for the Optimization and Reoptimization of Multiple Constant Multiplications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 233-244.	5.4	16
89	Erratum to â€œEfficient VLSI Implementation of Scaling of Signed Integer in RNS {}â€•[Oct 13 1936-1940]. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1612-1612.	3.1	0
90	Secure Licensing of IP Cores on SRAM-Based FPGAs. , 2016, , 391-418.		1

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91	Hardware IP Watermarking and Fingerprinting. , 2016, , 329-368.		17
92	Design and Implementation of High-Quality Physical Unclonable Functions for Hardware-Oriented Cryptography. , 2016, , 39-81.		14
93	A high-speed and area-efficient sign detector for three moduli set RNS {2n, 2n-1, 2n+1}. , 2015, , .		1
94	Low field domain wall dynamics in artificial spin-ice basis structure. Journal of Applied Physics, 2015, 118, .	2.5	3
95	Design of Optimal Scan Tree Based on Compact Test Patterns for Test Time Reduction. IEEE Transactions on Computers, 2015, 64, 3417-3429.	3.4	11
96	A Low-Power Hybrid RO PUF With Improved Thermal Stability for Lightweight Applications. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1143-1147.	2.7	96
97	Highly Reliable Spin-Transfer Torque Magnetic RAM-Based Physical Unclonable Function With Multi-Response-Bits Per Cell. IEEE Transactions on Information Forensics and Security, 2015, 10, 1630-1642.	6.9	27
98	Optimizating Emerging Nonvolatile Memories for Dual-Mode Applications: Data Storage and Key Generator. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1176-1187.	2.7	30
99	Efficient structural adder pipelining in transposed form FIR filters. , 2015, , .		8
100	CMOS Image Sensor Based Physical Unclonable Function for Coherent Sensor-Level Authentication. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 2629-2640.	5.4	65
101	A new unified modular adder/subtractor for arbitrary moduli. , 2015, , .		1
102	Statistical analysis and design of 6T SRAM cell for physical unclonable function with dual application modes. , 2015, , .		8
103	Public key protocol for usage-based licensing of FPGA IP cores. , 2015, , .		4
104	Base Transformation With Injective Residue Mapping for Dynamic Range Reduction in RNS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 2248-2259.	5.4	5
105	Residue Number Systems: A New Paradigm to Datapath Optimization for Low-Power and High-Performance Digital Signal Processing Applications. IEEE Circuits and Systems Magazine, 2015, 15, 26-44.	2.3	114
106	Novel Design Algorithm for Low Complexity Programmable FIR Filters Based on Extended Double Base Number System. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 224-233.	5.4	36
107	New algorithm for signed integer comparison in four-moduli superset {2ⁿ, 2ⁿ −1, 2ⁿ +1, 2ⁿ⁺¹−1}. , 2014, , .		6
108	A Pragmatic Per-Device Licensing Scheme for Hardware IP Cores on SRAM-Based FPGAs. IEEE Transactions on Information Forensics and Security, 2014, 9, 1893-1905.	6.9	21

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109	A Cluster-Based Distributed Active Current Sensing Circuit for Hardware Trojan Detection. IEEE Transactions on Information Forensics and Security, 2014, 9, 2220-2231.	6.9	41
110	A modular design of elliptic-curve point multiplication for resource constrained devices. , 2014, , .		1
111	Leakage-resilient memory-based physical unclonable function using phase change material. , 2014, , .		7
112	Obfuscation and watermarking of FPGA designs based on constant value generators. , 2014, , .		3
113	Hardware Trojan detection with linear regression based gate-level characterization. , 2014, , .		7
114	Highly reliable memory-based Physical Unclonable Function using Spin-Transfer Torque MRAM. , 2014, , .		49
115	Feasibility study of emerging non-volatilememory based physical unclonable functions. , 2014, , .		13
116	Area-efficient and fast sign detection for four-moduli set RNS {2ⁿ −1,2ⁿ, 2ⁿ +1,22ⁿ +1}. , 2014, , .		0
117	Design of programmable FIR filters using Canonical Double Based Number Representation. , 2014, , .		4
118	CMOS image sensor based physical unclonable function for smart phone security applications. , 2014, , .		7
119	A 0.7V low-power fully programmable Gaussian function generator for brain-inspired Gaussian correlation associative memory. Neurocomputing, 2014, 138, 69-77.	5.9	10
120	A Blind Dynamic Fingerprinting Technique for Sequential Circuit Intellectual Property Protection. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 76-89.	2.7	29
121	Exploiting Process Variations and Programming Sensitivity of Phase Change Memory for Reconfigurable Physical Unclonable Functions. IEEE Transactions on Information Forensics and Security, 2014, 9, 921-932.	6.9	80
122	A new algorithm for single residue digit error correction in Redundant Residue Number System. , 2014, , .		22
123	A signed integer programmable power-of-two scaler for {2ⁿ-1, 2ⁿ, 2ⁿ+1} RNS. , 2013, , .		0
124	A New Approach to the Design of Efficient Residue Generators for Arbitrary Moduli. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 2366-2374.	5.4	23
125	Thermal simulator of 3D-IC with modeling of anisotropic TSV conductance and microchannel entrance effects. , 2013, , .		7
126	Efficient VLSI Implementation of $2^{{n}}$ Scaling of Signed Integer in RNS ${{2^{n}-1, 2^{n},2^{n}+1}}$. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1936-1940.	3.1	21

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127	An efficient channel clustering and flow rate allocation algorithm for non-uniform microfluidic cooling of 3D integrated circuits. The Integration VLSI Journal, 2013, 46, 57-68.	2.1	12
128	Radix-4 and Radix-8 Booth Encoded Multi-Modulus Multipliers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 2940-2952.	5.4	31
129	Cluster-based distributed active current timer for hardware Trojan detection. , 2013, , .		11
130	PCKGen: A Phase Change Memory based cryptographic key generator. , 2013, , .		34
131	Microchannel splitting and scaling for thermal balancing of liquid-cooled 3DIC. , 2013, , .		2
132	A post-processing scan-chain watermarking scheme for VLSI intellectual property protection. , 2012, , .		7
133	State encoding watermarking for field authentication of sequential circuit intellectual property. , 2012, , .		12
134	Pipelined adder graph optimization for high speed multiple constant multiplication. , 2012, , .		38
135	A unified {2ⁿ−1, 2ⁿ, 2ⁿ+1} RNS scaler with dual scaling constants. , 2012, , .		0
136	Guest Editorial Special Section on the 2011 IEEE Custom Integrated Circuits Conference (CICC 2011). IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 1601-1603.	5.4	0
137	A fast and compact circuit for integer square root computation based on Mitchell logarithmic method. , 2012, , .		3
138	An Area and Energy Efficient Inner-Product Processor for Serial-Link Bus Architecture. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 2945-2955.	5.4	3
139	Dynamical Systems Guided Design and Analysis of Silicon Oscillators for Central Pattern Generators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 3046-3059.	5.4	8
140	A VLSI Efficient Programmable Power-of-Two Scaler for ${2^{n}-1,2^{n},2^{n}+1}$ RNS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 2911-2919.	5.4	16
141	Area-Power Efficient Modulo $2^{n}-1$ and Modulo $2^{n}+1$ Multipliers for ${2^{n}-1, 2^{n}, 2^{n}+1}$ Based RNS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 2263-2274.	5.4	42
142	A compact 16-bit dual-slope integrating circuit for direct analog-to-residue conversion. , 2012, , .		1
143	Radix-8 Booth Encoded Modulo $2 ^{n} -1$ Multipliers With Adaptive Delay for High Dynamic Range Residue Number System. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 982-993.	5.4	34
144	Low error bit width reduction for structural adders of FIR filters. , 2011, , .		5

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145	Simple, Fast, and Exact RNS Scaler for the Three-Moduli Set ${2^{n} - 1, 2^{n}, 2^{n} + 1}$. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 2686-2697.	5.4	35
146	Bit-parallel Multiple Constant Multiplication using Look-Up Tables on FPGA. , 2011, , .		14
147	A High Bit Rate Serial-Serial Multiplier With On-the-Fly Accumulation by Asynchronous Counters. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1733-1745.	3.1	16
148	A Robust FSM Watermarking Scheme for IP Protection of Sequential Circuit Design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 678-690.	2.7	81
149	Bayesian Separation With Sparsity Promotion in Perceptual Wavelet Domain for Speech Enhancement and Hybrid Speech Recognition. IEEE Transactions on Systems, Man and Cybernetics, Part A: Systems and Humans, 2011, 41, 284-293.	2.9	22
150	Sign-Extension Avoidance and Word-Length Optimization by Positive-Offset Representation for FIR Filter Design. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 916-920.	3.0	5
151	A hybrid watermarking scheme for sequential functions. , 2011, , .		19
152	A simple radix-4 Booth encoded modulo 2ⁿ+1 multiplier. , 2011, , .		3
153	A new RNS scaler for {2ⁿ − 1, 2ⁿ, 2ⁿ + 1}. , 2011, , .		0
154	Dynamical systems: A tool for analysis and design of silicon half center oscillators. , 2011, , .		1
155	Fast and VLSI efficient binary-to-CSD encoder using bypass signal. Electronics Letters, 2011, 47, 18.	1.0	14
156	Cyber-Physical Thermal Management of 3D Multi-Core Cache-Processor System with Microfluidic Cooling. Journal of Low Power Electronics, 2011, 7, 110-121.	0.6	30
157	Fast hard multiple generators for radix-8 Booth encoded modulo 2ⁿ−1 and modulo 2ⁿ+1 multipliers. , 2010, , .		4
158	Reconfigurable multiple constant multiplication using minimum adder depth. , 2010, , .		9
159	A novel counter-based low complexity inner-product architecture for high speed inputs. , 2010, , .		4
160	Real-time thermal management of 3D multi-core system with fine-grained cooling control. , 2010, , .		1
161	A very low power 0.7 V subthreshold fully programmable Gaussian function generator. , 2010, , .		6
162	A Low Error and High Performance Multiplexer-Based Truncated Multiplier. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1767-1771.	3.1	37

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163	On â€œA New Common Subexpression Elimination Algorithm for Realizing Low-Complexity Higher Order Digital Filtersâ€• IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 844-848.	2.7	20
164	Synthesis-for-Testability Watermarking for Field Authentication of VLSI Intellectual Property. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 1618-1630.	5.4	32
165	Low Complexity Digit Serial Systolic Montgomery Multipliers for Special Class of ${m GF}(2^{m})$. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 847-852.	3.1	42
166	Minimal Logic Depth adder tree optimization for Multiple Constant Multiplication. , 2010, , .		29
167	Performance analysis of different special moduli sets for RNS-based inner product step processor. , 2010, , .		4
168	Reduction of partial product matrix for high-speed single or multiple constant multiplication. , 2010, , .		0
169	New power index model for switching power analysis from adder graph of FIR filter. , 2009, , .		11
170	Time-multiplexed data flow graph for the design of configurable multiplier block. , 2009, , .		2
171	A compact current mode neuron circuit with Gaussian taper learning capability. , 2009, , .		11
172	Optimization of structural adders in fixed coefficient transposed direct form FIR filters. , 2009, , .		15
173	Fixed and variable multi-modulus squarer architectures for triple moduli base of RNS. , 2009, , .		12
174	A New Redundant Binary Booth Encoding for Fast 2^{n}-Bit Multiplier Design. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 1192-1201.	5.4	32
175	An improved publicly detectable watermarking scheme based on scan chain ordering. , 2009, , .		14
176	High-Level Synthesis Algorithm for the Design of Reconfigurable Constant Multiplier. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 1844-1856.	2.7	39
177	Information Theoretic Approach to Complexity Reduction of FIR Filter Design. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 2310-2321.	5.4	39
178	Contention Resolutionâ€”A New Approach to Versatile Subexpressions Sharing in Multiple Constant Multiplications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 559-571.	5.4	17
179	IP Watermarking Using Incremental Technology Mapping at Logic Synthesis Level. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1565-1570.	2.7	41
180	A Power-Delay Efficient Hybrid Carry-Lookahead/Carry-Select Based Redundant Binary to Two's Complement Converter. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 336-346.	5.4	31

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181	High-speed and low-power serial accumulator for serial/parallel multiplier. , 2008, , .		6
182	Programmable LSB-first and MSB-first modular multipliers for ECC in GF(2^m). , 2008, , .		0
183	Intellectual property authentication by watermarking scan chain in design-for-testability flow. , 2008, , .		2
184	A low complexity modulo 2ⁿ+1 squarer design. , 2008, , .		3
185	Contention Resolution-A New Approach to Versatile Subexpressions Sharing in Multiple Constant Multiplications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, , 1-1.	5.4	0
186	Watermarking for IP Protection through Template Substitution at Logic Synthesis Level. , 2007, , .		11
187	A Generalized Timeâ€“Frequency Subtraction Method for Robust Speech Enhancement Based on Wavelet Filter Banks Modeling of Human Auditory System. IEEE Transactions on Systems, Man, and Cybernetics, 2007, 37, 877-889.	5.0	38
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