Chip-Hong Chang

List of Publications by Year
in descending order

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288 papers	4,803 citations	126907 33 h-index	149698 56 g-index
292 all docs	292 docs citations	292 times ranked	2185 citing authors

#	Article	IF	Citations
1	Ultra Low-Voltage Low-Power CMOS 4-2 and 5-2 Compressors for Fast Arithmetic Circuits. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2004, 51, 1985-1997.	0.1	296
2	A review of 0.18-/spl mu/m full adder performances for tree structured arithmetic circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2005, 13, 686-695.	3.1	294
3	A Retrospective and a Look Forward: Fifteen Years of Physical Unclonable Function Advancement. IEEE Circuits and Systems Magazine, 2017, 17, 32-62.	2.3	125
4	Residue Number Systems: A New Paradigm to Datapath Optimization for Low-Power and High-Performance Digital Signal Processing Applications. IEEE Circuits and Systems Magazine, 2015, 15, 26-44.	2.3	114
5	Halide perovskite memristors as flexible and reconfigurable physical unclonable functions. Nature Communications, 2021, 12, 3681.	12.8	107
6	An efficient reverse converter for the 4-moduli set [2/sup n/ - 1, 2/sup n, 2/sup n + 1, 2/sup 2n/ + 1] based on the new chinese remainder theorem. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2003, 50, 1296-1303.	0.1	98
7	A Low-Power Hybrid RO PUF With Improved Thermal Stability for Lightweight Applications. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1143-1147.	2.7	96
8	New Adaptive Color Quantization Method Based on Self-Organizing Maps. IEEE Transactions on Neural Networks, 2005, 16, 237-249.	4.2	89
9	A Robust FSM Watermarking Scheme for IP Protection of Sequential Circuit Design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 678-690.	2.7	81
10	Exploiting Process Variations and Programming Sensitivity of Phase Change Memory for Reconfigurable Physical Unclonable Functions. IEEE Transactions on Information Forensics and Security, 2014, 9, 921-932.	6.9	80
11	A Residue-to-Binary Converter for a New Five-Moduli Set. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2007, 54, 1041-1049.	0.1	76
12	Reliable and Modeling Attack Resistant Authentication of Arbiter PUF in FPGA Implementation With Trinary Quadruple Response. IEEE Transactions on Information Forensics and Security, 2019, 14, 1109-1123.	6.9	75
13	Design of Low-Complexity FIR Filters Based on Signed-Powers-of-Two Coefficients With Reusable Common Subexpressions. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1898-1907.	2.7	68
14	CMOS Image Sensor Based Physical Unclonable Function for Coherent Sensor-Level Authentication. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 2629-2640.	5.4	65
15	Efficient reverse converters for four-moduli sets { 2nâˆ'1, 2n, 2n+1, 2n+1âˆ'1} and {2nâˆ'1, 2n, 2n+1, 2nâˆ'1âˆ'1}. IEE Proceedings: Computers and Digital Techniques, 2005, 152, 687.	1.6	63
16	ACRO-PUF: A Low-power, Reliable and Aging-Resilient Current Starved Inverter-Based Ring Oscillator Physical Unclonable Function. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 3138-3149.	5.4	60
17	An Overview of Hardware Security and Trust: Threats, Countermeasures, and Design Tools. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1010-1038.	2.7	56
18	Static and Dynamic Obfuscations of Scan Data Against Scan-Based Side-Channel Attacks. IEEE Transactions on Information Forensics and Security, 2017, 12, 363-376.	6.9	55

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19	An Area Efficient 64-bit Square Root Carry-select Adder for Low Power Applications. , 0, , .		51
20	Highly reliable memory-based Physical Unclonable Function using Spin-Transfer Torque MRAM. , 2014, , .		49
21	Contention resolution algorithm for common subexpression elimination in digital filter design. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2005, 52, 695-700.	2.2	47
22	Fuzzy-ART based adaptive digital watermarking scheme. IEEE Transactions on Circuits and Systems for Video Technology, 2005, 15, 65-81.	8.3	45
23	A Low Power Diode-Clamped Inverter-Based Strong Physical Unclonable Function for Robust and Lightweight Authentication. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3864-3873.	5.4	44
24	Low Complexity Digit Serial Systolic Montgomery Multipliers for Special Class of ${m GF}(2^{m})$. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 847-852.	3.1	42
25	Area-Power Efficient Modulo $2^{n}-1$ and Modulo $2^{n}+1$ Multipliers for ${2^{n}-1, 2^{n}, 2^{n}+1}$ Based RNS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 2263-2274.	5.4	42
26	IP Watermarking Using Incremental Technology Mapping at Logic Synthesis Level. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1565-1570.	2.7	41
27	A Cluster-Based Distributed Active Current Sensing Circuit for Hardware Trojan Detection. IEEE Transactions on Information Forensics and Security, 2014, 9, 2220-2231.	6.9	41
28	A novel hybrid pass logic with static CMOS output drive full-adder cell. , 0, , .		40
29	DW-AES: A Domain-Wall Nanowire-Based AES for High Throughput and Energy-Efficient Data Encryption in Non-Volatile Memory. IEEE Transactions on Information Forensics and Security, 2016, 11, 2426-2440.	6.9	40
30	Information Theoretic Approach to Complexity Reduction of FIR Filter Design. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 2310-2321.	5.4	39
31	High-Level Synthesis Algorithm for the Design of Reconfigurable Constant Multiplier. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 1844-1856.	2.7	39
32	A Generalized Timeâ€“Frequency Subtraction Method for Robust Speech Enhancement Based on Wavelet Filter Banks Modeling of Human Auditory System. IEEE Transactions on Systems, Man, and Cybernetics, 2007, 37, 877-889.	5.0	38
33	Pipelined adder graph optimization for high speed multiple constant multiplication. , 2012, , .		38
34	A Low Error and High Performance Multiplexer-Based Truncated Multiplier. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1767-1771.	3.1	37
35	Novel Design Algorithm for Low Complexity Programmable FIR Filters Based on Extended Double Base Number System. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 224-233.	5.4	36
36	Current Mirror Array: A Novel Circuit Topology for Combining Physical Unclonable Function and Machine Learning. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1314-1326.	5.4	36

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37	Simple, Fast, and Exact RNS Scaler for the Three-Moduli Set ${2^{n} - 1, 2^{n}, 2^{n} + 1}$. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 2686-2697.	5.4	35
38	Radix-8 Booth Encoded Modulo $2 ^{n} -1$ Multipliers With Adaptive Delay for High Dynamic Range Residue Number System. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 982-993.	5.4	34
39	PCKGen: A Phase Change Memory based cryptographic key generator. , 2013, , .		34
40	A PUF-Based Data-Device Hash for Tampered Image Detection and Source Camera Identification. IEEE Transactions on Information Forensics and Security, 2020, 15, 620-634.	6.9	34
41	A Modeling Attack Resistant Deception Technique for Securing Lightweight-PUF-Based Authentication. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1183-1196.	2.7	34
42	A New Redundant Binary Booth Encoding for Fast 2^{n}-Bit Multiplier Design. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 1192-1201.	5.4	32
43	Synthesis-for-Testability Watermarking for Field Authentication of VLSI Intellectual Property. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 1618-1630.	5.4	32
44	A Power-Delay Efficient Hybrid Carry-Lookahead/Carry-Select Based Redundant Binary to Two's Complement Converter. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 336-346.	5.4	31
45	Radix-4 and Radix-8 Booth Encoded Multi-Modulus Multipliers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 2940-2952.	5.4	31
46	Optimizating Emerging Nonvolatile Memories for Dual-Mode Applications: Data Storage and Key Generator. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1176-1187.	2.7	30
47	Cyber-Physical Thermal Management of 3D Multi-Core Cache-Processor System with Microfluidic Cooling. Journal of Low Power Electronics, 2011, 7, 110-121.	0.6	30
48	Minimal Logic Depth adder tree optimization for Multiple Constant Multiplication. , 2010, , .		29
49	A Blind Dynamic Fingerprinting Technique for Sequential Circuit Intellectual Property Protection. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 76-89.	2.7	29
50	A non-iterative multiple residue digit error detection and correction algorithm in RRNS. IEEE Transactions on Computers, 2016, 65, 396-408.	3.4	28
51	Highly Reliable Spin-Transfer Torque Magnetic RAM-Based Physical Unclonable Function With Multi-Response-Bits Per Cell. IEEE Transactions on Information Forensics and Security, 2015, 10, 1630-1642.	6.9	27
52	Multi-valued Arbiters for quality enhancement of PUF responses on FPGA implementation. , 2016, , .		27
53	A New Energy-Efficient and High Throughput Two-Phase Multi-Bit per Cycle Ring Oscillator-Based True Random Number Generator. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 272-283.	5.4	27
54	A New Polarization Image Demosaicking Algorithm by Exploiting Inter-Channel Correlations With Guided Filtering. IEEE Transactions on Image Processing, 2020, 29, 7076-7089.	9.8	26

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55	Forward and inverse transformations between Haar spectra and ordered binary decision diagrams of Boolean functions. IEEE Transactions on Computers, 1997, 46, 1272-1279.	3.4	25
56	A New PUF Based Lock and Key Solution for Secure In-Field Testing of Cryptographic Chips. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 1095-1105.	4.6	25
57	Self-Organizing Topological Tree for Online Vector Quantization and Data Clustering. IEEE Transactions on Systems, Man, and Cybernetics, 2005, 35, 515-526.	5.0	24
58	A New Approach to the Design of Efficient Residue Generators for Arbitrary Moduli. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 2366-2374.	5.4	23
59	A New Fast and Area-Efficient Adder-Based Sign Detector for RNS {<inline-formula> <tex-math notation="LaTeX">$2^{n}-1, 2^{n}, 2^{n}+1$ </tex-math> </inline-formula>}. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2608-2612.	3.1	23
60	Bayesian Separation With Sparsity Promotion in Perceptual Wavelet Domain for Speech Enhancement and Hybrid Speech Recognition. IEEE Transactions on Systems, Man and Cybernetics, Part A: Systems and Humans, 2011, 41, 284-293.	2.9	22
61	A new algorithm for single residue digit error correction in Redundant Residue Number System. , 2014, , .		22
62	Imperceptible Misclassification Attack on Deep Learning Accelerator by Glitch Injection. , 2020, , .		22
63	Efficient algorithms for the calculation of arithmetic spectrum from OBDD and synthesis of OBDD from arithmetic spectrum for incompletely specified Boolean functions. , 0, , .		21
64	A Reconfigurable Multi-Modulus Modulo Multiplier. , 2006, , .		21
65	Efficient VLSI Implementation of $2^{{n}}$ Scaling of Signed Integer in RNS ${{2^{n}-1, 2^{n},2^{n}+1}}$. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1936-1940.	3.1	21
66	A Pragmatic Per-Device Licensing Scheme for Hardware IP Cores on SRAM-Based FPGAs. IEEE Transactions on Information Forensics and Security, 2014, 9, 1893-1905.	6.9	21
67	A New Paradigm of Common Subexpression Elimination by Unification of Addition and Subtraction. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1605-1617.	2.7	21
68	UDhashing: Physical Unclonable Function-Based User-Device Hash for Endpoint Authentication. IEEE Transactions on Industrial Electronics, 2019, 66, 9559-9570.	7.9	21
69	On â€œA New Common Subexpression Elimination Algorithm for Realizing Low-Complexity Higher Order Digital Filtersâ€• IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 844-848.	2.7	20
70	A hybrid watermarking scheme for sequential functions. , 2011, , .		19
71	Secure Mutual Authentication and Key-Exchange Protocol between PUF-Embedded IoT Endpoints. , 2021, , .		19
72	A Comparison of Pipelined RAG-n and DA FPGA-based Multiplierless Filters. , 2006, , .		18

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73	An Energy-Efficient Current-Starved Inverter Based Strong Physical Unclonable Function With Enhanced Temperature Stability. IEEE Access, 2019, 7, 105287-105297.	4.2	18
74	A Modeling Attack Resistant Deception Technique for Securing PUF based Authentication. , 2019, , .		18
75	Contention Resolutionâ€"A New Approach to Versatile Subexpressions Sharing in Multiple Constant Multiplications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 559-571.	5.4	17
76	A 1036-F²/Bit High Reliability Temperature Compensated Cross-Coupled Comparator-Based PUF. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1449-1460.	3.1	17
77	Hardware IP Watermarking and Fingerprinting. , 2016, , 329-368.		17
78	A High Bit Rate Serial-Serial Multiplier With On-the-Fly Accumulation by Asynchronous Counters. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1733-1745.	3.1	16
79	A VLSI Efficient Programmable Power-of-Two Scaler for ${2^{n}-1,2^{n},2^{n}+1}$ RNS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 2911-2919.	5.4	16
80	Hypergraph Based Minimum Arborescence Algorithm for the Optimization and Reoptimization of Multiple Constant Multiplications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 233-244.	5.4	16
81	Optimization of structural adders in fixed coefficient transposed direct form FIR filters. , 2009, , .		15
82	A New Cost-Aware Sensitivity-Driven Algorithm for the Design of FIR Filters. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 1588-1598.	5.4	15
83	An exact minimizer of fixed polarity Reed-Muller expansions. International Journal of Electronics, 1995, 79, 389-409.	1.4	14
84	AN ULTRA LOW-POWER CURRENT-MODE SENSE AMPLIFIER FOR SRAM APPLICATIONS. Journal of Circuits, Systems and Computers, 2005, 14, 939-951.	1.5	14
85	An improved publicly detectable watermarking scheme based on scan chain ordering. , 2009, , .		14
86	Bit-parallel Multiple Constant Multiplication using Look-Up Tables on FPGA. , 2011, , .		14
87	Fast and VLSI efficient binary-to-CSD encoder using bypass signal. Electronics Letters, 2011, 47, 18.	1.0	14
88	Ed-PUF: Event-Driven Physical Unclonable Function for Camera Authentication in Reactive Monitoring System. IEEE Transactions on Information Forensics and Security, 2020, 15, 2824-2839.	6.9	14
89	Design and Implementation of High-Quality Physical Unclonable Functions for Hardware-Oriented Cryptography. , 2016, , 39-81.		14
90	A large-scale comprehensive evaluation of single-slice ring oscillator and PicoPUF bit cells on 28-nm Xilinx FPGAs. Journal of Cryptographic Engineering, 2021, 11, 227-238.	1.8	14

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91	Properties and methods of calculating generalised arithmetic and adding transforms. IET Circuits, Devices and Systems, 1997, 144, 249.	0.6	13
92	Feasibility study of emerging non-volatilememory based physical unclonable functions. , 2014, , .		13
93	Securing IoT Monitoring Device using PUF and Physical Layer Authentication. , 2018, , .		13
94	Tap Delay-and-Accumulate Cost Aware Coefficient Synthesis Algorithm for the Design of Area-Power Efficient FIR Filters. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 712-722.	5.4	13
95	A novel paired Haar based transform: algorithms and interpretations in Boolean domain. , 0, , .		12
96	Generation of multi-polarity arithmetic transform from reduced representation of Boolean functions. , 0, , .		12
97	Paired Haar spectra computation through operations on disjoint cubes. IET Circuits, Devices and Systems, 1999, 146, 117.	0.6	12
98	Ultra low voltage, low power 4-2 compressor for high speed multiplications. , 0, , .		12
99	Low-power differential coefficients-based FIR filters using hardware-optimised multipliers. IET Circuits, Devices and Systems, 2007, 1, 13.	1.4	12
100	Fixed and variable multi-modulus squarer architectures for triple moduli base of RNS. , 2009, , .		12
101	State encoding watermarking for field authentication of sequential circuit intellectual property. , 2012, , .		12
102	An efficient channel clustering and flow rate allocation algorithm for non-uniform microfluidic cooling of 3D integrated circuits. The Integration VLSI Journal, 2013, 46, 57-68.	2.1	12
103	A new event-driven Dynamic Vision Sensor based Physical Unclonable Function for camera authentication in reactive monitoring system. , 2016, , .		12
104	Low-cost fortification of arbiter PUF against modeling attack. , 2017, , .		12
105	An energy-efficient true random number generator based on current starved ring oscillators. , 2017, , .		12
106	Facial biohashing based user-device physical unclonable function for bring your own device security. , 2018, , .		12
107	Fingerprinting Deep Neural Networks - a DeepFool Approach. , 2021, , .		12
108	Adaptive exact optimisation of minimally testable FPRM expansions. IEE Proceedings: Computers and Digital Techniques, 1998, 145, 385.	1.6	11

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109	Modified reduced adder graph algorithm for multiplierless FIR filters. Electronics Letters, 2005, 41, 302.	1.0	11
110	Watermarking for IP Protection through Template Substitution at Logic Synthesis Level. , 2007, , .		11
111	New power index model for switching power analysis from adder graph of FIR filter. , 2009, , .		11
112	A compact current mode neuron circuit with Gaussian taper learning capability. , 2009, , .		11
113	Cluster-based distributed active current timer for hardware Trojan detection. , 2013, , .		11
114	Design of Optimal Scan Tree Based on Compact Test Patterns for Test Time Reduction. IEEE Transactions on Computers, 2015, 64, 3417-3429.	3.4	11
115	New Algorithm for Signed Integer Comparison in ${2^{n+k},2^{n}-1,2^{n}+1,2^{npm 1}-1}$ and Its Efficient Hardware Implementation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 1481-1493.	5.4	11
116	Fast generalized arithmetic and adding transforms. , 0, , .		10
117	Stego-signature at logic synthesis level for digital design IP protection. , 0, , .		10
118	A 0.7V low-power fully programmable Gaussian function generator for brain-inspired Gaussian correlation associative memory. Neurocomputing, 2014, 138, 69-77.	5.9	10
119	FPGA implementation of modeling attack resistant arbiter PUF with enhanced reliability. , 2017, , .		10
120	A New Accurate and Fast Homography Computation Algorithm for Sports and Traffic Video Analysis. IEEE Transactions on Circuits and Systems for Video Technology, 2018, 28, 2993-3006.	8.3	10
121	Flexible optimization of fixed polarity Reed-Muller expansions for multiple output completely and incompletely specified Boolean functions. , 1995, , .		10
122	Efficient Algorithms for Forward and Inverse Transformations between Haar Spectrum and Binary Decisi. , 0, , .		9
123	Mutual conversions between generalised arithmetic expansions and free binary decision diagrams. IET Circuits, Devices and Systems, 1998, 145, 219.	0.6	9
124	A Configurable Dual Moduli Multi-Operand Modulo Adder. , 0, , .		9
125	Self Organizing Feature Map for Color Quantization on FPGA. , 2006, , 225-245.		9
126	Reconfigurable multiple constant multiplication using minimum adder depth. , 2010, , .		9

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127	Using image sensor PUF as root of trust for birthmarking of perceptual image hash. , 2016, , .		9
128	20 Years of research on intellectual property protection. , 2017, , .		9
129	An effective computer algorithm for the calculation of disjoint cube representation of Boolean functions. , 0, , .		8
130	Efficient algorithms for the calculation of Walsh spectrum from OBDD and synthesis of OBDD from Walsh spectrum for incompletely specified Boolean functions. , 0, , .		8
131	Hadamardâ€“Walsh spectral characterization of Reedâ€“Muller expansions. Computers and Electrical Engineering, 1999, 25, 111-134.	4.8	8
132	On the initialization and training methods for Kohonen self-organizing feature maps in color image quantization. , 0, , .		8
133	A New Method for Eye Extraction from Facial Image. , 0, , .		8
134	A Versatile Speech Enhancment System Based on Perceptual Wavelet Denoising. , 0, , .		8
135	Dynamical Systems Guided Design and Analysis of Silicon Oscillators for Central Pattern Generators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 3046-3059.	5.4	8
136	Efficient structural adder pipelining in transposed form FIR filters. , 2015, , .		8
137	Statistical analysis and design of 6T SRAM cell for physical unclonable function with dual application modes. , 2015, , .		8
138	Sizing of SRAM Cell with Voltage Biasing Techniques for Reliability Enhancement of Memory and PUF Functions. Journal of Low Power Electronics and Applications, 2016, 6, 16.	2.0	8
139	A new write-contention based dual-port SRAM PUF with multiple response bits per cell. , 2017, , .		8
140	High-Speed True Random Number Generator Based on Differential Current Starved Ring Oscillators with Improved Thermal Stability. , 2019, , .		8
141	Adder based residue to binary converters for a new balanced 4-moduli set. , 0, , .		7
142	Low voltage, low power (5:2) compressor cell for fast arithmetic circuits. , 0, , .		7
143	Hamming weight pyramid â€“ A new insight into canonical signed digit representation and its applications. Computers and Electrical Engineering, 2007, 33, 195-207.	4.8	7
144	A post-processing scan-chain watermarking scheme for VLSI intellectual property protection. , 2012, , .		7

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145	Thermal simulator of 3D-IC with modeling of anisotropic TSV conductance and microchannel entrance effects. , 2013, , .		7
146	Leakage-resilient memory-based physical unclonable function using phase change material. , 2014, , .		7
147	Hardware Trojan detection with linear regression based gate-level characterization. , 2014, , .		7
148	CMOS image sensor based physical unclonable function for smart phone security applications. , 2014, , .		7
149	Current mirror array: A novel lightweight strong PUF topology with enhanced reliability. , 2017, , .		7
150	A novel low power low voltage full adder cell. , 0, , .		6
151	Operations on Boolean functions and variables in spectral domain of arithmetic transform. , 0, , .		6
152	Calculation of arithmetic spectra from free binary decision diagrams. , 0, , .		6
153	Generalised k-variable-mixed-polarity Reedâ€“Muller expansions for system of Boolean functions and their minimisation. IET Circuits, Devices and Systems, 2000, 147, 201.	0.6	6
154	HWP: a new insight into canonical signed digit. , 0, , .		6
155	Efficient algorithms for common subexpression elimination in digital filter design. , 0, , .		6
156	Low Power FIR Filter Realization using Minimal Difference Coefficients: Part I - Complexity Analysis. , 2006, , .		6
157	High-speed and low-power serial accumulator for serial/parallel multiplier. , 2008, , .		6
158	A very low power 0.7 V subthreshold fully programmable Gaussian function generator. , 2010, , .		6
159	New algorithm for signed integer comparison in four-moduli superset {2ⁿ, 2ⁿ −1, 2ⁿ +1, 2ⁿ⁺¹−1}. , 2014, , .		6
160	A low-voltage, low power STDP synapse implementation using domain-wall magnets for spiking neural networks. , 2016, , .		6
161	A new watermarking scheme on scan chain ordering for hard IP protection. , 2017, , .		6
162	New Hardware and Power Efficient Sporadic Logarithmic Shifters for DSP Applications. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 896-900.	2.7	6

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163	A Sub-pico Joules Per Bit Robust Physical Unclonable Function Based on Subthreshold Voltage References. , 2018, , .		6
164	Editorial TVLSI Positioningâ€"Continuing and Accelerating an Upward Trajectory. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 253-280.	3.1	6
165	An Efficient Full Hardware Implementation of Extended Merkle Signature Scheme. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 682-693.	5.4	6
166	Properties and applications of paired Haar transform. , 0, , .		5
167	Calculation of paired Haar spectra for systems of incompletely specified Boolean functions. , 0, , .		5
168	NPN classification using weight and literal vectors of Reed-Muller expansion. Electronics Letters, 1999, 35, 798.	1.0	5
169	Self-organizing topological tree. , 0, , .		5
170	A Novel Multiplexer Based Truncated Array Multiplier. , 0, , .		5
171	Low error bit width reduction for structural adders of FIR filters. , 2011, , .		5
172	Sign-Extension Avoidance and Word-Length Optimization by Positive-Offset Representation for FIR Filter Design. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 916-920.	3.0	5
173	Base Transformation With Injective Residue Mapping for Dynamic Range Reduction in RNS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 2248-2259.	5.4	5
174	Low-power, lightweight and reliability-enhanced current starved inverter based RO PUFs. , 2016, , .		5
175	Area- and Power-Efficient Nearly-Linear Phase Response IIR Filter by Iterative Convex Optimization. IEEE Access, 2019, 7, 22952-22965.	4.2	5
176	Detecting Adversarial Examples for Deep Neural Networks via Layer Directed Discriminative Noise Injection. , 2019, , .		5
177	Stealthy and Robust Glitch Injection Attack on Deep Learning Accelerator for Target With Variational Viewpoint. IEEE Transactions on Information Forensics and Security, 2021, 16, 1928-1942.	6.9	5
178	Haar spectra-based entropy approach to quasi-minimisation of FBDDs. IEE Proceedings: Computers and Digital Techniques, 1999, 146, 41.	1.6	5
179	In-place transformation of generalized and complex spectra through algebraic decision diagrams. , 0, , .		4
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181	Algorithm and architecture for a high density, low power scalar product macrocell. IEE Proceedings: Computers and Digital Techniques, 2004, 151, 161.	1.6	4
182	Local Search Method for FIR Filter Coefficients Synthesis. , 0, , .		4
183	A new contention resolution algorithm for the design of minimal logic depth multiplierless filters. , 0, , .		4
184	A New Design Method to Modulo 2>sup<n>/sup<-1 Squaring. , 0, , .		4
185	A Novel Covalent Redundant Binary Booth Encoder. , 0, , .		4
186	Fast hard multiple generators for radix-8 Booth encoded modulo 2ⁿ−1 and modulo 2ⁿ+1 multipliers. , 2010, , .		4
187	A novel counter-based low complexity inner-product architecture for high speed inputs. , 2010, , .		4
188	Performance analysis of different special moduli sets for RNS-based inner product step processor. , 2010, , .		4
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