Masahiro Aoyagi

List of Publications by Year
in descending order

193	1,659	471509 17	414414 32
papers	citations	h-index	g-index

194	194	194	687
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Niobium nitride Josephson tunnel junctions with magnesium oxide barriers. Applied Physics Letters, 1985, 46, 1098-1100.	3.3	133
2	High quality Nb/Alâ€AlOx/Nb Josephson junction. Applied Physics Letters, 1985, 46, 1179-1181.	3.3	101
3	New fabrication process for Josephson tunnel junctions with (niobium nitride, niobium) doubleâ€layered electrodes. Applied Physics Letters, 1982, 41, 1097-1099.	3.3	69
4	All refractory Josephson tunnel junctions fabricated by reactive ion etching. IEEE Transactions on Magnetics, 1983, 19, 827-830.	2.1	59
5	Specific capacitance of Nb/AlOx/Nb Josephson junctions with critical current densities in the range of 0.1â€“18 kA/cm2. Applied Physics Letters, 1995, 66, 2134-2136.	3.3	59
6	Temperature-dependent properties of niobium nitride Josephson tunnel junctions. IEEE Transactions on Magnetics, 1987, 23, 1464-1471.	2.1	51
7	Synthesis of a Novel Poly(binaphthylene ether) Containing Trifluoromethyl Groups with a Low Dielectric Constant. Macromolecules, 2006, 39, 3964-3966.	4.8	51
8	An integration of all refractory Josephson logic LSI circuit. IEEE Transactions on Magnetics, 1985, 21, 102-109.	2.1	48
9	A 1 kbit Josephson random access memory using variable threshold cells. IEEE Journal of Solid-State Circuits, 1989, 24, 1034-1040.	5.4	34
10	Liquid-Nitrogen-Cooled Dry Etching of YBaCuO Thin Films. Japanese Journal of Applied Physics, 1992, 31, L1044-L1046.	1.5	34
11	A 4-bit Josephson computer ETL-JC1. IEEE Transactions on Applied Superconductivity, 1991, 1, 37-47.	1.7	32
12	Rapid single-flux-quantum dual-rail logic for asynchronous circuits. IEEE Transactions on Applied Superconductivity, 1997, 7, 2705-2708.	1.7	27
13	Improved Fabrication Method for Nb/Al/AlOx/Al/Nb Superconducting Tunnel Junctions as X-Ray Detectors. Japanese Journal of Applied Physics, 2000, 39, 5090-5094.	1.5	27
14	Fabrication of High-Density Wiring Interposer for 10 GHz 3D Packaging Using a Photosensitive Multiblock Copolymerized Polyimide. Japanese Journal of Applied Physics, 2004, 43, 4141-4145.	1.5	25
15	A multichip superconducting microcomputer ETL-JC1. IEEE Transactions on Magnetics, 1991, 27, 2610-2617.	2.1	22
16	A Josephson 4 bit RALU for a prototype computer. IEEE Journal of Solid-State Circuits, 1989, 24, 1076-1084.	5.4	20
17	Integrated DCâ€“SQUID Magnetometer. Japanese Journal of Applied Physics, 1987, 26, 1050-1055.	1.5	19
18	An interface circuit for a Josephson-CMOS hybrid digital system. IEEE Transactions on Applied Superconductivity, 1999, 9, 3314-3317.	1.7	18

#	Article	IF	Citations
19	High speed logic operations of all refractory Josephson integrated circuits. Applied Physics Letters, 1983, 43, 213-215.	3.3	17
20	Fabrication process for Josephson computer ETL-JC1 using Nb tunnel junctions. IEEE Transactions on Magnetics, 1991, 27, 3109-3112.	2.1	16
21	Low-impedance evaluation of power distribution network for decoupling capacitor embedded interposers of 3-D integrated LSI system. , 2010, , .		16
22	Josephson address control unit IC for a 4-bit microcomputer prototype. IEEE Transactions on Magnetics, 1989, 25, 789-794.	2.1	15
23	A fully operational 1 kb variable threshold Josephson RAM. IEEE Journal of Solid-State Circuits, 1991, 26, 572-577.	5.4	15
24	Investigation of low-temperature deposition high-uniformity coverage Parylene-HT as a dielectric layer for 3D interconnection. , 2014, , .		15
25	All Niobium Nitride Josephson Junction with Hydrogenated Amorphous Silicon Barrier and its Application to the Logic Circuit. Japanese Journal of Applied Physics, 1984, 23, L916-L918.	1.5	13
26	NbN/MgO/NbN Josephson Junctions for Integrated Circuits. Japanese Journal of Applied Physics, 1992, 31, 1778-1783.	1.5	13
27	A novel method of hotspot temperature reduction for a 3D stacked CMOS IC chip device fabricated on an ultrathin substrate. Journal of Micromechanics and Microengineering, 2013, 23, 025020.	2.6	13
28	Validation of TSV thermo-mechanical simulation by stress measurement. Microelectronics Reliability, 2016, 59, 95-101.	1.7	13
29	Superconductor Wiring in Multichip Module for Josephson LSI Circuits. Japanese Journal of Applied Physics, 1993, 32, L898-L900.	1.5	12
30	Vortex phases and energy dissipation in narrow Nb strips: Reduction of collective pinning. Physical Review B, 1993, 47, 5481-5484.	3.2	12
31	Low-Cost Optical Subassembly Using VCSEL Pre-Self-Aligned With Optical Fiber for Optical Interconnect Applications. Journal of Lightwave Technology, 2009, 27, 4516-4523.	4.6	12
32	Impact of die thinning on the thermal performance of a central TSV bus in a 3D stacked circuit. Microelectronics Journal, 2015, 46, 1106-1113.	2.0	12
33	Fabrication and stress analysis of annular-trench-isolated TSV. Microelectronics Reliability, 2016, 63, 142-147.	1.7	12
34	A 1 Âµm Cross-Line Junction Process. , 1986, , 557-563.		12
35	Sub-Micron-Accuracy Gold-to-Gold Interconnection Flip-Chip Bonding Approach for Electronicsâ€“Optics Heterogeneous Integration. Japanese Journal of Applied Physics, 2013, 52, 04CB08.	1.5	12
36	PECVD SiO<inf>2</inf>film as a junction isolation for all refractory Josephson IC. IEEE Transactions on Magnetics, 1987, 23, 1389-1392.	2.1	11

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37	Josephson LSI fabrication technology using NbN/MgO/NbN tunnel junctions. IEEE Transactions on Magnetics, 1991, 27, 3180-3183.	2.1	11
38	Development of superconducting tunnel junctions with an aluminum-oxide insulation layer for X-ray detection. IEEE Transactions on Applied Superconductivity, 1999, 9, 4475-4478.	1.7	11
39	A basic circuit for asynchronous superconductive logic using RSFQ gates. Superconductor Science and Technology, 1996, 9, A46-A49.	3.5	10
40	Interconnection of Micropad Electrodes by Controlled â€œExtraneousâ€•Deposition of Electroless NiB Film. Electrochemical and Solid-State Letters, 2007, 10, D92.	2.2	10
41	Fabrication and electrical characterization of Parylene-HT liner bottom-up copper filled through silicon via (TSV). , 2014, , .		10
42	Analysis of thermal stress distribution for TSV with novel structure. , 2014, , .		10
43	15-Âµm-pitch Cu/Au interconnections relied on self-aligned low-temperature thermosonic flip-chip bonding technique for advanced chip stacking applications. Japanese Journal of Applied Physics, 2014, 53, 04EB04.	1.5	10
44	Methods to reduce thermal stress for TSV Scaling â^¼TSV with novel structure: Annular-Trench-Isolated TSV. , 2015, , .		10
45	Development of a high-yield via-last through silicon via process using notchless silicon etching and wet cleaning of the first metal layer. Japanese Journal of Applied Physics, 2017, 56, 07KE02.	1.5	10
46	Submicron NbN Josephson tunnel junctions for digital applications. IEEE Transactions on Magnetics, 1989, 25, 1223-1226.	2.1	9
47	Submicron NbN/MgO/NbN Josephson tunnel junctions and their application to the logic circuit. IEEE Transactions on Applied Superconductivity, 1992, 2, 183-186.	1.7	9
48	Observation of Josephson self-coupling inNbAlOxNbtunnel junctions. Physical Review B, 1994, 50, 9664-9667.	3.2	9
49	Low-Cost and High-Density 10Gbps/ch Optical Parallel Link Module for Multi-Terabit Router Application. , 2006, , .		9
50	Impact of joint materials on the reliability of double-side packaged SiC power devices during high temperature aging. Journal of Materials Science: Materials in Electronics, 2010, 21, 917-925.	2.2	9
51	COOL interconnect low power interconnection technology for scalable 3D LSI design. , 2011, , .		9
52	Copper-Filled Through-Silicon Vias With Parylene-HT Liner. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2016, 6, 510-517.	2.5	9
53	Residual stress investigation of via-last through-silicon via by polarized Raman spectroscopy measurement and finite element simulation. Japanese Journal of Applied Physics, 2018, 57, 07MF02.	1.5	9
54	Subgap characteristics of Nb/AlOx/Nb tunnel junctions with high critical current density. IEEE Transactions on Applied Superconductivity, 1995, 5, 3073-3076.	1.7	8

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55	Noise and gain in frequency mixers with NbN SIS junctions. IEEE Transactions on Applied Superconductivity, 1997, 7, 1077-1080.	1.7	8
56	Interlayer dielectric process for LSI circuits using positive photosensitive polyimide synthesized by block-copolymerization. , 2001, , .		8
57	New fabrication process for josephson tunnel junctions using photosensitive polyimide insulation layer for superconducting integrated circuits. IEEE Transactions on Applied Superconductivity, 2003, 13, 119-122.	1.7	8
58	Fluidic platform with embedded differential capacitively coupled contactless conductivity detector for micro-object sensing. International Journal of Nanotechnology, 2018, 15, 24.	0.2	8
59	Stress investigation of annular-trench-isolated TSV by polarized Raman spectroscopy measurement and finite element simulation. Microelectronics Reliability, 2019, 99, 125-131.	1.7	8
60	Band-Stop Filter Effect of Power/Ground Plane on Through-Hole Signal Via in Multilayer PCB. IEICE Transactions on Electronics, 2006, E89-C, 551-559.	0.6	8
61	A Josephson 10-b instruction 128-word ROM unit. IEEE Journal of Solid-State Circuits, 1990, 25, 971-978.	5.4	7
62	Fabrication of submicron Nb/AlO/sub x//Nb Josephson junctions using ECR plasma etching technique. IEEE Transactions on Applied Superconductivity, 1997, 7, 2644-2648.	1.7	7
63	Investigation of a Sic Module with a High Operating Temperature for Power Applications. , 2007, , .		7
64	High-density and Low-cost 10-Gbps x 12ch Optical Modules for High-end Optical Interconnect Applications. , 2008, , .		7
65	Vertically Pluggable and Compact 10-Gb/s$,imes,$12-Channel Optical Modules With Anisotropic Conductive Film for Over 100-Gb/s Optical Interconnect Systems. Journal of Lightwave Technology, 2009, 27, 3249-3258.	4.6	7
66	Novel through silicon via exposure process comprising Si/Cu grinding, electroless Niâ€“B plating, and wet etching of Si. Japanese Journal of Applied Physics, 2014, 53, 05GE02.	1.5	7
67	Damage Evaluation of Wet-Chemical Si-Wafer Thinning/Backside Via Exposure Process. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2014, 4, 741-747.	2.5	7
68	Flip-chip bonding alignment accuracy enhancement using self-aligned interconnection elements to realize low-temperature construction of ultrafine-pitch copper bump interconnections. , 2014, , .		7
69	Metal contamination evaluation of a TSV reveal process using direct Si/Cu grinding and residual metal removal. , 2015, , .		7
70	Antenna-coupled superconducting contacts in submillimeter and FIR astronomy. Infrared Physics and Technology, 1994, 35, 463-476.	2.9	6
71	An improved etching process used for the fabrication of submicron Nb/AlO/sub x//Nb Josephson junctions. IEEE Transactions on Applied Superconductivity, 1995, 5, 2334-2337.	1.7	6
72	Influence of a NbN overlayer on Nb/Alâ€“AlOx/Nb high quality Josephson tunnel junctions for xâ€ray detection. Applied Physics Letters, 1995, 67, 3340-3342.	3.3	6

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73	A niobiumnitride mixer with niobium tuning circuit. Applied Physics Letters, 1996, 69, 4102-4104.	3.3	6
74	Properties of Substrate Phonon Events in Superconducting Tunnel Junctions Induced by X-Ray Absorption. Japanese Journal of Applied Physics, 2000, 39, 1710-1718.	1.5	6
75	Development of superconducting tunnel junctions for ultra soft X-ray detectors. IEEE Transactions on Applied Superconductivity, 2001, 11, 721-723.	1.7	6
76	On-chip coil integrated superconducting tunnel junction for a high performance X-ray detector. Physica C: Superconductivity and Its Applications, 2002, 372-376, 403-406.	1.2	6
77	Cool System scalable 3-D stacked heterogeneous Multi-Core / Multi-Chip architecture for ultra low-power digital TV applications. , 2012, , .		6
78	Modified thermosonic flip-chip bonding based on electroplated Cu microbumps and concave pads for high-precision low-temperature assembly applications. , 2013, , .		6
79	30-GHz High-Frequency Application of Screen Printed Interconnects on an Organic Substrate. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2017, 7, 1506-1515.	2.5	6
80	Fabrication and performance of all refractory josephson logic circuits for 1 Kbit SFQ memory. IEEE Transactions on Magnetics, 1985, 21, 733-736.	2.1	5
81	NbN-MgO-NbN junctions prepared on room-temperature quartz substrates for quasiparticle mixers. IEEE Transactions on Applied Superconductivity, 1997, 7, 2603-2606.	1.7	5
82	Precise patterning technique for Nb junctions using optical proximity correction. IEEE Transactions on Applied Superconductivity, 2001, 11, 381-384.	1.7	5
83	A GHz multi-channel cryogenic test fixture for superconducting integrated circuit testing. IEEE Transactions on Applied Superconductivity, 2003, 13, 459-462.	1.7	5
84	Double Relaxation Oscillation SQUID with a 4JL On-Chip Digital Flux Locked-Loop Circuit. IEEE Transactions on Applied Superconductivity, 2005, 15, 332-335.	1.7	5
85	Self-Alignment of Optical Devices With Fiber for Low-Cost Optical Interconnect Modules. IEEE Photonics Technology Letters, 2008, 20, 193-195.	2.5	5
86	Joint Reliability of Double-Side Packaged SiC Power Devices to a DBC Substrate with High Temperature Solders. , 2008, , .		5
87	High optical coupling efficiency using 45Â°-ended fibre for low-height and low-cost optical interconnect modules. Electronics Letters, 2008, 44, 724.	1.0	5
88	Anisotropic Deposition of Localized Electroless Nickel for Preferential Bridge Connection. Journal of the Electrochemical Society, 2010, 157, D65.	2.9	5
89	Development of a chip prober for pre-bond testing of a 3D-IC. , 2013, , .		5
90	Development of decoupling capacitor embedded interposers using narrow gap chip parts mounting technology with wideband ultralow PDN impedance. , 2013, , .		5

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91	Improvement of a TSV Reveal Process Comprising Direct Si/Cu Grinding and Residual Metal Removal. , 2016, , .		5
92	Two-axis tilt angle detection based on dielectric liquid capacitive sensor. , 2016, , .		5
93	A Robust Two-axis Tilt Angle Sensor Based on Air/Liquid Two-phase Dielectric Capacitive Sensing Structure. IETE Journal of Research, 2020, 66, 685-696.	2.6	5
94	Properties of Large-Sized Nb-Based Superconducting TunnelJunctions for X-Ray Detection. Japanese Journal of Applied Physics, 1991, 30, 1969-1974.	1.5	4
95	A microstrip-coil integration on superconducting tunnel junctions for X-ray detection. IEEE Transactions on Applied Superconductivity, 2001, 11, 700-703.	1.7	4
96	Efficient Fabrication Process for Superconducting Integrated Circuits Using Photosensitive Polyimide Insulation Layers. IEEE Transactions on Applied Superconductivity, 2005, 15, 94-97.	1.7	4
97	A novel chip joint method for high temperature operated SiC power modules. , 2006, , .		4
98	A Study on Coupling Efficiency between VCSEL and 45Â°-angled mirror component for Low-cost and High-density 10Gbps/ch Optical Parallel Link Module. Conference Proceedings - Lasers and Electro-Optics Society Annual Meeting-LEOS, 2007, , .	0.0	4
99	Novel Flip-Chip Bonding Technology using Chemical Process. , 2007, , .		4
100	A method of “chemical flip-chip bonding” without loading and heating for ultra-fine chip-to-substrate interconnects. , 2009, , .		4
101	Low-impedance power distribution network of decoupling capacitor embedded interposers for 3-D integrated LSI system. , 2009, , .		4
102	A Novel Three-Dimensional Packaging Method for Al-Metalized SiC Power Devices. IEEE Transactions on Advanced Packaging, 2009, 32, 773-779.	1.6	4
103	New optical three dimensional structure measurement method of cone shape micro bumps used for 3D LSI chip stacking. , 2013, , .		4
104	Fine-pitch probing on TSVs and microbumps using a chip prober having a transparent membrane probe card. , 2014, , .		4
105	Fabrication of a membrane probe card using transparent film for three-dimensional integrated circuit testing. Japanese Journal of Applied Physics, 2014, 53, 06JM06.	1.5	4
106	Small-diameter TSV reveal process using direct Si/Cu grinding and metal contamination removal. , 2014, , .		4
107	Low Residual Stress in Si Substrate of Annular-Trench-Isolated TSV. , 2016, , .		4
108	Cool Interconnect: A 1024-bit Wide Bus for Chip-to-Chip Communications in 3-D Integrated Circuits. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2019, 9, 525-535.	2.5	4

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109	Fine Cone-shaped Bumps for Three-dimensional LSI Packageâ€"An Optimization of Thermocompression Bonding Process. Sensors and Materials, 2018, 30, 2905.	0.5	4
110	Chip layout design of a Josephson LSI circuit for examining high-speed operability by using a standard cell automatic placement and routing technique. IEEE Transactions on Applied Superconductivity, 1994, 4, 169-176.	1.7	3
111	<title>Noise properties of a mixer with SIS NbN quasi-particle tunnel junctions</title>. , 1995, , .		3
112	Numerical studies of interchip pulse transmission for complex RSFQ systems. IEEE Transactions on Applied Superconductivity, 1999, 9, 3725-3728.	1.7	3
113	10-Gbps Signal Propagation of High-Density Wiring Interposer Using Photosensitive Polyimide for 3D Packaging. , 0, , .		3
114	A Method of Fabricating Bump-Less Interconnects Applicable to Wafer-Scale Flip-Chip Bonding. , 2008, , .		3
115	Chemical flip-chip bonding method for fabricating 10-.MU.m-pad-pitch interconnect. IEICE Electronics Express, 2008, 5, 732-737.	0.8	3
116	SrTiO<inf>3</inf> thin film decoupling capacitors on Si interposers for 3D system integration. , 2009, , .		3
117	Development of damage-less wet-chemical silicon-wafer thinning process for three-dimensional integration. , 2012, , .		3
118	Wet-Chemical Silicon Wafer Thinning Process for High Chip Strength. ECS Transactions, 2012, 45, 141-150.	0.5	3
119	Wideband ultralow power distribution network impedance evaluation of decoupling capacitor embedded interposers for 3-D integrated LSI system. , 2013, , .		3
120	Development of Cu-less TSV reveal process using Si/Cu grinding, electroless Ni plating, and alkaline etching of Si. , 2013, , .		3
121	Ultrawideband ultralow PDN impedance of decoupling capacitor embedded interposers using narrow gap chip parts mounting technology for 3-D integrated LSI system. , 2014, , .		3
122	Investigation of effects of die thinning on central TSV bus driver thermal performance. , 2014, , .		3
123	Method for back-annotating per-transistor power values onto 3DIC layouts to enable detailed thermal analysis. , 2014, , .		3
124	Investigation into the thermal effects of thinning stacked dies in three-dimensional integrated circuits. , 2015, , .		3
125	Thermal Stress Comparison of Annular-Trench-Isolated (ATI) TSV with Cu and Solder Core. , 2019, , .		3
126	Material effect on thermal stress of annular-trench-isolated through silicon via (TSV). Japanese Journal of Applied Physics, 2020, 59, SLLH01.	1.5	3

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127	Formation of Au Microbump Arrays for Flip-Chip Bonding Using Electroless Au Deposition from a Non-Cyanide Plating Bath. Transactions of the Japan Institute of Electronics Packaging, 2009, 2, 109-115.	0.4	3
128	Palladium Thin-Film Resistors for Josephson LSI Circuits. Japanese Journal of Applied Physics, 1992, 31, 2550-2553.	1.5	2
129	Low noise submillimeter SIS receiver with niobium nitride quasiparticle tunnel junctions. Journal of Infrared, Millimeter and Terahertz Waves, 1996, 17, 1139-1147.	0.6	2
130	Fabrication process of superconducting integrated circuits with submicron Nb/AlO x /Nb junctions using electron-beam direct writing technique. , 1997, , .		2
131	A high-resolution X-ray detection system using STJ and SQUID amplifier. IEEE Transactions on Applied Superconductivity, 2001, 11, 704-707.	1.7	2
132	On-chip coil-integrated STJ using the persistent superconducting current for photon detectors. IEEE Transactions on Applied Superconductivity, 2003, 13, 1132-1138.	1.7	2
133	Micropattern Formation of Photosensitive Imide Block Copolymer Thick Films. Journal of Photopolymer Science and Technology = [Fotoporima Konwakai Shi], 2005, 18, 301-306.	0.3	2
134	Extracting dielectric constant of low-k thin film material for interposer of 3-D multilayer packaging. , 2006, , .		2
135	Compliant bump technology for back-side illuminated CMOS image sensor. , 2009, , .		2
136	Silicon wafer thinning and backside via exposure by wet etching. , 2012, , .		2
137	Thermal Conductive Properties of a Semiconductor Laser on a Polymer Interposer. Japanese Journal of Applied Physics, 2013, 52, 04CG05.	1.5	2
138	Copper filled TSV formation with Parylene-HT insulator for low-temperature compatible 3D integration. , 2014, , .		2
139	3D IC testing using a chip prober and a transparent membrane probe card. , 2014, , .		2
140	Twice-etched silicon approach for via-last through-silicon-via with a Parylene-HT liner. , 2015, , .		2
141	Wet cleaning process for high-yield via-last TSV formation. , 2016, , .		2
142	Impact of thinning stacked dies on the thermal resistance of bump-bonded three-dimensional integrated circuits. Microelectronics Reliability, 2016, 67, 2-8.	1.7	2
143	Evaluation of substrate noise suppression method to mitigate crosstalk among trough-silicon vias. Japanese Journal of Applied Physics, 2018, 57, 04FC07.	1.5	2
144	Niobium Nitride Josephson Junctions with Double-Tunnel Barriers. Japanese Journal of Applied Physics, 1987, 26, 1611.	1.5	2

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145	NbN Josephson junction with high critical current density for integrated circuits. Superconductor Science and Technology, 1991, 4, 626-628.	3.5	1
146	Superconducting sampling measurement system for characterization of electronic packaging. , 0, , .		1
147	Detection of heavy ions using Nb-based superconducting tunnel junction. IEEE Transactions on Applied Superconductivity, 2001, 11, 712-715.	1.7	1
148	X-Ray Detection Using Superconducting Tunnel Junctions With Polyimide Insulation Layer. IEEE Transactions on Applied Superconductivity, 2005, 15, 606-608.	1.7	1
149	New Fabrication Process for Superconducting Quantum Interference Devices With Nb/AlAlOx/Nb Junctions by Using Photosensitive Polyimide Insulation Layers. IEEE Transactions on Applied Superconductivity, 2005, 15, 825-828.	1.7	1
150	Polyimide Buffer Layer for STJ Photon Detector. Journal of Physics: Conference Series, 2006, 43, 1319-1321.	0.4	1
151	Hot spots suppression by high thermal conductivity film in thin-sub strate CMOS ICs for 3D integration. , 2012, , .		1
152	Investigation of optimized high-density flip-chip interconnect design including micro Au bumps and underfill for ultrabroadband (DC-40GHz) applications. , 2012, , .		1
153	Investigation of optimized high-density flip-chip interconnect design including micro Au bumps for 3-D stacked LSI packaging. , 2013, , .		1
154	High-precision integration approach based on alignment maintaining flip-chip bonding using cone shaped bump and truncated pyramid pad. , 2014, , .		1
155	Basic evaluation of Au micro-bumps formed by cyanide-free electroless Au plating process. , 2014, , .		1
156	High-speed optical three dimensional measurement method for micro bump inspection in 3D LSI chip stacking technology. , 2015, , .		1
157	Sensitivity of the thermal profile of bump-bonded 3D systems to inter-die bonding layer properties. , 2015, , .		1
158	Guard-ring monitoring system for inspecting defects in TSV-based data buses. , 2015, , .		1
159	Fabrication of superconducting tunnel junctions with embedded coil for applying magnetic field. Physica C: Superconductivity and Its Applications, 2016, 530, 90-92.	1.2	1
160	Thermal impact of extreme die thinning in bump-bonded three-dimensional integrated circuits. Microelectronics Reliability, 2017, 79, 380-386.	1.7	1
161	Coplanar differential capacitively coupled contactless conductivity detection (CD-C4D) sensor for micro object inside fluidic flow recognization. , 2017, , .		1
162	Fabrication and stacking of through-silicon-via array chip formed by notchless Si etching and wet cleaning of first metal layer. Japanese Journal of Applied Physics, 2019, 58, SDDL09.	1.5	1

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163	Hardness Characteristics of Au Cone-Shaped Bumps Targeted for 3-D Packaging Applications. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2019, 9, 419-426.	2.5	1
164	Josephson Junctions Consisting of all (103) Oriented YBaCuO/PrBaCuO/YBaCuO Trilayer Films. , 1994, , 1063-1066.		1
165	Title is missing!. Journal of Japan Institute of Electronics Packaging, 2009, 12, 606-615.	0.1	1
166	Investigation of metal contamination induced by a through silicon via reveal process using direct Si/Cu grinding and residual metal removal. Japanese Journal of Applied Physics, 2016, 55, 06GP06.	1.5	1
167	Josephson computer technology. Endeavour, 1991, 15, 58-65.	0.4	0
168	Design of a 16 kbit variable threshold Josephson RAM. IEEE Transactions on Applied Superconductivity, 1993, 3, 2675-2678.	1.7	0
169	A Josephson built-in self-testing (JBIST) system for gigahertz functional tests of Josephson RAMs. Superconductor Science and Technology, 1996, 9, A50-A54.	3.5	0
170	Development of a compact system for high-resolution X-ray detection using a SQUID amplifier. IEEE Transactions on Applied Superconductivity, 1999, 9, 3858-3861.	1.7	0
171	Spectral features of substrate phonon events obtained by illuminating superconducting tunnel junctions with X-rays. IEEE Transactions on Applied Superconductivity, 2001, 11, 708-711.	1.7	0
172	High-Tc interferometers using all YBa2Cu3O7â˜Î´ trilayer junctions. Applied Physics Letters, 2003, 83, 2390-2392.	3.3	0
173	X-ray detection by an on-chip coil integrated superconducting tunnel junction. Review of Scientific Instruments, 2003, 74, 3258-3262.	1.3	0
174	Response of an On-Chip Coil-Integrated Superconducting Tunnel Junction to X-rays. Japanese Journal of Applied Physics, 2003, 42, 2860-2863.	1.5	0
175	Superconducting ultrahigh-speed time domain reflectometry measurement system for electrical characterization of transmission line structures. Superconductor Science and Technology, 2003, 16, 1434-1437.	3.5	0
176	Precise high frequency measurement method without connectors for small diameter coaxial cable. , 2004, , .		0
177	Ultralow impedance evaluation system of wideband frequency for power distribution network of decoupling capacitor embedded substrates. , 2009, , .		0
178	Ultralow impedance analysis and evaluation of power distribution network for decoupling capacitor embedded interposers of 3-D integrated LSI system. , 2012, , .		0
179	Special session 4C: Hot topic 3D-IC design and test. , 2013, , .		0
180	High-Speed Alkaline Etching for Backside Exposure of Through Silicon Vias. ECS Transactions, 2013, 50, 39-48.	0.5	0

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181	Investigation of a microchannel-based cooling interposer for high-performance memory-on-logic 3DIC design. , 2013, , .		0
182	Substrate monitoring system for inspecting defects in TSV-based data buses. , 2014, , .		0
183	A method enabling height-control of chips for edge-emitting laser stacking. Japanese Journal of Applied Physics, 2015, 54, 04DB02.	1.5	0
184	Investigation of effects of metalization on heat spreading in bump-bonded 3D systems. , 2015, , .		0
185	High frequency performance characterization of super-fine inkjet printed silver traces. , 2016, , .		0
186	Integration of a microfluidic chip with multiplexed optical fluorescence detector through anisotropic etching of Si using Tetramethylammonium hydroxide (TMAH). , 2016, , .		0
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