Baris Taskin

List of Publications by Year
in descending order

86	460	1163117 8	1199594 12
papers	citations	h-index	g-index

87	87	87	203
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Multiphase Digital Low-Dropout Regulators. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 40-50.	3.1	0
2	Interconnects for DNA, Quantum, In-Memory, and Optical Computing: Insights From a Panel Discussion. IEEE Micro, 2022, 42, 40-49.	1.8	11
3	Resonant Clock Synchronization With Active Silicon Interposer for Multi-Die Systems. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 1636-1645.	5.4	8
4	Comprehensive Low Power Adiabatic Circuit Design with Resonant Power Clocking. , 2020, , .		2
5	SnackNoC: Processing in the Communication Layer. , 2020, , .		6
6	TSVâ€based antenna for onâ€chip wireless communication. IET Microwaves, Antennas and Propagation, 2020, 14, 302-307.	1.4	2
7	TSV Antennas for Multi-Band Wireless Communication. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2020, 10, 100-113.	3.6	15
8	FOPAC: Flexible On-Chip Power and Clock. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 4628-4636.	5.4	1
9	Design and fabrication of twoâ€port threeâ€beam switched beam antenna array for 60 GHz communication. IET Microwaves, Antennas and Propagation, 2019, 13, 1438-1442.	1.4	6
10	RotaSYN: Rotary Traveling Wave Oscillator SYNthesizer. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 2685-2698.	5.4	7
11	SLECTS: Slew-Driven Clock Tree Synthesis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 864-874.	3.1	10
12	The Adiabatically Driven StrongARM Comparator. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1957-1961.	3.0	2
13	Distributed Digital Low-Dropout Regulators with Phase Interleaving for On-Chip Voltage Noise Mitigation. , 2019, , .		3
14	Robust Low Power Clock Synchronization for Multi-Die Systems. , 2019, , .		4
15	Slew Merging Region Propagation for Bounded Slew and Skew Clock Tree Synthesis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1-10.	3.1	6
16	Custard: ASIC Workload-Aware Reliable Design for Multicore IoT Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 700-710.	3.1	3
17	Vertical Arbitration-Free 3-D NoCs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1853-1866.	2.7	3
18	mm Wave Antenna Gain Switching to Mitigate Indoor Blockage. , 2018, , .		1

#	Article	IF	Citations
19	Low Frequency Rotary Traveling Wave Oscillators. , 2018, , .		5
20	Towards Design Decisions for Genetic Algorithms in Clock Tree Synthesis. , 2018, , .		0
21	Towards Cross-Framework Workload Analysis via Flexible Event-Driven Interfaces. , 2018, , .		1
22	NoC Router Lifetime Improvement using Per-Port Router Utilization. , 2018, , .		1
23	Workload-Aware Routing (WAR) for Network-on-Chip Lifetime Improvement. , 2018, , .		6
24	A 900 MHz Charge Recovery Comparator With 40 fJ per Conversion. , 2018, , .		3
25	Wireless NoCs Using Directional and Substrate Propagation Antennas. , 2017, , .		1
26	Charge recovery implementation of an analog comparator: Initial results. , 2017, , .		4
27	Stability of Rotary Traveling Wave Oscillators under process variations and NBTI. , 2017, , .		4
28	Charge recovery logic for thermal harvesting applications. , 2016, , .		0
29	Exploiting useful skew in gated low voltage clock trees. , 2016, , .		0
30	Energy aware routing of multi-level Network-on-Chip traffic. , 2016, , .		2
31	Wireless Network-on-Chip analysis of propagation technique for on-chip communication. , 2016, , .		2
32	Design Methodology for Voltage-Scaled Clock Distribution Networks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 3080-3093.	3.1	18
33	ROA-Brick Topology for Low-Skew Rotary Resonant Clock Network Design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2519-2530.	3.1	9
34	Uncore RPD: Rapid design space exploration of the uncore via regression modeling. , 2015, , .		1
35	Innovative propagation mechanism for inter-chip and intra-chip communication. , 2015, , .		11
36	Can You Trust Your Memory Trace? A Comparison of Memory Traces from Binary Instrumentation and Simulation. , 2015, , .		2

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37	Synchrotrace: synchronization-aware architecture-agnostic traces for light-weight multicore simulation. , 2015, , .		15
38	Enhanced level shifter for multi-voltage operation. , 2015, , .		9
39	Timing characterization of clock buffers for clock tree synthesis. , 2014, , .		6
40	Frequency-centric resonant rotary clock distribution network design. , 2014, , .		2
41	High Performance Low Swing Clock Tree Synthesis with Custom D Flip-Flop Design. , 2014, , .		6
42	Iterative skew minimization for low swing clocks. The Integration VLSI Journal, 2014, 47, 356-364.	2.1	0
43	A microcontroller-based embedded system design course with PSoC3. , 2013, , .		3
44	Sparse-Rotary Oscillator Array (SROA) Design for Power and Skew Reduction. , 2013, , .		10
45	Resonant frequency divider design methodology for dynamic frequency scaling. , 2013, , .		7
46	Wireless on Networks-on-Chip. , 2013, , .		0
47	Skew-bounded low swing clock tree optimization. , 2013, , .		7
48	Synchronization scheme for brick-based rotary oscillator arrays. , 2012, , .		8
49	ZeROA: Zero Clock Skew Rotary Oscillatory Array. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1528-1532.	3.1	4
50	Clock mesh synthesis with gated local trees and activity driven register clustering. , 2012, , .		16
51	A unified design methodology for a hybrid wireless 2-D NoC. , 2012, , .		6
52	3-D Parasitic Modeling for Rotary Interconnects. , 2012, , .		6
53	Multi-voltage domain clock mesh design. , 2012, , .		6
54	Clock mesh synthesis method using the Earth Mover's Distance under transformations. , 2012, , .		2

#	Article	IF	Citations
55	A Reconfigurable Clock Polarity Assignment Flow for Clock Gated Designs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1002-1011.	3.1	7
56	EM and circuit co-simulation of a reconfigurable hybrid wireless NoC on 2D ICs. , 2011, , .		5
57	Steiner tree based rotary clock routing with bounded skew and capacitive load balancing. , 2011, , .		7
58	Process variation sensitivity of the Rotary Traveling Wave Oscillator. , 2011, , .		7
59	ROA-brick topology for rotary resonant clocks. , 2011, , .		7
60	From RTL to GDSII: An ASIC design course development using Synopsys® University Program. , 2011, , .		18
61	CROA: Design and Analysis of the Custom Rotary Oscillatory Array. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1837-1847.	3.1	14
62	Register On MEsh (ROME): A novel approach for clock mesh network synthesis. , 2011, , .		5
63	Reconfigurable clock polarity assignment for peak current reduction of clock-gated circuits. , 2011, , .		1
64	STATISTICAL TIMING ANALYSIS OF THE CLOCK PERIOD IMPROVEMENT THROUGH CLOCK SKEW SCHEDULING. Journal of Circuits, Systems and Computers, 2011, 20, 881-898.	1.5	1
65	Post-CTS Delay Insertion. VLSI Design, 2010, 2010, 1-9.	0.5	16
66	Skew-aware capacitive load balancing for low-power zero clock skew rotary oscillatory array. , 2010, , .		8
67	Skew analysis and bounded skew constraint methodology for rotary clocking technology. , 2010, , .		3
68	Clock buffer polarity assignment considering capacitive load. , 2010, , .		7
69	Leakage current analysis for intra-chip wireless interconnects. , 2010, , .		6
70	Simulation Based Feasibility Study of Wireless RF Interconnects for 3D ICs. , 2010, , .		7
71	Clock Tree Synthesis with XOR Gates for Polarity Assignment. , 2010, , .		10
72	Analysis, Design and Simulation of Capacitive Load Balanced Rotary Oscillatory Array. , 2010, , .		5

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73	Look-Up Table Based Low Power Rotary Traveling Wave Oscillator Design Considering the Skin Effect. Journal of Low Power Electronics, 2010, 6, 491-502.	0.6	0
74	Incremental register placement for low power CTS. , 2009, , .		1
75	Post-CTS clock skew scheduling with limited delay buffering. , 2009, , .		13
76	Design automation scheme for wirelength analysis of resonant clocking technologies. , 2009, , .		1
77	Skew analysis and design methodologies for improved performance of resonant clocking. , 2009, , .		2
78	MULTI-PHASE ROTARY CLOCK SYNCHRONIZATION OF LEVEL-SENSITIVE CIRCUITS. Journal of Circuits, Systems and Computers, 2009, 18, 899-908.	1.5	2
79	Zero clock skew synchronization with rotary clocking technology. , 2009, , .		5
80	Capacitive load balancing for mobius implementation of standing wave oscillator. , 2009, , .		5
81	Statistical timing analysis of nonzero clock skew circuits. , 2008, , .		1
82	Maze router based scheme for rotary clock router. , 2008, , .		2
83	Custom rotary clock router. , 2008, , .		11
84	Post-CTS delay insertion to fix timing violations. , 2008, , .		1
85	Design-for-Debug: A Vital Aspect in Education. , 2007, , .		7
86	A shift-register-based QCA memory architecture. , 2007, , .		2