Junichi Hattori

List of Publications by Year
in descending order

46	309	1040056 9	1125743 13
papers	citations	h-index	g-index

46	46	46	415
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Fully coupled 3-D device simulation of negative capacitance FinFETs for sub 10 nm integration. , 2016, , .		77
2	Material and device engineering in fully depleted silicon-on-insulator transistors to realize a steep subthreshold swing using negative capacitance. Japanese Journal of Applied Physics, 2016, 55, 08PD01.	1.5	20
3	A TCAD device simulator for exotic materials and its application to a negative-capacitance FET. Journal of Computational Electronics, 2019, 18, 534-542.	2.5	19
4	Corrugated Si nanowires with reduced thermal conductivity for wide-temperature-range thermoelectricity. Journal of Applied Physics, 2016, 120, .	2.5	17
5	Perspective of negative capacitance FinFETs investigated by transient TCAD simulation. , 2017, , .		17
6	Fringing field effects in negative capacitance field-effect transistors with a ferroelectric gate insulator. Japanese Journal of Applied Physics, 2018, 57, 04FD07.	1.5	16
7	Scaling consideration and compact model of electron scattering enhancement due to acoustic phonon modulation in an ultrafine free-standing cylindrical semiconductor nanowire. Journal of Applied Physics, 2010, 107, 033712.	2.5	11
8	A Self-Consistent Compact Model of Ballistic Nanowire MOSFET With Rectangular Cross Section. IEEE Transactions on Electron Devices, 2013, 60, 856-862.	3.0	10
9	Carrier and heat transport properties of poly-crystalline GeSn films for thin-film transistor applications. Journal of Applied Physics, 2019, 126, .	2.5	10
10	Ellipsoidal Band Structure Effects on Maximum Ballistic Current in Silicon Nanowires. Japanese Journal of Applied Physics, 2011, 50, 04DN09.	1.5	10
11	Structural advantages of silicon-on-insulator FETs over FinFETs in steep subthreshold-swing operation in ferroelectric-gate FETs. Japanese Journal of Applied Physics, 2017, 56, 04CD10.	1.5	9
12	Multidomain Dynamics of Ferroelectric Polarization and its Coherency-Breaking in Negative Capacitance Field-Effect Transistors. , 2018, , .		9
13	Acoustic phonon modulation and electronâ€“phonon interaction inÂsemiconductor slabs and nanowires. Journal of Computational Electronics, 2011, 10, 104-120.	2.5	8
14	Impact of Isotope Doping on Phonon Thermal Transport in Silicon Nanowires. Japanese Journal of Applied Physics, 2013, 52, 04CN04.	1.5	8
15	Steep switching less than 15 mV dec^{âˆ’1} in silicon-on-insulator tunnel FETs by a trimmed-gate structure. Japanese Journal of Applied Physics, 2019, 58, SBBA16.	1.5	8
16	Compact model of ferroelectric-gate field-effect transistor for circuit simulation based on multidomain Landauâ€“Kalathnikov theory. Japanese Journal of Applied Physics, 2017, 56, 04CE07.	1.5	7
17	Universality in electronâ€“modulated-acoustic-phonon interactions in a free-standing semiconductor nanowire. Mathematical and Computer Modelling, 2010, 51, 880-887.	2.0	5
18	Steep switching in trimmed-gate tunnel FET. AIP Advances, 2018, 8, .	1.3	5

#	Article	IF	Citations
19	Interlayer coupling effect on the performance of monolithic three-dimensional inverters and its dependence on the interlayer dielectric thickness. Japanese Journal of Applied Physics, 2017, 56, 04CC02.	1.5	4
20	Technology computer-aided design simulation of phonon heat transport in semiconductor devices. Japanese Journal of Applied Physics, 2021, 60, SBBA03.	1.5	4
21	Ellipsoidal Band Structure Effects on Maximum Ballistic Current in Silicon Nanowires. Japanese Journal of Applied Physics, 2011, 50, 04DN09.	1.5	3
22	Simulation study of short-channel effects of tunnel field-effect transistors. Japanese Journal of Applied Physics, 2018, 57, 04FD04.	1.5	3
23	A transient simulation approach to obtaining capacitanceâ€“voltage characteristics of GaN MOS capacitors with deep-level traps. Japanese Journal of Applied Physics, 2018, 57, 04FG04.	1.5	3
24	Device Simulation of Negative-Capacitance Field-Effect Transistors With a Ferroelectric Gate Insulator. , 2018, , .		3
25	A Poissonâ€“Schrodinger and cellular automaton coupled approach for two-dimensional electron gas transport modeling of GaN-based high mobility electron transistors. Japanese Journal of Applied Physics, 2021, 60, SBBD04.	1.5	3
26	Form factor increase and its physical origins in electron-modulated acoustic phonon interaction in a free-standing semiconductor plate. Mathematical and Computer Modelling, 2010, 51, 863-872.	2.0	2
27	Electronâ€“Modulated-Acoustic-Phonon Interactions in a Coated Silicon Nanowire. Japanese Journal of Applied Physics, 2010, 49, 04DN09.	1.5	2
28	On the drain bias dependence of long-channel silicon-on-insulator-based tunnel field-effect transistors. Japanese Journal of Applied Physics, 2017, 56, 04CD04.	1.5	2
29	Design of steep-slope negative-capacitance FinFETs for dense integration: Importance of appropriate ferroelectric capacitance and short-channel effects. Japanese Journal of Applied Physics, 2018, 57, 04FD03.	1.5	2
30	Implementation of Coulomb blockade transport on a semiconductor device simulator and its application to tunnel-FET-based quantum dot devices. Japanese Journal of Applied Physics, 2020, 59, SIIE02.	1.5	2
31	Importance of source and drain extension design in cryogenic MOSFET operation: causes of unexpected threshold voltage increases. Applied Physics Express, 2022, 15, 084004.	2.4	2
32	Design and simulation of steep-slope silicon-on-insulator FETs using negative capacitance: Impact of buried oxide thickness and remnant polarization. , 2016, , .		1
33	Axial strain effects on ballistic phonon thermal transport in silicon nanowires. Japanese Journal of Applied Physics, 2016, 55, 04EP07.	1.5	1
34	Enhancement of capacitance benefit by drain offset structure in tunnel field-effect transistor circuit speed associated with tunneling probability increase. Japanese Journal of Applied Physics, 2018, 57, 04FD13.	1.5	1
35	Implementation of Automatic Differentiation to Python-based Semiconductor Device Simulator. , 2019, , .		1
36	A time-dependent Verilog-A compact model for MOS capacitors with interface traps. Japanese Journal of Applied Physics, 2019, 58, SBBD06.	1.5	1

#	Article	IF	Citations
37	Device simulation of negative-capacitance field-effect transistors with a uniaxial ferroelectric gate insulator. Nonlinear Theory and Its Applications IEICE, 2020, 11, 145-156.	0.6	1
38	Buried nanomagnet realizing high-speed/low-variability silicon spin qubits: implementable in error-correctable large-scale quantum computers. , 2021, , .		1
39	Mechanism of extraordinary gate-length dependence of quantum dot operation in isoelectronic-trap-assisted tunnel FETs. Applied Physics Express, 2020, 13, 114001.	2.4	1
40	A theoretical study of effect of gate voltage on electron-modulated-acoustic-phonon interactions in silicon nanowire MOSFETs. , 2010, , .		0
41	A moving mesh method for device simulation. , 2015, , .		0
42	Simulation of GaN MOS capacitance with frequency dispersion and hysteresis. , 2017, , .		0
43	Simulation of deep level transient spectroscopy using circuit simulator with deep level trap model implemented by Verilog-A language. , 2019, , .		0
44	Temperature-dependent mobility modeling of GaN HEMTs by cellular automaton method. , 2021, , .		0
45	TCAD simulation for transition metal dichalcogenide channel Tunnel FETs consistent with ab-initio based NEGF calculation. , 2020, , .		0
46	Cellular automaton approach for carrier degeneracy effects on the electron mobility of high electron mobility transistors. Japanese Journal of Applied Physics, 2022, 61, SC1043.	1.5	0