Zhongfeng Wang

List of Publications by Year
in descending order

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		430442	476904
174	1,556	18	29
papers	citations	h-index	g-index

174	174	174	1184
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	FTA-GAN: A Computation-Efficient Accelerator for GANs With Fast Transformation Algorithm. IEEE Transactions on Neural Networks and Learning Systems, 2023, 34, 2978-2992.	7.2	5
2	ETA: An Efficient Training Accelerator for DNNs Based on Hardware-Algorithm Co-Optimization. IEEE Transactions on Neural Networks and Learning Systems, 2023, 34, 7660-7674.	7.2	8
3	Efficient Software Implementation of the SIKE Protocol Using a New Data Representation. IEEE Transactions on Computers, 2022, 71, 670-683.	2.4	4
4	Rethinking Adaptive Computing: Building a Unified Model Complexity-Reduction Framework With Adversarial Robustness. IEEE Transactions on Neural Networks and Learning Systems, 2022, 33, 1803-1810.	7.2	1
5	Memory-Efficient CNN Accelerator Based on Interlayer Feature Map Compression. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 668-681.	3.5	11
6	An Area-Efficient Message Passing Detector for Massive MIMO Systems. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 1751-1764.	3.5	7
7	A Flexible and Efficient FPGA Accelerator for Various Large-Scale and Lightweight CNNs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 1185-1198.	3.5	22
8	High-Throughput LDPC-CC Decoders Based on Storage, Arithmetic, and Control Improvements. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 1069-1073.	2.2	1
9	RvDfi: A RISC-V Architecture With Security Enforcement by High Performance Complete Data-Flow Integrity. IEEE Transactions on Computers, 2022, 71, 2499-2512.	2.4	2
10	A Reliability Profile Based Low-Complexity Dynamic Schedule LDPC Decoding. IEEE Access, 2022, 10, 3390-3399.	2.6	1
11	FPGA-Accelerated Maze Routing Kernel for VLSI Designs. , 2022, , .		2
12	LDPC decoding with locally informed dynamic scheduling based on the law of large numbers. IET Communications, 2022, 16, 634-648.	1.5	1
13	An Efficient High-Throughput Structured-Light Depth Engine. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 1047-1058.	2.1	2
14	A low latency traffic sign detection model with an automatic data labeling pipeline. Neural Computing and Applications, 2022, 34, 15499-15512.	3.2	1
15	THETA: A High-Efficiency Training Accelerator for DNNs With Triple-Side Sparsity Exploration. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 1034-1046.	2.1	5
16	Hybrid Stochastic-Binary Computing for Low-Latency and High-Precision Inference of CNNs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 2707-2720.	3.5	6
17	PREFENDER: A Prefetching Defender against Cache Side Channel Attacks as A Pretender. , 2022, , .		1
18	An Efficient Reconfigurable Encoder for the IEEE 1901 Standard. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 1368-1372.	2.1	2

#	Article	IF	Citations
19	Iterative Hard Thresholding Algorithm-Based Detector for Compressed OFDM-IM Systems. IEEE Communications Letters, 2022, 26, 2205-2209.	2.5	1
20	Evaluations on Deep Neural Networks Training Using Posit Number System. IEEE Transactions on Computers, 2021, 70, 174-187.	2.4	30
21	Design of High-Performance and Area-Efficient Decoder for 5G LDPC Codes. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 879-891.	3.5	17
22	Lowâ€complexity sphere decoding for MIMOâ€SCMA systems. IET Communications, 2021, 15, 537-545.	1.5	2
23	Fast Modular Multipliers for Supersingular Isogeny-Based Post-Quantum Cryptography. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 359-371.	2.1	7
24	An Improved Reliability-Based Decoding Algorithm for NB-LDPC Codes. IEEE Communications Letters, 2021, 25, 1153-1157.	2.5	2
25	Accelerating 3D Convolutional Neural Networks Using 3D Fast Fourier Transform. , 2021, , .		4
26	A DNN Optimization Framework with Unlabeled Data for Efficient and Accurate Reconfigurable Hardware Inference. , 2021, , .		2
27	Low-Latency Architecture for the Parallel Extended GCD Algorithm of Large Numbers. , 2021, , .		1
28	Transform-Based Feature Map Compression for CNN Inference. , 2021, , .		10
29	High-Speed and Scalable FPGA Implementation of the Key Generation for the Leighton-Micali Signature Protocol. , 2021, , .		6
30	Flexible-width Bit-level Compressor for Convolutional Neural Network. , 2021, , .		2
31	Federated Regularization Learning: an Accurate and Safe Method for Federated Learning. , 2021, , .		8
32	Elbert: Fast Albert with Confidence-Window Based Early Exit. , 2021, , .		7
33	A Hidden DCT-Based Invisible Watermarking Method for Low-Cost Hardware Implementations. Electronics (Switzerland), 2021, 10, 1465.	1.8	3
34	An Efficient and Flexible Accelerator Design for Sparse Convolutional Neural Networks. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 2936-2949.	3.5	27
35	Low-Latency Hardware Accelerator for Improved Engle-Granger Cointegration in Pairs Trading. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 2911-2924.	3.5	5
36	Counter Random Gradient Descent Bit-Flipping Decoder for LDPC Codes. , 2021, , .		4

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37	PipeBSW: A Two-Stage Pipeline Structure for Banded Smith-Waterman Algorithm on FPGA. , 2021, , .		3
38	A Reconfigurable Accelerator for Generative Adversarial Network Training Based on FPGA. , 2021, , .		2
39	DARM: A Low-Complexity and Fast Modular Multiplier for Lattice-Based Cryptography. , 2021, , .		3
40	LITNet: A Light-weight Image Transform Net for Image Style Transfer. , 2021, , .		0
41	An FPGA-Based Reconfigurable Accelerator for Low-Bit DNN Training. , 2021, , .		3
42	High-Speed FPGA Implementation of SIKE Based on an Ultra-Low-Latency Modular Multiplier. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 3719-3731.	3.5	19
43	Generalized Analog-to-Information Converter With Analysis Sparse Prior. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 3574-3586.	3.5	5
44	An Improved Method for Performance Analysis of Generalized Integrated Interleaved Codes. IEEE Communications Letters, 2021, 25, 3166-3169.	2.5	2
45	Piecewise Parabolic Approximate Computation Based on an Error-Flattened Segmenter and a Novel Quantizer. Electronics (Switzerland), 2021, 10, 2704.	1.8	4
46	A Memory-Efficient Hardware Architecture for Deformable Convolutional Networks. , 2021, , .		4
47	A Stage-wise Conversion Strategy for Low-Latency Deformable Spiking CNN. , 2021, , .		0
48	Automatic Generation of Dynamic Inference Architecture for Deep Neural Networks. , 2021, , .		0
49	Reducing Search Complexity of Dynamic SC-Flip Decoding for Polar Codes. , 2021, , .		0
50	Optimized Trellis-Based Min-Max Decoder for NB-LDPC Codes. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 57-61.	2.2	9
51	A Novel Iterative Reliability-Based Majority-Logic Decoder for NB-LDPC Codes. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1399-1403.	2.2	3
52	GH CORDIC-Based Architecture for Computing N th Root of Single-Precision Floating-Point Number. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 864-875.	2.1	17
53	Exploring Quantization in Few-Shot Learning. , 2020, , .		1
54	Information Storage Bit-Flipping Decoder for LDPC Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2464-2468.	2.1	9

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55	F-DNA: Fast Convolution Architecture for Deconvolutional Network Acceleration. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1867-1880.	2.1	11
56	An Implementation of Pre-Quantized Random Demodulator Based on Amplitude-to-Pulse Converter. , 2020, , .		1
57	A Novel Modular Multiplier for Isogeny-Based Post-Quantum Cryptography. , 2020, , .		3
58	A Serial Maximum-likelihood Detection Algorithm for Massive MIMO Systems. , 2020, , .		1
59	Hardware Accelerator for Engle-Granger Cointegration in Pairs Trading. , 2020, , .		3
60	LSTM-Based Quantitative Trading Using Dynamic K-Top and Kelly Criterion. , 2020, , .		2
61	A Computation-Efficient Solution for Acceleration of Generative Adversarial Network. , 2020, , .		3
62	CLA Formula and its Acceleration of Architecture Design for Clustered Look-Ahead Pipelined Recursive Digital Filter. Journal of Signal Processing Systems, 2020, 93, 617.	1.4	0
63	A Precision-Scalable Energy-Efficient Convolutional Neural Network Accelerator. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3484-3497.	3.5	18
64	Fine-Grained Bit-Flipping Decoding for LDPC Codes. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 896-900.	2.2	10
65	A Novel Approximation Methodology and Its Efficient VLSI Implementation for the Sigmoid Function. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3422-3426.	2.2	16
66	Efficient Precision-Adjustable Architecture for Softmax Function in Deep Learning. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3382-3386.	2.2	29
67	Multi-Layer Generalized Integrated Interleaved Codes. IEEE Communications Letters, 2020, 24, 1880-1884.	2.5	4
68	Calibration of timing mismatch in TIADC based on monotonicity detecting of sampled data. IEICE Electronics Express, 2020, 17, 20190699-20190699.	0.3	4
69	A Universal Approximation Method and Optimized Hardware Architectures for Arithmetic Functions Based on Stochastic Computing. IEEE Access, 2020, 8, 46229-46241.	2.6	10
70	An Efficient FPGA Accelerator Optimized for High Throughput Sparse CNN Inference. , 2020, , .		9
71	Efficient FPGA design for Convolutions in CNN based on FFT-pruning. , 2020, , .		1
72	LBFP: Logarithmic Block Floating Point Arithmetic for Deep Neural Networks. , 2020, , .		4

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73	Fast Permutation Architecture on Encrypted Data for Secure Neural Network Inference. , 2020, , .		4
74	An Efficient Accelerator of the Squaring for the Verifiable Delay Function Over a Class Group. , 2020, , .		3
75	Optimizing stochastic computing for low latency inference of convolutional neural networks. , 2020, , .		2
76	A Configurable FPGA Accelerator of Bi-LSTM Inference with Structured Sparsity. , 2020, , .		3
77	A High-Speed Architecture for the Reduction in VDF Based on a Class Group. , 2020, , .		0
78	A Reconfigurable Permutation Based Address Encryption Architecture for Memory Security. , 2020, , .		0
79	Hardware Accelerator for Multi-Head Attention and Position-Wise Feed-Forward in the Transformer. , 2020, , .		35
80	Efficient Inference of Large-Scale and Lightweight Convolutional Neural Networks on FPGA. , 2020, , .		1
81	A Reconfigurable DNN Training Accelerator on FPGA. , 2020, , .		2
82	A High-Speed Successive-Cancellation Decoder for Polar Codes Using Approximate Computing. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 227-231.	2.2	6
83	FPAP: A Folded Architecture for Energy-Quality Scalable Convolutional Neural Networks. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 288-301.	3.5	10
84	A New Clock Phase Calibration Method in High-Speed and High-Resolution DACs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 332-336.	2.2	0
85	An Efficient Post-Processor for Lowering the Error Floor of LDPC Codes. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 397-401.	2.2	2
86	Background Calibration of Comparator Offsets in SHA-Less Pipelined ADCs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 357-361.	2.2	4
87	A New Probabilistic Gradient Descent Bit Flipping Decoder for LDPC Codes. , 2019, , .		4
88	Methodology for Efficient Reconfigurable Architecture of Generative Neural Network. , 2019, , .		7
89	TIE. , 2019, , .		38
90	A Novel Low-Complexity Joint Coding and Decoding Algorithm for NB-LDPC Codes. , 2019, , .		3

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91	A New Fast-SSC-Flip Decoding of Polar Codes. , 2019, , .		5
92	A Hardware-Oriented and Memory-Efficient Method for CTC Decoding. IEEE Access, 2019, 7, 120681-120694.	2.6	5
93	USCA: A Unified Systolic Convolution Array Architecture for Accelerating Sparse Neural Network. , 2019, , .		10
94	Efficient T-EMS Based Decoding Algorithms for High-Order LDPC Codes. IEEE Access, 2019, 7, 50980-50992.	2.6	6
95	Generalized Hyperbolic CORDIC and Its Logarithmic and Exponential Computation With Arbitrary Fixed Base. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2156-2169.	2.1	34
96	Improved Fast-SSC-Flip Decoding of Polar Codes. IEEE Communications Letters, 2019, 23, 950-953.	2.5	12
97	A Low-latency Sparse-Winograd Accelerator for Convolutional Neural Networks. , 2019, , .		20
98	Analysis and Design of a Large Dither Injection Circuit for Improving Linearity in Pipelined ADCs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2008-2020.	2.1	11
99	E-LSTM: An Efficient Hardware Architecture for Long Short-Term Memory. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 280-291.	2.7	41
100	A 124-Gb/s Decoder for Generalized Integrated Interleaved Codes. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3174-3187.	3.5	16
101	An Improved Gradient Descent Bit-Flipping Decoder for LDPC Codes. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3188-3200.	3.5	18
102	Improved Decoding Algorithms of LDPC Codes Based on Reliability Metrics of Variable Nodes. IEEE Access, 2019, 7, 35769-35778.	2.6	9
103	Modified GII-BCH Codes for Low-Complexity and Low-Latency Encoders. IEEE Communications Letters, 2019, 23, 785-788.	2.5	7
104	Improved Soft-Assisted Iterative Bounded Distance Decoding for Product Codes. , 2019, , .		1
105	Redundancy-Aided Iterative Reliability-Based Majority-Logic Decoding for NB-LDPC Codes. , 2019, , .		0
106	DynExit: A Dynamic Early-Exit Strategy for Deep Residual Networks. , 2019, , .		15
107	Ultra-Fast Modular Multiplication Implementation for Isogeny-Based Post-Quantum Cryptography. , 2019, , .		7
108	A 100 Gbps Turbo Product Code Decoder for Optical Communications. , 2019, , .		3

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109	Corrections to â€œGeneralized Hyperbolic CORDIC and Its Logarithmic and Exponential Computation With Arbitrary Fixed Baseâ€•[Sep 19 DOI: 10.1109/TVLSI.2019.2919557]. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2222-2222.	2.1	2
110	A Decomposition Mapping based Quantized Belief Propagation Decoding for 5G LDPC Codes. , 2019, , .		0
111	A New Inversionless Berlekamp-Massey Algorithm with Efficient Architecture. , 2019, , .		1
112	A Low-Latency and Low-Complexity Hardware Architecture for CTC Beam Search Decoding. , 2019, , .		1
113	An Enhanced Offset Min-Sum decoder for 5G LDPC Codes. , 2019, , .		0
114	EAGLE: Exploiting Essential Address in Both Weight and Activation to Accelerate CNN Computing. , 2019, , .		0
115	Training Deep Neural Networks Using Posit Number System. , 2019, , .		11
116	A Low-Complexity Error-and-Erasure Decoding Algorithm for t=2 RS Codes. , 2019, , .		3
117	Hybrid Preconditioned CG Detection with Sequential Update for Massive MIMO Systems. , 2019, , .		1
118	Hardware Implementation of Improved Fast-SSC-Flip Decoder for Polar Codes. , 2019, , .		9
119	A Low-Complexity RS Decoder for Triple-Error-Correcting RS Codes. , 2019, , .		2
120	Fast-ABC: A Fast Architecture for Bottleneck-Like Based Convolutional Neural Networks. , 2019, , .		10
121	An Improved Gauss-Seidel Algorithm and Its Efficient Architecture for Massive MIMO Systems. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1194-1198.	2.2	30
122	Efficient Hardware Architectures for Deep Convolutional Neural Network. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1941-1953.	3.5	106
123	Stuck-at-close defect propagation and its blocking technique in CMOL cell mapping. Microelectronics Journal, 2018, 72, 100-108.	1.1	5
124	Low Complexity Message Passing Detection Algorithm for Large-Scale MIMO Systems. IEEE Wireless Communications Letters, 2018, 7, 708-711.	3.2	32
125	Design of Binary LDPC Codes With Parallel Vector Message Passing. IEEE Transactions on Communications, 2018, 66, 1363-1375.	4.9	9
126	A Stage-Combined Belief Propagation Decoder for Polar Codes. Journal of Signal Processing Systems, 2018, 90, 687-694.	1.4	4

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127	A 21.66 Gbps Nonbinary LDPC Decoder for High-Speed Communications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 226-230.	2.2	8
128	An Energy-Efficient Architecture for Binary Weight Convolutional Neural Networks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 280-293.	2.1	54
129	A High-Speed and Low-Complexity Architecture for Softmax Function in Deep Learning. , 2018, , .		74
130	A Low-Complexity Decoder for Turbo Product Codes Based on Extended Hamming Codes. , 2018, , .		5
131	Comparison between Generalized Integrated Interleaved Codes and Generalized Error Location Codes. , 2018, , .		2
132	Efficient Reconfigurable Hardware Core for Convolutional Neural Networks. , 2018, , .		1
133	Fast and Low-Complexity Decoding Algorithm and Architecture for Quadruple-Error-Correcting RS codes. , 2018, , .		4
134	An Improved Variable-Node-Based BP Decoding Algorithm for NAND Flash Memory. , 2018, , .		2
135	Analysis of the Dual-Threshold-Based Shrinking Scheme for Efficient NB-LDPC Decoding. , 2018, , .		0
136	A Novel Hardware Architecture to Accelerate Burrows-Wheeler Transform. , 2018, , .		1
137	Approximate Comparator: Design and Analysis. , 2018, , .		6
138	Bandwidth Efficient Architectures for Convolutional Neural Network. , 2018, , .		0
139	A Novel Compiler for Regular Expression Matching Engine Construction. , 2018, , .		0
140	Increasing the Accuracy of Approximate Adders with Very Low Extra Complexity. , 2018, , .		0
141	Eadnet: Efficient Architecture for Decomposed Convolutional Neural Networks. , 2018, , .		0
142	An Efficient NB-LDPC Decoding Algorithm for Next-Generation Memories. , 2018, , .		2
143	A New Soft-input Hard-output decoding algorithm for Turbo Product Codes. , 2018, , .		1
144	Hardware-Oriented Compression of Long Short-Term Memory for Efficient Inference. IEEE Signal Processing Letters, 2018, 25, 984-988.	2.1	8

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145	An Efficient Convolution Core Architecture for Privacy-Preserving Deep Learning. , 2018, , .		11
146	FPAP: A Folded Architecture for Efficient Computing of Convolutional Neural Networks. , 2018, , .		2
147	An Optimized Architecture For Decomposed Convolutional Neural Networks. , 2018, , .		0
148	CORDIC-Based Architecture for Computing Nth Root and Its Implementation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 4183-4195.	3.5	27
149	Compressed Level Crossing Sampling for Ultra-Low Power IoT Devices. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2495-2507.	3.5	9
150	Fully-Parallel Area-Efficient Deep Neural Network Design Using Stochastic Computing. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1382-1386.	2.2	26
151	Low-complexity detection algorithms based on matrix partition for massive MIMO. , 2017, , .		4
152	Accelerating Recurrent Neural Networks: A Memory-Efficient Approach. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2763-2775.	2.1	68
153	Efficient Soft Cancelation Decoder Architectures for Polar Codes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 87-99.	2.1	11
154	High-Speed Parallel LFSR Architectures Based on Improved State-Space Transformations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1159-1163.	2.1	23
155	Energy efficient SVM classifier using approximate computing. , 2017, , .		6
156	Efficient approximate layered LDPC decoder. , 2017, , .		5
157	Advanced Baseband Processing Algorithms, Circuits, and Implementations for 5G Communication. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2017, 7, 477-490.	2.7	26
158	Guest Editorial Advanced Baseband Processing Circuits and Systems for 5G Communications. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2017, 7, 473-476.	2.7	0
159	Algorithm and architecture for joint detection and decoding for MIMO with LDPC codes. , 2017, , .		6
160	Reduced complexity message passing detection algorithm in large-scale MIMO systems. , 2017, , .		3
161	Reduced complexity list polar decoder with an improved path pruning scheme. , 2017, , .		0
162	A reduced complexity decoding algorithm for NB-LDPC codes. , 2017, , .		2

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163	Efficient fast convolution architectures for convolutional neural network. , 2017, , .		18
164	Segmented successive cancellation list polar decoding with joint BCH-CRC codes. , 2017, , .		2
165	An efficient post processing scheme to lower the error floor of LDPC decoders. , 2017, , .		1
166	Improved BP decoder for polar codes based on a modified kernel matrix. Electronics Letters, 2016, 52, 1982-1984.	0.5	5
167	Intra-layer nonuniform quantization of convolutional neural network. , 2016, , .		6
168	Beyond 100Gbps Encoder Design for Staircase Codes. , 2016, , .		2
169	An Efficient Hardware Architecture for Lossless Data Compression in Data Center. , 2016, , .		1
170	Efficient convolution architectures for convolutional neural network. , 2016, , .		22
171	Area-Efficient Scaling-Free DFT/FFT Design Using Stochastic Computing. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 1131-1135.	2.2	26
172	Area-efficient check node unit architecture for single block-row quasi-cyclic LDPC codes. , 2014, , .		2
173	A High-Throughput LDPC Decoder Architecture With Rate Compatibility. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 839-847.	3.5	29
174	High-Throughput Layered LDPC Decoding Architecture. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 582-587.	2.1	42