Fadi J Kurdahi

List of Publications by Year
in descending order

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149 papers	1,607 citations	471509 17 h-index	526287 27 g-index
150 all docs	150 docs citations	150 times ranked	1080 citing authors

#	Article	IF	Citations
1	The Self-Aware Information Processing Factory Paradigm for Mixed-Critical Multiprocessing. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 250-266.	4.6	4
2	CFFNN: Cross Feature Fusion Neural Network for Collaborative Filtering. IEEE Transactions on Knowledge and Data Engineering, 2022, 34, 4650-4662.	5.7	21
3	In-Memory Associative Processors: Tutorial, Potential, and Challenges. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2641-2647.	3.0	6
4	Predicting Failures in Embedded Systems Using Long Short-Term Inference. IEEE Embedded Systems Letters, 2021, 13, 85-89.	1.9	0
5	Design Exploration of Sensing Techniques in 2T-2R Resistive Ternary CAMs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 762-766.	3.0	9
6	Cost- and Dataset-free Stuck-at Fault Mitigation for ReRAM-based Deep Learning Accelerators. , 2021, , .		10
7	Textile-integrated metamaterials for near-field multibody area networks. Nature Electronics, 2021, 4, 808-817.	26.0	54
8	Are CNNs Reliable Enough for Critical Applications? An Exploratory Study. IEEE Design and Test, 2020, 37, 76-83.	1.2	31
9	Learning to Predict IR Drop with Effective Training for ReRAM-based Neural Network Hardware. , 2020, , .		25
10	On-Chip Error-Triggered Learning of Multi-Layer Memristive Spiking Neural Networks. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2020, 10, 522-535.	3.6	18
11	NEWERTRACK: ML-Based Accurate Tracking of In-Mouth Nutrient Sensors Position Using Spectrum-Wide Information. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 3833-3841.	2.7	6
12	Error-triggered Three-Factor Learning Dynamics for Crossbar Arrays. , 2020, , .		15
13	Biometric Identity Based on Intra-Body Communication Channel Characteristics and Machine Learning. Sensors, 2020, 20, 1421.	3.8	1
14	Spiking neural networks for inference and learning: a memristor-based design perspective. , 2020, , 499-530.		11
15	IR-QNN Framework: An IR Drop-Aware Offline Training of Quantized Crossbar Arrays. IEEE Access, 2020, 8, 228392-228408.	4.2	21
16	Power Performance Tradeoffs Using Adaptive Bit Width Adjustments on Resistive Associative Processors. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 302-312.	5.4	5
17	IBCFAP: Intra-Body Communications Five-Layers Arm Phantom Model. IEEE Access, 2019, 7, 93701-93710.	4.2	2
18	An Ultra-Area-Efficient 1024-Point In-Memory FFT Processor. Micromachines, 2019, 10, 509.	2.9	14

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19	Mask Technique for Fast and Efficient Training of Binary Resistive Crossbar Arrays. IEEE Nanotechnology Magazine, 2019, 18, 704-716.	2.0	31
20	Non-Stationary Polar Codes for Resistive Memories. , 2019, , .		7
21	The information processing factory. , 2019, , .		9
22	Independent Component Analysis Using RRAMs. IEEE Nanotechnology Magazine, 2019, 18, 611-615.	2.0	14
23	Efficient Tracing Methodology Using Automata Processor. Transactions on Embedded Computing Systems, 2019, 18, 1-18.	2.9	8
24	Sensitivity of Galvanic Intra-Body Communication Channel to System Parameters. Lecture Notes of the Institute for Computer Sciences, Social-Informatics and Telecommunications Engineering, 2019, , 150-160.	0.3	0
25	A Two-Dimensional Associative Processor. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1659-1670.	3.1	14
26	Rapid in-memory matrix multiplication using associative processor. , 2018, , .		6
27	Guest Editorial: Special Issue on Accelerated Computing. IEEE Transactions on Multi-Scale Computing Systems, 2018, 4, 1-2.	2.4	0
28	Modeling and Analysis of Passive Switching Crossbar Arrays. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 270-282.	5.4	55
29	Low-Power Resistive Associative Processor Implementation Through the Multi-Compare. , 2018, , .		2
30	Platform-Centric Self-Awareness as a Key Enabler for Controlling Changes in CPS. Proceedings of the IEEE, 2018, 106, 1543-1567.	21.3	20
31	Circuit Inspired Modeling Method for Irrigation. , 2018, , .		1
32	Design methodologies for enabling self-awareness in autonomous systems. , 2018, , .		8
33	A Hybrid Approximate Computing Approach for Associative In-Memory Processors. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 758-769.	3.6	20
34	Physical Multi-Layer Phantoms for Intra-Body Communications. IEEE Access, 2018, 6, 42812-42821.	4.2	11
35	Power optimization techniques for associative processors. Journal of Systems Architecture, 2018, 90, 44-53.	4.3	4
36	Minimal Disturbed Bits in Writing Resistive Crossbar Memories. , 2018, , .		1

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37	AS8â€static random access memory (SRAM): asymmetric SRAM architecture for soft error hardening enhancement. IET Circuits, Devices and Systems, 2017, 11, 89-94.	1.4	30
38	Reliability Enhancement of Low-Power Sequential Circuits Using Reconfigurable Pulsed Latches. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 1803-1814.	5.4	8
39	Approximate Memristive In-memory Computing. Transactions on Embedded Computing Systems, 2017, 16, 1-18.	2.9	18
40	Efficient pulsed-latch implementation for multiport register files. , 2017, , .		3
41	Low Latency Approximate Adder for Highly Correlated Input Streams. , 2017, , .		2
42	On one step row readout technique of selector-less resistive arrays. , 2017, , .		3
43	On the Optimum Data Carrier for Intra-body Communication Applications. , 2017, , .		4
44	Microarchitecture-Level SoC Design. , 2017, , 867-913.		0
45	Resource Aggregation for Collaborative Video from Multiple Projector enabled Mobile Devices. , 2016, , .		0
46	Process variations-aware resistive associative processor design. , 2016, , .		4
47	Rectangular stable power-aware mobile projection on planar surfaces. , 2016, , .		0
48	A System-Level Exploration of Power Delivery Architectures for Near-Threshold Manycores Considering Performance Constraints. , 2016, , .		2
49	Conquering MPSoC complexity with principles of a self-aware information processing factory. , 2016, , .		9
50	Lattice-based Boolean diagrams. , 2016, , .		0
51	Microarchitecture-Level SoC Design. , 2016, , 1-46.		0
52	DWT-based watermarking technique for video authentication. , 2015, , .		10
53	Intra-body communication model based on variable biological parameters. , 2015, , .		9
54	NUVA: Architectural support for runtime verification of parametric specifications over multicores. , 2015, , .		11

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55	Cooperative On-Chip Temperature EstimationUsing Multiple Virtual Sensors. IEEE Embedded Systems Letters, 2015, 7, 37-40.	1.9	5
56	Thermal sensor allocation for SoCs based on temperature gradients. , 2015, , .		6
57	State dependent statistical timing model for voltage scaled circuits. , 2014, , .		3
58	Algorithms and Architectures of Energy-Efficient Error-Resilient MIMO Detectors for Memory-Dominated Wireless Communication Systems. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 2159-2171.	5.4	11
59	Equi-Noise: A Statistical Model That Combines Embedded Memory Failures and Channel Noise. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 407-419.	5.4	8
60	Low power reduced-complexity error-resilient MIMO detector. , 2014, , .		0
61	Mobile Collaborative Video. IEEE Transactions on Circuits and Systems for Video Technology, 2014, 24, 1594-1604.	8.3	2
62	Joint Power Management and Adaptive Modulation and Coding for Wireless Communications Systems With Unreliable Buffering Memories. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 2456-2465.	5.4	4
63	Memristor Multiport Readout: A Closed-Form Solution for Sneak Paths. IEEE Nanotechnology Magazine, 2014, 13, 274-282.	2.0	73
64	Multicopy Cache. Transactions on Embedded Computing Systems, 2014, 13, 1-27.	2.9	3
65	A survey of cross-layer power-reliability tradeoffs in multi and many core systems-on-chip. Microprocessors and Microsystems, 2013, 37, 760-771.	2.8	6
66	Architectural support for runtime verification on ccNUMA multiprocessors. , 2013, , .		0
67	Vision-inspired global routing for enhanced performance and reliability. , 2013, , .		0
68	Error-aware power management for memory dominated OFDM systems. , 2013, , .		0
69	Heterogeneous memory management for 3D-DRAM and external DRAM with QoS. , 2013, , .		5
70	Low overhead correction scheme for unreliable LDPC buffering. , 2013, , .		3
71	Collaborative video playback on a federation of tiled mobile projectors enabled by visual feedback. , 2012, , .		2
72	Error-Aware Algorithm/Architecture Coexploration for Video Over Wireless Applications. Transactions on Embedded Computing Systems, 2012, 11S, 1-23.	2.9	4

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73	Reliable low power Distributed Arithmetic filters via N-Modular Redundancy. , 2012, , .		1
74	Fast error aware model for arithmetic and logic circuits. , 2012, , .		15
75	Parity-based mono-Copy Cache for low power consumption and high reliability. , 2012, , .		5
76	Error resilient MIMO detector for memory-dominated wireless communication systems. , 2012, , .		6
77	Variation Trained Drowsy Cache (VTD-Cache): A History Trained Variation Aware Drowsy Cache for Fine Grain Voltage Scaling. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 630-642.	3.1	7
78	Adjustable supply voltages and refresh cycle for process variations, temperature changes, and device degradation adaptation in 1T1C embedded DRAM. , 2011, , .		1
79	Camera-based video synchronization for a federation of mobile projectors. , 2011, , .		1
80	Reconfigurable filter implementation of a matched-filter based spectrum sensor for Cognitive Radio systems. , 2011, , .		7
81	A Multi-Granularity Power Modeling Methodology for Embedded Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 668-681.	3.1	31
82	Embedded Memories Fault-Tolerant Pre- and Post-Silicon Optimization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1916-1921.	3.1	8
83	On leakage power optimization in clock tree networks for ASICs and general-purpose processors. Sustainable Computing: Informatics and Systems, 2011, 1, 75-87.	2.2	4
84	Reliability-aware placement in SRAM-based FPGA for voltage scaling realization in the presence of process variations. , 2011, , .		4
85	Area, reconfiguration delay and reliability trade-offs in designing reliable multi-mode FIR filters. , 2011, , .		1
86	A Class of Low Power Error Compensation Iterative Decoders. , 2011, , .		13
87	Adjustable supply voltages and refresh cycle for process variations and temperature changing adaptation in DRAM to minimize power consumption. , 2011, , .		1
88	Inquisitive Defect Cache: A Means of Combating Manufacturing Induced Process Variation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1597-1609.	3.1	17
89	E < MC2. , 2010, , .		28
90	Effect of body biasing on embedded SRAM failure. , 2010, , .		1

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91	FFT processing through faulty memories in OFDM based systems. , 2010, , .		4
92	Placement-aware partial reconfiguration for a class of FIR-like structures. , 2010, , .		2
93	Multiple sleep modes leakage control in peripheral circuits of a all major SRAM-based processor units. , 2010, , .		0
94	A combined channel and hardware noise resilient Viterbi decoder. , 2010, , .		22
95	A Unified Hardware and Channel Noise Model for Communication Systems. , 2010, , .		17
96	CAPPS: A Framework for Powerâ€“Performance Tradeoffs in Bus-Matrix-Based On-Chip Communication Architecture Synthesis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 209-221.	3.1	9
97	Low-Power Multimedia System Design by Aggressive Voltage Scaling. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 852-856.	3.1	35
98	Evaluating Carbon Nanotube Global Interconnects for Chip Multiprocessor Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1376-1380.	3.1	13
99	Post-synthesis sleep transistor insertion for leakage power optimization in clock tree networks. , 2010, , .		2
100	Exploiting Architectural Similarities and Mode Sequencing in Joint Cost Optimization of Multi-mode FIR Filters. , 2010, , .		0
101	Process variation aware transcoding for low power H.264 decoding. , 2010, , .		4
102	TRAM: A tool for Temperature and Reliability Aware Memory Design. , 2009, , .		2
103	A Low Power JPEG2000 Encoder With Iterative and Fault Tolerant Error Concealment. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 827-837.	3.1	18
104	System-level PVT variation-aware power exploration of on-chip communication architectures. ACM Transactions on Design Automation of Electronic Systems, 2009, 14, 1-25.	2.6	3
105	Exploring Carbon Nanotube Bundle Global Interconnects for Chip Multiprocessor Applications. , 2009, , .		5
106	Size-Reconfiguration Delay Tradeoffs for a Class of DSP Blocks in Multi-mode Communication Systems. , 2009, , .		10
107	Dynamically reconfigurable on-chip communication architectures for multi use-case chip multiprocessor applications. , 2009, , .		5
108	On chip Communication-Architecture Based Thermal Management for SoCs. , 2009, , .		3

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109	A fault tolerant cache architecture for sub 500mV operation. , 2009, , .		25
110	Managing leakage power and reliability in hot chips using system floorplanning and SRAM design. , 2008, , .		2
111	Architectural and algorithm level fault tolerant techniques for low power high yield multimedia devices. , 2008, , .		1
112	Thermal Aware Global Routing of VLSI Chips for Enhanced Reliability. , 2008, , .		10
113	System level performance analysis of carbon nanotube global interconnects for emerging chip multiprocessors. , 2008, , .		6
114	A partial memory protection scheme for higher effective yield of embedded memory for video data. , 2008, , .		5
115	Incorporating PVT Variations in System-Level Power Exploration of On-Chip Communication Architectures. , 2008, , .		5
116	PTSMT: A Tool for Cross-Level Power, Performance, and Thermal Exploration of SMT Processors. , 2008, , .		0
117	Cross-layer co-exploration of exploiting error resilience for video over wireless applications. , 2008, , .		6
118	Methodology for multi-granularity embedded processor power model generation for an ESL design flow. , 2008, , .		7
119	Power Management for Cognitive Radio Platforms. , 2007, , .		13
120	LEAF: A System Level Leakage-Aware Floorplanner for SoCs. , 2007, , .		19
121	Fault Tolerant Approaches Targeting Ultra Low Power Communications System Design. IEEE Vehicular Technology Conference, 2007, , .	0.4	7
122	System level power estimation methodology with H.264 decoder prediction IP case study. , 2007, , .		10
123	STEFAL: A System Level Temperature- and Floorplan-Aware Leakage Power Estimator for SoCs. , 2007, , .		10
124	Error-Aware Design. , 2007, , .		8
125	Limits on voltage scaling for caches utilizing fault tolerant techniques. , 2007, , .		10
126	Exploiting Fault Tolerance Towards Power Efficient Wireless Multimedia Applications. , 2007, , .		5

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127	Cross Layer Error Exploitation for Aggressive Voltage Scaling. , 2007, , .		33
128	A scalable embedded JPEG 2000 architecture. Journal of Systems Architecture, 2007, 53, 524-538.	4.3	6
129	Reducing Off-Chip Memory Access via Stream-Conscious Tiling on Multimedia Applications. International Journal of Parallel Programming, 2007, 35, 63-98.	1.5	1
130	A hierarchical pipelining architecture and FPGA implementation for lifting-based 2-D DWT. Journal of Real-Time Image Processing, 2007, 2, 281-291.	3.5	3
131	A Coarse-Grain Dynamically Reconfigurable System and Compilation Framework. , 2007, , 181-215.		1
132	Floorplan driven leakage power aware IP-based SoC design space exploration. , 2006, , .		4
133	System-level power-performance trade-offs in bus matrix communication architecture synthesis. , 2006, , .		31
134	Compile-time area estimation for LUT-based FPGAs. ACM Transactions on Design Automation of Electronic Systems, 2006, 11, 104-122.	2.6	28
135	System Redundancy; A Means of Improving Process Variation Yield Degradation in Memory Arrays. , 2006, , .		8
136	Design and Analysis of Low Power Image Filters Toward Defect-Resilient Embedded Memories for Multimedia SoCs. Lecture Notes in Computer Science, 2006, , 295-308.	1.3	4
137	Improving effective yield through error tolerant system design. , 2005, , .		11
138	Automatic compilation to a coarse-grained reconfigurable system-opn-chip. Transactions on Embedded Computing Systems, 2003, 2, 560-589.	2.9	27
139	A case study of mapping a software-defined radio (SDR) application on a reconfigurable DSP core. , 2003, , .		6
140	Kernel scheduling techniques for efficient solution space exploration in reconfigurable computing. Journal of Systems Architecture, 2001, 47, 277-292.	4.3	8
141	A compiler framework for mapping applications to a coarse-grained reconfigurable computer architecture. , 2001, , .		50
142	A data scheduler for multi-context reconfigurable architectures. , 2001, , .		2
143	Design and Implementation of the MorphoSys Reconfigurable Computing Processor. Journal of Signal Processing Systems, 2000, 24, 147-164.	1.0	82
144	MorphoSys. , 2000, , .		59

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145	System-level Time-stationary Control Synthesis for Pipelined Data Paths. VLSI Design, 1999, 9, 159-180.	0.5	0
146	MorphoSys: a reconfigurable processor targeted to high performance image application. Lecture Notes in Computer Science, 1999, , 661-669.	1.3	2
147	Kernel scheduling in reconfigurable computing. , 1999, , .		28
148	The MorphoSys Parallel Reconfigurable System. Lecture Notes in Computer Science, 1999, , 727-734.	1.3	35
149	Register-Transfer Synthesis of Pipelined Data Paths. VLSI Design, 1994, 2, 17-32.	0.5	1