Jacques-Olivier Klein

List of Publications by Year
in descending order

153	4,870	94433 37	110387 64
papers	citations	h-index	g-index

156	156	156	2826
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Spin-Transfer Torque Magnetic Memory as a Stochastic Memristive Synapse for Neuromorphic Systems. IEEE Transactions on Biomedical Circuits and Systems, 2015, 9, 166-174.	4.0	332
2	Compact Modeling of Perpendicular-Anisotropy CoFeB/MgO Magnetic Tunnel Junctions. IEEE Transactions on Electron Devices, 2012, 59, 819-826.	3.0	330
3	Failure and reliability analysis of STT-MRAM. Microelectronics Reliability, 2012, 52, 1848-1852.	1.7	192
4	Perpendicular-anisotropy magnetic tunnel junction switched by spin-Hall-assisted spin-transfer torque. Journal Physics D: Applied Physics, 2015, 48, 065001.	2.8	176
5	Reconfigurable Codesign of STT-MRAM Under Process Variations in Deeply Scaled Technology. IEEE Transactions on Electron Devices, 2015, 62, 1769-1777.	3.0	135
6	Compact Model of Dielectric Breakdown in Spin-Transfer Torque Magnetic Tunnel Junction. IEEE Transactions on Electron Devices, 2016, 63, 1762-1767.	3.0	132
7	Low Power Magnetic Full-Adder Based on Spin Transfer Torque MRAM. IEEE Transactions on Magnetics, 2013, 49, 4982-4987.	2.1	126
8	Perpendicular-magnetic-anisotropy CoFeB racetrack memory. Journal of Applied Physics, 2012, 111, .	2.5	111
9	Design considerations and strategies for high-reliable STT-MRAM. Microelectronics Reliability, 2011, 51, 1454-1458.	1.7	99
10	Synchronous Non-Volatile Logic Gate Design Based on Resistive Switching Memories. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 443-454.	5.4	90
11	Compact model of magnetic tunnel junction with stochastic spin transfer torque switching for reliability analyses. Microelectronics Reliability, 2014, 54, 1774-1778.	1.7	89
12	A High-Reliability, Low-Power Magnetic Full Adder. IEEE Transactions on Magnetics, 2011, 47, 4611-4616.	2.1	84
13	All Spin Artificial Neural Networks Based on Compound Spintronic Synapse and Neuron. IEEE Transactions on Biomedical Circuits and Systems, 2016, 10, 828-836.	4.0	84
14	Spintronics. ACM Journal on Emerging Technologies in Computing Systems, 2015, 12, 1-42.	2.3	83
15	Analytical Macrospin Modeling of the Stochastic Switching Time of Spin-Transfer Torque Devices. IEEE Transactions on Electron Devices, 2015, 62, 164-170.	3.0	82
16	Ultra Low Power Magnetic Flip-Flop Based on Checkpointing/Power Gating and Self-Enable Mechanisms. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 1755-1765.	5.4	79
17	Compact Model of Subvolume MTJ and Its Design Application at Nanoscale Technology Nodes. IEEE Transactions on Electron Devices, 2015, 62, 2048-2055.	3.0	78
18	Electrical Modeling of Stochastic Spin Transfer Torque Writing in Magnetic Tunnel Junctions for Memory and Logic Applications. IEEE Transactions on Magnetics, 2013, 49, 4375-4378.	2.1	74

#	Article	IF	Citations
19	Magnetic Adder Based on Racetrack Memory. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 1469-1477.	5.4	74
20	Proposal of Toggle Spin Torques Magnetic RAM for Ultrafast Computing. IEEE Electron Device Letters, 2019, 40, 726-729.	3.9	74
21	Failure Analysis in Magnetic Tunnel Junction Nanopillar with Interfacial Perpendicular Magnetic Anisotropy. Materials, 2016, 9, 41.	2.9	72
22	Self-Enabled â€œError-Freeâ€•Switching Circuit for Spin Transfer Torque MRAM and Logic. IEEE Transactions on Magnetics, 2012, 48, 2403-2406.	2.1	71
23	Robust neural logic block (NLB) based on memristor crossbar array. , 2011, , .		62
24	A radiation hardened hybrid spintronic/CMOS nonvolatile unit using magnetic tunnel junctions. Journal Physics D: Applied Physics, 2014, 47, 405003.	2.8	60
25	Yield and Reliability Improvement Techniques for Emerging Nonvolatile STT-MRAM. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2015, 5, 28-39.	3.6	57
26	Domain Wall Shift Register-Based Reconfigurable Logic. IEEE Transactions on Magnetics, 2011, 47, 2966-2969.	2.1	54
27	Variation-Tolerant and Disturbance-Free Sensing Circuit for Deep Nanometer STT-MRAM. IEEE Nanotechnology Magazine, 2014, 13, 1088-1092.	2.0	52
28	Compact Modeling of Perpendicular-Magnetic-Anisotropy Double-Barrier Magnetic Tunnel Junction With Enhanced Thermal Stability Recording Structure. IEEE Transactions on Electron Devices, 2019, 66, 2431-2436.	3.0	51
29	Digital Biologically Plausible Implementation of Binarized Neural Networks With Differential Hafnium Oxide Resistive Memory Arrays. Frontiers in Neuroscience, 2019, 13, 1383.	2.8	51
30	Dynamic compact model of Spin-Transfer Torque based Magnetic Tunnel Junction (MTJ). , 2009, , .		50
31	Synchronous 8-bit Non-Volatile Full-Adder based on Spin Transfer Torque Magnetic Tunnel Junction. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 1757-1765.	5.4	50
32	High reliability sensing circuit for deep submicron spin transfer torque magnetic random access memory. Electronics Letters, 2013, 49, 1283-1285.	1.0	49
33	Hardening Techniques for MRAM-Based Nonvolatile Latches and Logic. IEEE Transactions on Nuclear Science, 2012, 59, 1136-1141.	2.0	47
34	Physical Realization of a Supervised Learning System Built with Organic Memristive Synapses. Scientific Reports, 2016, 6, 31932.	3.3	47
35	A low-cost built-in error correction circuit design for STT-MRAM reliability improvement. Microelectronics Reliability, 2013, 53, 1224-1229.	1.7	43
36	Ultra-High Density Content Addressable Memory Based on Current Induced Domain Wall Motion in Magnetic Track. IEEE Transactions on Magnetics, 2012, 48, 3219-3222.	2.1	41

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37	Ultrahigh Density Memristor Neural Crossbar for On-Chip Supervised Learning. IEEE Nanotechnology Magazine, 2015, 14, 954-962.	2.0	40
38	Spintronic logic design methodology based on spin Hall effectâ€“driven magnetic tunnel junctions. Journal Physics D: Applied Physics, 2016, 49, 065008.	2.8	40
39	Spin-transfer torque magnetic memory as a stochastic memristive synapse. , 2014, , .		39
40	Current-limiting challenges for all-spin logic devices. Scientific Reports, 2015, 5, 14905.	3.3	39
41	Gate-Driven Pure Spin Current in Graphene. Physical Review Applied, 2017, 8, .	3.8	39
42	A compact model for magnetic tunnel junction (MTJ) switched by thermally assisted Spin transfer torque (TAS + STT). Nanoscale Research Letters, 2011, 6, 368.	5.7	37
43	Neuromorphic function learning with carbon nanotube based synapses. Nanotechnology, 2013, 24, 384013.	2.6	37
44	Compact thermal modeling of spin transfer torque magnetic tunnel junction. Microelectronics Reliability, 2015, 55, 1649-1653.	1.7	37
45	Cross-Point Architecture for Spin-Transfer Torque Magnetic Random Access Memory. IEEE Nanotechnology Magazine, 2012, 11, 907-917.	2.0	35
46	Magnetic nonâ€volatile flipâ€flop with spinâ€Hall assistance. Physica Status Solidi - Rapid Research Letters, 2015, 9, 375-378.	2.4	33
47	Compact modelling of ferroelectric tunnel memristor and its use for neuromorphic simulation. Applied Physics Letters, 2014, 104, 053505.	3.3	32
48	Ultra-Dense Ring-Shaped Racetrack Memory Cache Design. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 215-225.	5.4	31
49	Proposal for a graphene-based all-spin logic gate. Applied Physics Letters, 2015, 106, .	3.3	30
50	Low power, high reliability magnetic flip-flop. Electronics Letters, 2010, 46, 1493.	1.0	29
51	A compact model of domain wall propagation for logic and memory design. Journal of Applied Physics, 2011, 109, .	2.5	29
52	Design Optimization and Analysis of Multicontext STT-MTJ/CMOS Logic Circuits. IEEE Nanotechnology Magazine, 2015, 14, 169-177.	2.0	29
53	High-Frequency Low-Power Magnetic Full-Adder Based on Magnetic Tunnel Junction With Spin-Hall Assistance. IEEE Transactions on Magnetics, 2015, 51, 1-4.	2.1	28
54	A DSP-like analogue processing unit for smart image sensors. International Journal of Circuit Theory and Applications, 2002, 30, 595-609.	2.0	27

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55	Nanodevice-based novel computing paradigms and the neuromorphic approach. , 2012, , .		27
56	Stochastic Computing for Hardware Implementation of Binarized Neural Networks. IEEE Access, 2019, 7, 76394-76403.	4.2	26
57	Design of MRAM based logic circuits and its applications. , 2011, , .		24
58	A physics-based compact model of ferroelectric tunnel junction for memory and logic design. Journal Physics D: Applied Physics, 2014, 47, 045001.	2.8	24
59	Robust learning approach for neuro-inspired nanoscale crossbar architecture. ACM Journal on Emerging Technologies in Computing Systems, 2014, 10, 1-20.	2.3	24
60	Separated Precharge Sensing Amplifier for Deep Submicrometer MTJ/CMOS Hybrid Logic Circuits. IEEE Transactions on Magnetics, 2014, 50, 1-5.	2.1	22
61	Design and Analysis of Radiation Hardened Sensing Circuits for Spin Transfer Torque Magnetic Memory and Logic. IEEE Transactions on Nuclear Science, 2014, 61, 3258-3264.	2.0	20
62	Nonvolatile Boolean Logic Block Based on Ferroelectric Tunnel Memristor. IEEE Transactions on Magnetics, 2014, 50, 1-4.	2.1	20
63	Robust magnetic full-adder with voltage sensing 2T/2MTJ cell. , 2015, , .		19
64	Reliability-Enhanced Separated Pre-Charge Sensing Amplifier for Hybrid CMOS/MTJ Logic Circuits. IEEE Transactions on Magnetics, 2017, 53, 1-5.	2.1	19
65	Domain wall motion based magnetic adder. Electronics Letters, 2012, 48, 1049-1051.	1.0	18
66	Spintronic Devices as Key Elements for Energy-Efficient Neuroinspired Architectures. , 2015, , .		18
67	Perspectives of Racetrack Memory for Large-Capacity On-Chip Memory: From Device to System. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 629-638.	5.4	18
68	Reliability-Enhanced Hybrid CMOS/MTJ Logic Circuit Architecture. IEEE Transactions on Magnetics, 2017, 53, 1-5.	2.1	18
69	An overview of spin-based integrated circuits. , 2014, , .		17
70	Multi-level cell Spin Transfer Torque MRAM based on stochastic switching. , 2013, , .		16
71	Spintronics for low-power computing. , 2014, , .		16
72	Ferroelectric tunnel memristor-based neuromorphic network with 1T1R crossbar architecture. , 2014, , .		16

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73	Magnetic domain-wall racetrack memory for high density and fast data storage. , 2012, , .		15
74	Current induced perpendicular-magnetic-anisotropy racetrack memory with magnetic field assistance. Applied Physics Letters, 2014, 104, .	3.3	15
75	DFSTT-MRAM: Dual Functional STT-MRAM Cell Structure for Reliability Enhancement and 3-D MLC Functionality. IEEE Transactions on Magnetics, 2014, 50, 1-7.	2.1	14
76	Design and analysis of crossbar architecture based on complementary resistive switching non-volatile memory cells. Journal of Parallel and Distributed Computing, 2014, 74, 2484-2496.	4.1	14
77	High-Speed, Low-Power, and Error-Free Asynchronous Write Circuit for STT-MRAM and Logic. IEEE Transactions on Magnetics, 2016, 52, 1-4.	2.1	14
78	Partial spin absorption induced magnetization switching and its voltage-assisted improvement in an asymmetrical all spin logic device at the mesoscopic scale. Applied Physics Letters, 2017, 111, .	3.3	14
79	Image Processing Vision Systems: Standard Image Sensors Versus Retinas. IEEE Transactions on Instrumentation and Measurement, 2007, 56, 1675-1687.	4.7	13
80	Design and Modeling of a Neuro-Inspired Learning Circuit Using Nanotube-Based Memory Devices. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 2172-2181.	5.4	12
81	Full-adder circuit design based on all-spin logic device. , 2015, , .		12
82	Supervised learning with organic memristor devices and prospects for neural crossbar arrays. , 2015, , .		12
83	Spatio-temporal learning with arrays of analog nanosynapses. , 2017, , .		12
84	High Performance SoC Design Using Magnetic Logic and Memory. International Federation for Information Processing, 2012, , 10-33.	0.4	12
85	Write operation study of Co/BTO/LSMO ferroelectric tunnel junction. Journal of Applied Physics, 2013, 114, 044108.	2.5	11
86	Racetrack memory based reconfigurable computing. , 2013, , .		11
87	Read disturbance issue and design techniques for nanoscale STT-MRAM. Journal of Systems Architecture, 2016, 71, 2-11.	4.3	11
88	Modeling for Spin-FET and Design of Spin-FET-Based Logic Gates. IEEE Transactions on Magnetics, 2017, 53, 1-6.	2.1	11
89	Variation-Tolerant High-Reliability Sensing Scheme for Deep Submicrometer STT-MRAM. IEEE Transactions on Magnetics, 2014, 50, 1-4.	2.1	10
90	Peristaltic perpendicular-magnetic-anisotropy racetrack memory based on chiral domain wall motions. Journal Physics D: Applied Physics, 2015, 48, 105001.	2.8	10

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91	Implementing Binarized Neural Networks with Magnetoresistive RAM without Error Correction. , 2019, , .		10
92	Design and electrical simulation of on-chip neural learning based on nanocomponents. Electronics Letters, 2008, 44, 575.	1.0	9
93	MRAM crossbar based configurable logic block. , 2012, , .		9
94	High Density Spin-Transfer Torque (STT)-MRAM Based on Cross-Point Architecture. , 2012, , .		9
95	Electro-grafted organic memristors: Properties and prospects for artificial neural networks based on STDP. , 2014, , .		9
96	Read disturbance issue for nanoscale STT-MRAM. , 2015, , .		9
97	A process-variation-resilient methodology of circuit design by using asymmetrical forward body bias in 28nm FDSOI. Microelectronics Reliability, 2016, 64, 26-30.	1.7	9
98	A Smart Sensor for Image Processing: Towards a System on Chip. , 2006, , .		8
99	Design of TAS-MRAM prototype for NV embedded memory applications. , 2010, , .		8
100	Design study of efficient digital order-based STDP neuron implementations for extracting temporal features. , 2013, , .		8
101	On-Chip Universal Supervised Learning Methods for Neuro-Inspired Block of Memristive Nanodevices. ACM Journal on Emerging Technologies in Computing Systems, 2015, 11, 1-20.	2.3	8
102	Contrasting Advantages of Learning With Random Weights and Backpropagation in Non-Volatile Memory Neural Networks. IEEE Access, 2019, 7, 73938-73953.	4.2	8
103	Hight fault tolerance in neural crossbar. , 2010, , .		6
104	Spin-electronics based logic fabrics. , 2013, , .		6
105	On-chip supervised learning rule for ultra high density neural crossbar using memristor for synapse and neuron. , 2014, , .		6
106	On-chip supervised learning rule for ultra high density neural crossbar using memristor for synapse and neuron. , 2014, , .		6
107	Perspectives of racetrack memory based on current-induced domain wall motion: From device to system. , 2015, , .		6
108	Arithmetic Logic Unit based on all-spin logic devices. , 2017, , .		6

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109	Multiscaled Simulation Methodology for Neuro-Inspired Circuits Demonstrated with an Organic Memristor. IEEE Transactions on Multi-Scale Computing Systems, 2018, 4, 822-832.	2.4	6
110	Ultrafast and Energy-Efficient Ferrimagnetic XNOR Logic Gates for Binary Neural Networks. IEEE Electron Device Letters, 2021, 42, 621-624.	3.9	6
111	Improved ARAM for PARIS, an original programmable vision chip. , 0, , .		5
112	VHDL Simulation of Magnetic Domain Wall Logic. IEEE Transactions on Magnetics, 2006, 42, 2754-2756.	2.1	5
113	SPINTRONIC MEMORY-BASED RECONFIGURABLE COMPUTING. Spin, 2013, 03, 1340010.	1.3	5
114	A novel SEU-tolerant MRAM latch circuit based on C-element. , 2014, , .		5
115	Sneak paths effects in CBRAM memristive devices arrays for spiking neural networks. , 2014, , .		5
116	Spintronics for low-power computing. , 2014, , .		5
117	Implementation of magnetic field assistance to current-induced perpendicular-magnetic-anisotropy racetrack memory. Journal of Applied Physics, 2014, 115, 17D509.	2.5	5
118	Exploiting the short-term to long-term plasticity transition in memristive nanodevice learning architectures. , 2016, , .		5
119	Efficient Magnetic Domain Nucleation and Domain Wall Motion With Voltage Control Magnetic Anisotropy Effect and Antiferromagnetic/Ferromagnetic Coupling. IEEE Transactions on Magnetics, 2019, 55, 1-4.	2.1	5
120	In-Memory Resistive RAM Implementation of Binarized Neural Networks for Medical Applications. , 2020, , .		5
121	Implementation of Ternary Weights With Resistive RAM Using a Single Sense Operation Per Synapse. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 138-147.	5.4	5
122	Chip-in-the-loop learning algorithm for Boltzmann machine. Electronics Letters, 1995, 31, 986-988.	1.0	4
123	A smart sensor-based vision system: implementation and evaluation. Journal Physics D: Applied Physics, 2006, 39, 1694-1705.	2.8	4
124	Synthesis methodology for magnetic domain wall logic. International Journal of Electronics, 2008, 95, 249-263.	1.4	4
125	Design of embedded MRAM macros for memory-in-logic applications. , 2010, , .		4
126	High Tunnel Magnetoresistance in Mo/CoFe/MgO Magnetic Tunnel Junction: A First-Principles Study. IEEE Transactions on Magnetics, 2017, 53, 1-4.	2.1	4

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127	Proposal for Multi-Gate Spin Field-Effect Transistor. IEEE Transactions on Magnetics, 2018, 54, 1-5.	2.1	4
128	Magnetic Look-Up Table (MLUT) Featuring Radiation Hardness, High Performance and Low Power. Lecture Notes in Computer Science, 2011, , 275-280.	1.3	4
129	Time comparison in image processing: APS sensors versus an artificial retina based vision system. Measurement Science and Technology, 2007, 18, 2817-2826.	2.6	3
130	Synthesis of Finite State Machines with Magnetic Domain Wall Logic. , 2007, , .		3
131	Electrical simulation of learning stage in OG-CNTFET based neural crossbar. , 2010, , .		3
132	Low power magnetic flip-flop based on checkpointing and self-enable mechanism. , 2013, , .		3
133	Synchronous full-adder based on complementary resistive switching memory cells. , 2013, , .		3
134	Sneak paths effects in CBRAM memristive devices arrays for spiking neural networks. , 2014, , .		3
135	One-step majority-logic-decodable codes enable STT-MRAM for high speed working memories. , 2014, , .		3
136	Current-Induced Magnetic Switching for High-Performance Computing. , 2015, , 1-51.		3
137	Vortex-based spin transfer oscillator compact model for IC design. , 2015, , .		3
138	Model of the Weak Reset Process in HfO_x Resistive Memory for Deep Learning Frameworks. IEEE Transactions on Electron Devices, 2021, 68, 4925-4932.	3.0	3
139	A dynamic reference scheme to improve the sensing reliability of magnetic random access memory. , 2014, , .		2
140	A comprehensive compact model for the design of all-spin-logic based circuits. Microelectronics Journal, 2019, 92, 104442.	2.0	2
141	Architecture of neural synaptic array, design and simulation. , 2007, , .		1
142	Emerging hybrid logic circuits based on non-volatile magnetic memories. , 2013, , .		1
143	Monte-Carlo Simulations of Magnetic Tunnel Junctions: From physics to application. , 2014, , .		1
144	Approximate programming of magnetic memory elements for energy saving. , 2015, , .		1

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145	Channel Modeling and Reliability Enhancement Design Techniques for STT-MRAM. , 2015, , .		1
146	Embracing the Unreliability of Memory Devices for Neuromorphic Computing. , 2020, , .		1
147	Mixed analog-digital design of a learning nano-circuit for neuronal architectures. , 2008, , .		0
148	Compact modelling for Co/BTO/LSMO Ferroelectric Tunnel Junction. , 2013, , .		0
149	Spin transfer torque memories and logic gates. , 2014, , .		0
150	A recurrent crossbar of memristive nanodevices implements online novelty detection. , 2016, , .		0
151	Offset Analysis and Design Optimization of a Dynamic Sense Amplifier for Resistive Memories. , 2017, , .		0
152	Large scale, high density integration of all spin logic. , 2018, , .		0
153	Memory-Centric Neuromorphic Computing With Nanodevices. , 2019, , .		0