Nobuyuki Yoshikawa

List of Publications by Year
in descending order

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322	4,401	172457	189892
papers	citations	29 h-index	50 g-index

325	325	325	852
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	An adiabatic quantum flux parametron as an ultra-low-power logic device. Superconductor Science and Technology, 2013, 26, 035010.	3.5	266
2	Nb 9-Layer Fabrication Process for Superconducting Large-Scale SFQ Circuits and Its Process Evaluation. IEICE Transactions on Electronics, 2014, E97.C, 132-140.	0.6	132
3	Adiabatic quantum-flux-parametron cell library designed using a 10 kA cm^{â^'2}niobium fabrication process. Superconductor Science and Technology, 2017, 30, 035002.	3.5	97
4	Dynamic Characteristics of Inverter Circuits Using Single Electron Transistors. Japanese Journal of Applied Physics, 1995, 34, 1332-1338.	1.5	93
5	Adiabatic quantum-flux-parametron cell library adopting minimalist design. Journal of Applied Physics, 2015, 117, .	2.5	90
6	Design and Implementation of a Pipelined Bit-Serial SFQ Microprocessor, ${m CORE}1eta$. IEEE Transactions on Applied Superconductivity, 2007, 17, 474-477.	1.7	87
7	Bit-Serial Single Flux Quantum Microprocessor CORE. IEICE Transactions on Electronics, 2008, E91-C, 342-349.	0.6	83
8	100 GHz Demonstrations Based on the Single-Flux-Quantum Cell Library for the 10 kA/cm2 Nb Multi-Layer Process. IEICE Transactions on Electronics, 2010, E93-C, 440-444.	0.6	68
9	Measurement of 10 zJ energy dissipation of adiabatic quantum-flux-parametron logic using a superconducting resonator. Applied Physics Letters, 2013, 102, .	3.3	65
10	Reduction of power consumption of RSFQ circuits by inductance-load biasing. Superconductor Science and Technology, 1999, 12, 918-920.	3.5	64
11	Superconducting digital electronics. Proceedings of the IEEE, 2004, 92, 1549-1563.	21.3	64
12	New Nb multi-layer fabrication process for large-scale SFQ circuits. Physica C: Superconductivity and Its Applications, 2009, 469, 1578-1584.	1.2	64
13	Demonstration of a Single-Flux-Quantum Microprocessor Using Passive Transmission Lines. IEEE Transactions on Applied Superconductivity, 2005, 15, 400-404.	1.7	62
14	Margin and Energy Dissipation of Adiabatic Quantum-Flux-Parametron Logic at Finite Temperature. IEEE Transactions on Applied Superconductivity, 2013, 23, 1700304-1700304.	1.7	58
15	Reversible logic gate using adiabatic superconducting devices. Scientific Reports, 2014, 4, 6354.	3.3	58
16	Energy efficiency of adiabatic superconductor logic. Superconductor Science and Technology, 2015, 28, 015003.	3.5	54
17	Study of LR-Loading Technique for Low-Power Single Flux Quantum Circuits. IEEE Transactions on Applied Superconductivity, 2007, 17, 150-153.	1.7	50
18	ColdFlux Superconducting EDA and TCAD Tools Project: Overview and Progress. IEEE Transactions on Applied Superconductivity, 2019, 29, 1-7.	1.7	50

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19	MANA: A Monolithic Adiabatic iNtegration Architecture Microprocessor Using 1.4-zJ/op Unshunted Superconductor Josephson Junction Devices. IEEE Journal of Solid-State Circuits, 2021, 56, 1152-1165.	5.4	49
20	An adiabatic superconductor 8-bit adder with 24kBT energy dissipation per junction. Applied Physics Letters, 2019, 114, .	3.3	47
21	Timing jitter measurement of single-flux-quantum pulse in Josephson transmission line. Applied Physics Letters, 2004, 84, 2133-2135.	3.3	45
22	Simulation of sub-kBT bit-energy operation of adiabatic quantum-flux-parametron logic with low bit-error-rate. Applied Physics Letters, 2013, 103, .	3.3	38
23	Characterization of 4 K CMOS Devices and Circuits for Hybrid Josephson-CMOS Systems. IEEE Transactions on Applied Superconductivity, 2005, 15, 267-271.	1.7	37
24	Proposal of a Desk-Side Supercomputer with Reconfigurable Data-Paths Using Rapid Single-Flux-Quantum Circuits. IEICE Transactions on Electronics, 2008, E91-C, 350-355.	0.6	37
25	Data-driven self-timed RSFQ high-speed test system. IEEE Transactions on Applied Superconductivity, 1997, 7, 3830-3833.	1.7	32
26	Pseudo Sigmoid Function Generator for a Superconductive Neural Network. IEEE Transactions on Applied Superconductivity, 2013, 23, 1701004-1701004.	1.7	31
27	Simulation and Experimental Demonstration of Logic Circuits Using an Ultra-Low-Power Adiabatic Quantum-Flux-Parametron. IEEE Transactions on Applied Superconductivity, 2013, 23, 1301105-1301105.	1.7	31
28	Possibility of Kosterlitz-Thouless effect at the resistive transition of high Tc oxide superconductors. Physics Letters, Section A: General, Atomic and Solid State Physics, 1987, 125, 429-431.	2.1	30
29	Design of a pipelined 8-bit-serial single-flux-quantum microprocessor with multiple ALUs. Superconductor Science and Technology, 2006, 19, S344-S349.	3.5	30
30	Demonstration of 30 Gbit/s Generation of Superconductive True Random Number Generator. IEEE Transactions on Applied Superconductivity, 2011, 21, 843-846.	1.7	30
31	Large-Scale Integrated Circuit Design Based on a Nb Nine-Layer Structure for Reconfigurable Data-Path Processors. IEICE Transactions on Electronics, 2014, E97.C, 157-165.	0.6	29
32	Thermodynamic Study of Energy Dissipation in Adiabatic Superconductor Logic. Physical Review Applied, 2015, 4, .	3.8	29
33	Top-down RSFQ logic design based on a binary decision diagram. IEEE Transactions on Applied Superconductivity, 2001, 11, 1098-1101.	1.7	28
34	Design and component test of a tiny processor based on the SFQ technology. IEEE Transactions on Applied Superconductivity, 2003, 13, 441-445.	1.7	28
35	Design and Implementation of a Fully Asynchronous SFQ Microprocessor: SCRAM2. IEEE Transactions on Applied Superconductivity, 2007, 17, 478-481.	1.7	28
36	Design and implementation of a pipelined 8 bit-serial single-flux-quantum microprocessor with cache memories. Superconductor Science and Technology, 2007, 20, S305-S309.	3.5	28

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37	Implementation and Experimental Evaluation of a Cryocooled System Prototype for High-Throughput SFQ Digital Applications. IEEE Transactions on Applied Superconductivity, 2007, 17, 546-551.	1.7	28
38	Majority-Logic-Optimized Parallel Prefix Carry Look-Ahead Adder Families Using Adiabatic Quantum-Flux-Parametron Logic. IEEE Transactions on Applied Superconductivity, 2017, 27, 1-7.	1.7	28
39	Fully Functional Operation of Low-Power 64-kb Josephson-CMOS Hybrid Memories. IEEE Transactions on Applied Superconductivity, 2017, 27, 1-7.	1.7	27
40	Adiabatic Quantum-Flux-Parametron: Towards Building Extremely Energy-Efficient Circuits and Systems. Scientific Reports, 2019, 9, 10514.	3.3	27
41	A stochastic-computing based deep learning framework using adiabatic quantum-flux-parametron superconducting technology. , 2019, , .		27
42	Advanced Direct Synthesis Approach for High Selectivity In-Line Topology Filters Comprising N - 1 Adjacent Frequency-Variant Couplings. IEEE Access, 2019, 7, 41659-41668.	4.2	27
43	100-GHz Single-Flux-Quantum Bit-Serial Adder Based on 10-${m kA/cm}^{2}$ Niobium Process. IEEE Transactions on Applied Superconductivity, 2011, 21, 792-796.	1.7	26
44	HDL-Based Modeling Approach for Digital Simulation of Adiabatic Quantum Flux Parametron Logic. IEEE Transactions on Applied Superconductivity, 2016, 26, 1-5.	1.7	25
45	Design and Implementation of a 16-Word by 1-Bit Register File Using Adiabatic Quantum Flux Parametron Logic. IEEE Transactions on Applied Superconductivity, 2017, 27, 1-4.	1.7	25
46	Synthesis Flow for Cell-Based Adiabatic Quantum-Flux-Parametron Structural Circuit Generation With HDL Back-End Verification. IEEE Transactions on Applied Superconductivity, 2017, 27, 1-5.	1.7	25
47	Design methodology of single-flux-quantum flip-flops composed of both 0- and Ï€-shifted Josephson junctions. Superconductor Science and Technology, 2018, 31, 105003.	3.5	25
48	Superconductive Random Number Generator Using Thermal Noises in SFQ Circuits. IEEE Transactions on Applied Superconductivity, 2009, 19, 630-633.	1.7	24
49	Design, Implementation and On-Chip High-Speed Test of SFQ Half-Precision Floating-Point Multiplier. IEEE Transactions on Applied Superconductivity, 2009, 19, 657-660.	1.7	24
50	16-Bit Wave-Pipelined Sparse-Tree RSFQ Adder. IEEE Transactions on Applied Superconductivity, 2013, 23, 1700605-1700605.	1.7	24
51	8-Bit Asynchronous Sparse-Tree Superconductor RSFQ Arithmetic-Logic Unit With a Rich Set of Operations. IEEE Transactions on Applied Superconductivity, 2013, 23, 1700104-1700104.	1.7	24
52	Structure-Parameter Dependence of Modality of Macroscopic Quantum Effect in Superconductor Junction (I) â€“Tunnel-Type Junctionâ€“. Japanese Journal of Applied Physics, 1989, 28, 1816-1824.	1.5	23
53	Simulation and Measurements on a 64-kbit Hybrid Josephson-CMOS Memory. IEEE Transactions on Applied Superconductivity, 2005, 15, 415-418.	1.7	23
54	High-Speed Demonstration of Bit-Serial Floating-Point Adders and Multipliers Using Single-Flux-Quantum Circuits. IEEE Transactions on Applied Superconductivity, 2015, 25, 1-6.	1.7	23

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55	Three-dimensional adiabatic quantum-flux-parametron fabricated using a double-active-layered niobium process. Superconductor Science and Technology, 2017, 30, 075003.	3.5	23
56	Development and Demonstration of Routing and Placement EDA Tools for Large-Scale Adiabatic Quantum-Flux-Parametron Circuits. IEEE Transactions on Applied Superconductivity, 2017, 27, 1-9.	1.7	23
57	Low-latency adiabatic superconductor logic using delay-line clocking. Applied Physics Letters, 2019, 115, .	3.3	23
58	Reversibility and energy dissipation in adiabatic superconductor logic. Scientific Reports, 2017, 7, 75.	3.3	22
59	A semi-custom design methodology and environment for implementing superconductor adiabatic quantum-flux-parametron microprocessors. Superconductor Science and Technology, 2020, 33, 054006.	3.5	22
60	Self-timing and vector processing in RSFQ digital circuit technology. IEEE Transactions on Applied Superconductivity, 1999, 9, 7-17.	1.7	21
61	Design and implementation of SFQ programmable clock generators. Physica C: Superconductivity and Its Applications, 2004, 412-414, 1550-1554.	1.2	21
62	Josephson-CMOS Hybrid Memory With Nanocryotrons. IEEE Transactions on Applied Superconductivity, 2017, 27, 1-4.	1.7	21
63	Measurement of low bit-error-rates of adiabatic quantum-flux-parametron logic using a superconductor voltage driver. Applied Physics Letters, 2017, 110, .	3.3	21
64	A Majority Logic Synthesis Framework for Adiabatic Quantum-Flux-Parametron Superconducting Circuits. , 2019, , .		21
65	Implementation of a 4<tex>$times$</tex>4 Switch With Passive Interconnects. IEEE Transactions on Applied Superconductivity, 2005, 15, 356-359.	1.7	20
66	20-GHz 8 $imes$ 8-bit Parallel Carry-Save Pipelined RSFQ Multiplier. IEEE Transactions on Applied Superconductivity, 2013, 23, 1300104-1300104.	1.7	20
67	Josephson-CMOS hybrid memory with ultra-high-speed interface circuit. IEEE Transactions on Applied Superconductivity, 2003, 13, 467-470.	1.7	19
68	Design and Implementation and On-Chip High-Speed Test of SFQ Half-Precision Floating-Point Adders. IEEE Transactions on Applied Superconductivity, 2009, 19, 634-639.	1.7	19
69	Novel latch for adiabatic quantum-flux-parametron logic. Journal of Applied Physics, 2014, 115, 103910.	2.5	19
70	A new design approach for RSFQ logic circuits based on the binary decision diagram. IEEE Transactions on Applied Superconductivity, 1999, 9, 3161-3164.	1.7	18
71	Design of single flux quantum cells for a 10-Nb-layer process. Physica C: Superconductivity and Its Applications, 2009, 469, 1670-1673.	1.2	18
72	An Operand Routing Network for an SFQ Reconfigurable Data-Paths Processor. IEEE Transactions on Applied Superconductivity, 2009, 19, 665-669.	1.7	18

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73	Adiabatic quantum-flux-parametron interface for the readout of superconducting nanowire single-photon detectors. Optics Express, 2017, 25, 32650.	3.4	18
74	Scalable readout interface for superconducting nanowire single-photon detectors using AQFP and RSFQ logic families. Optics Express, 2020, 28, 15824.	3.4	18
75	A behavioral-level HDL description of SFQ logic circuits for quantitative performance analysis of large-scale SFQ digital systems. Physica C: Superconductivity and Its Applications, 2003, 392-396, 1495-1500.	1.2	17
76	Single-Flux-Quantum (SFQ) Circuit Design and Test of Crossbar Switch Scheduler. IEEE Transactions on Applied Superconductivity, 2005, 15, 423-426.	1.7	17
77	Reduction of the supply current of single-flux-quantum time-to-digital converters by current recycling techniques. IEEE Transactions on Applied Superconductivity, 2017, , 1-1.	1.7	17
78	Adiabatic Quantum-Flux-Parametron: A Tutorial Review. IEICE Transactions on Electronics, 2022, E105.C, 251-263.	0.6	17
79	RSFQ multiplexer and demultiplexer. IEEE Transactions on Applied Superconductivity, 1999, 9, 3310-3313.	1.7	16
80	Design and Investigation of Gate-to-Gate Passive Interconnections for SFQ Logic Circuits. IEEE Transactions on Applied Superconductivity, 2005, 15, 3814-3820.	1.7	16
81	Planarization Process for Fabricating Multi-Layer Nb Integrated Circuits Incorporating Top Active Layer. IEEE Transactions on Applied Superconductivity, 2009, 19, 167-170.	1.7	16
82	A compact AQFP logic cell design using an 8-metal layer superconductor process. Superconductor Science and Technology, 2020, 33, 035010.	3.5	16
83	Complementary Digital Logic Using Resistively Coupled Single-Electron Transistor. Japanese Journal of Applied Physics, 1996, 35, 1140-1145.	1.5	15
84	Engineering issues in high-frequency RSFQ circuits. Physica C: Superconductivity and Its Applications, 2002, 372-376, 1-6.	1.2	15
85	Latency and Power Measurements on a 64-kb Hybrid Josephson-CMOS Memory. IEEE Transactions on Applied Superconductivity, 2007, 17, 526-529.	1.7	15
86	On-chip RSFQ microwave pulse generator using a multi-flux-quantum driver for controlling superconducting qubits. Physica C: Superconductivity and Its Applications, 2010, 470, 1550-1554.	1.2	15
87	Synthesis and Design of Quasi-Canonical Planar Filters Comprising Cascaded Frequency-Variant Blocks. IEEE Transactions on Microwave Theory and Techniques, 2021, 69, 671-681.	4.6	15
88	Design and implementation of circuit components of the SFQ microprocessor, CORE1. Superconductor Science and Technology, 2004, 17, 301-307.	3.5	14
89	20 GHz Operation of Bit-Serial Handshaking Systems Using Asynchronous SFQ Logic Circuits. IEEE Transactions on Applied Superconductivity, 2005, 15, 255-258.	1.7	14
90	SFQ Pulse Transfer Circuits Using Inductive Coupling for Current Recycling. IEEE Transactions on Applied Superconductivity, 2009, 19, 649-652.	1.7	14

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91	Fabrication of Adiabatic Quantum-Flux-Parametron Integrated Circuits Using an Automatic Placement Tool Based on Genetic Algorithms. IEEE Transactions on Applied Superconductivity, 2019, 29, 1-6.	1.7	14
92	Design and Characterization of Track Routing Architecture for RSFQ and AQFP Circuits in a Multilayer Process. IEEE Transactions on Applied Superconductivity, 2020, 30, 1-9.	1.7	14
93	Dual Conduction Characteristics Observed in Highly Resistive NbN Granular Thin Films. Japanese Journal of Applied Physics, 1987, 26, 949.	1.5	13
94	High-Speed Demonstration of Single-Flux-Quantum Crossâ€“Bar Switch up to 50 GHz. IEEE Transactions on Applied Superconductivity, 2005, 15, 6-10.	1.7	13
95	Research on Effective Moat Configuration for Nb Multi-Layer Device Structure. IEEE Transactions on Applied Superconductivity, 2009, 19, 603-606.	1.7	13
96	Demonstration of a 47.8ÂGHz High-Speed FFT Processor Using Single-Flux-Quantum Technology. IEEE Transactions on Applied Superconductivity, 2021, 31, 1-5.	1.7	13
97	Development of Passive Interconnection Technology for SFQ Circuits. IEICE Transactions on Electronics, 2005, E88-C, 198-207.	0.6	13
98	The Relationship Between Bit-Error Rate, Operating Speed and Circuit Scale of SFQ Circuits. IEEE Transactions on Applied Superconductivity, 2005, 15, 364-367.	1.7	12
99	Quantitative evaluation of delay time in the single-flux-quantum circuit. Physica C: Superconductivity and Its Applications, 2007, 463-465, 1068-1071.	1.2	12
100	3D simulation of superconducting microwave devices with an electromagnetic-field simulator. Physica C: Superconductivity and Its Applications, 2009, 469, 1662-1665.	1.2	12
101	Superconductor Amoeba-Inspired Problem Solvers for Combinatorial Optimization. Physical Review Applied, 2019, 11, .	3.8	12
102	A Buffer and Splitter Insertion Framework for Adiabatic Quantum-Flux-Parametron Superconducting Circuits. , 2019, , .		12
103	Component test toward single-flux-quantum processors. Physica C: Superconductivity and Its Applications, 2003, 392-396, 1490-1494.	1.2	11
104	Design and component test of SFQ shift register memories. IEEE Transactions on Applied Superconductivity, 2003, 13, 555-558.	1.7	11
105	Design and high-speed test of (4 Ã— 8)-bit single-flux-quantum shift register files. Superconductor Science and Technology, 2003, 16, 1456-1459.	3.5	11
106	Quantitative Evaluation of the Single-Flux- Quantum Cross/Bar Switch. IEEE Transactions on Applied Superconductivity, 2005, 15, 324-327.	1.7	11
107	Progress of Single Flux Quantum Packet Switch Technology. IEEE Transactions on Applied Superconductivity, 2005, 15, 411-414.	1.7	11
108	Access time measurements of Josephsonâ€“CMOS hybrid memory using single-flux-quantum circuits. Superconductor Science and Technology, 2006, 19, S350-S353.	3.5	11

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109	Design of an SFQ Microwave Chopper for Controlling Quantum Bits. IEEE Transactions on Applied Superconductivity, 2007, 17, 146-149.	1.7	11
110	Demonstration of 10k Gate-Scale Adiabatic-Quantum-Flux-Parametron Circuits. , 2015, , .		11
111	Fast and accurate inductance and coupling calculation for a multi-layer Nb process. Superconductor Science and Technology, 2015, 28, 035013.	3.5	11
112	Demonstration of single-flux-quantum readout circuits for time-of-flight mass spectrometry systems using superconducting strip ion detectors. Superconductor Science and Technology, 2015, 28, 074003.	3.5	11
113	Evaluation of current sensitivity of quantum flux parametron. Superconductor Science and Technology, 2017, 30, 084004.	3.5	11
114	Minimum energy dissipation required for a logically irreversible operation. Physical Review E, 2018, 97, 012124.	2.1	11
115	Systematic method to evaluate energy dissipation in adiabatic quantum-flux-parametron logic. Journal of Applied Physics, 2019, 126, .	2.5	11
116	A reversible full adder using adiabatic superconductor logic. Superconductor Science and Technology, 2019, 32, 035005.	3.5	11
117	Low-latency power-dividing clocking scheme for adiabatic quantum-flux-parametron logic. Applied Physics Letters, 2020, 116, .	3.3	11
118	Design and High-Speed Demonstration of Single-Flux-Quantum Bit-Serial Floating-Point Multipliers Using a 10kA/cm² Nb Process. IEICE Transactions on Electronics, 2014, E97.C, 188-193.	0.6	11
119	Demonstration of a Single-Flux-Quantum Microprocessor Operating With Josephson-CMOS Hybrid Memory. IEEE Transactions on Applied Superconductivity, 2020, 30, 1-6.	1.7	11
120	Macroscopic Quantum Effect Conjugate to Josephson Effect. Journal of the Physical Society of Japan, 1984, 53, 3146-3152.	1.6	10
121	Structure-Parameter Dependence of Modality of Macroscopic Quantum Effect in Superconductor Junction (II) â€“Linked Junctionâ€“. Japanese Journal of Applied Physics, 1991, 30, 263-273.	1.5	10
122	Hybrid Josephson-CMOS memory: a solution for the Josephson memory problem. Superconductor Science and Technology, 2002, 15, 1669-1674.	3.5	10
123	Signal integrity in large-scale single-flux-quantum circuit. Physica C: Superconductivity and Its Applications, 2006, 445-448, 1003-1007.	1.2	10
124	A New Design Approach for High-Throughput Arithmetic Circuits for Single-Flux-Quantum Microprocessors. IEEE Transactions on Applied Superconductivity, 2007, 17, 516-519.	1.7	10
125	Design Approach of Dynamically Reconfigurable Single Flux Quantum Logic Gates. IEEE Transactions on Applied Superconductivity, 2011, 21, 831-834.	1.7	10
126	Design and Implementation of 64-kb CMOS Static RAMs for Josephson-CMOS Hybrid Memories. IEEE Transactions on Applied Superconductivity, 2013, 23, 1700704-1700704.	1.7	10

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127	Design and demonstration of adiabatic quantum-flux-parametron logic circuits with superconductor magnetic shields. Superconductor Science and Technology, 2015, 28, 045020.	3.5	10
128	Inductance and Coupling of Stacked Vias in a Multilayer Superconductive IC Process. IEEE Transactions on Applied Superconductivity, 2015, 25, 1-4.	1.7	10
129	Majority Gate-Based Feedback Latches for Adiabatic Quantum Flux Parametron Logic. IEICE Transactions on Electronics, 2016, E99.C, 710-716.	0.6	10
130	Design and Demonstration of an Adiabatic-Quantum-Flux-Parametron Field-Programmable Gate Array Using Josephson-CMOS Hybrid Memories. IEEE Transactions on Applied Superconductivity, 2019, 29, 1-6.	1.7	10
131	AQFPTX: Adiabatic Quantum-Flux-Parametron Timing eXtraction Tool. , 2019, , .		10
132	A Compact Interface Between Adiabatic Quantum-Flux-Parametron and Rapid Single-Flux-Quantum Circuits. IEEE Transactions on Applied Superconductivity, 2021, 31, 1-5.	1.7	10
133	Logic Synthesis of Sequential Logic Circuits for Adiabatic Quantum-Flux-Parametron Logic. IEEE Transactions on Applied Superconductivity, 2021, 31, 1-5.	1.7	10
134	Design and Demonstration of a Single-Flux-Quantum Multi-Stop Time-to-Digital Converter for Time-of-Flight Mass Spectrometry. IEICE Transactions on Electronics, 2014, E97.C, 182-187.	0.6	10
135	Design and component test of RSFQ packet decoders for shift register memories. Physica C: Superconductivity and Its Applications, 2002, 378-381, 1475-1480.	1.2	9
136	Diagnostic Test of Large-Scale SFQ Shift Register. IEEE Transactions on Applied Superconductivity, 2007, 17, 422-425.	1.7	9
137	New Delay-Time Measurements on a 64-kb Josephsonâ€“CMOS Hybrid Memory With a 600-ps Access Time. IEEE Transactions on Applied Superconductivity, 2010, 20, 14-20.	1.7	9
138	Design and Implementation of Component Circuits of an SFQ Half-Precision Floating-Point Adder Using 10-kA/cm^{2} Nb Process. IEEE Transactions on Applied Superconductivity, 2011, 21, 827-830.	1.7	9
139	Development of Pulse Transfer Circuits for Serially Biased SFQ Circuits Using the Nb 9-Layer 1-$muhbox{m}$ Process. IEEE Transactions on Applied Superconductivity, 2013, 23, 1300504-1300504.	1.7	9
140	Design and Implementation of an SFQ-Based Single-Chip FFT Processor. IEEE Transactions on Applied Superconductivity, 2017, 27, 1-5.	1.7	9
141	Superconducting Digital Electronics for Controlling Quantum Computing Systems. IEICE Transactions on Electronics, 2019, E102.C, 217-223.	0.6	9
142	MANA: A Monolithic Adiabatic iNtegration Architecture Microprocessor using 1.4zJ/op Superconductor Josephson Junction Devices. , 2020, , .		9
143	Binary Counters Using Adiabatic Quantum-Flux-Parametron Logic. IEEE Transactions on Applied Superconductivity, 2021, 31, 1-5.	1.7	9
144	Impedance Design of Excitation Lines in Adiabatic Quantum-Flux-Parametron Logic Using InductEx. IEEE Transactions on Applied Superconductivity, 2021, 31, 1-5.	1.7	9

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145	Adiabatic Quantum-Flux-Parametron Constant Cells using Asymmetrical Structures. IEEJ Transactions on Fundamentals and Materials, 2016, 136, 747-752.	0.2	9
146	Directly coupled adiabatic superconductor logic. Superconductor Science and Technology, 2020, 33, 065002.	3.5	9
147	Field-Effect Induced Sinusoidal Conductivity Variation of NbN Granular Thin Film. Japanese Journal of Applied Physics, 1987, 26, L1701-L1702.	1.5	8
148	A cell-based design approach for RSFQ circuits using a binary decision diagram. Superconductor Science and Technology, 1999, 12, 782-785.	3.5	8
149	Simulation and 18 Gb/s testing of a data-driven self-timed RSFQ demultiplexer. IEEE Transactions on Applied Superconductivity, 1999, 9, 4349-4352.	1.7	8
150	Design and component test of a 1-bit RSFQ microprocessor. Physica C: Superconductivity and Its Applications, 2002, 378-381, 1454-1460.	1.2	8
151	Single-flux-quantum integer multiplier with systolic array structure. Physica C: Superconductivity and Its Applications, 2006, 445-448, 1014-1019.	1.2	8
152	The influence of the ground current on large-scale single-flux-quantum circuits. Superconductor Science and Technology, 2006, 19, S362-S365.	3.5	8
153	Clock Line Considerations for an SFQ Large Scale Reconfigurable Data Paths Processor. IEEE Transactions on Applied Superconductivity, 2011, 21, 809-813.	1.7	8
154	Development of Bit-Serial RSFQ Microprocessors Integrated with Shift-Register-Based Random Access Memories. , 2015, , .		8
155	Inductance and Current Distribution Extraction in Nb Multilayer Circuits with Superconductive and Resistive Components. IEICE Transactions on Electronics, 2016, E99.C, 683-691.	0.6	8
156	Multi-excitation adiabatic quantum-flux-parametron. Journal of Applied Physics, 2017, 121, .	2.5	8
157	Recent Progress on Reversible Quantum-Flux-Parametron for Superconductor Reversible Computing. IEICE Transactions on Electronics, 2018, E101.C, 352-358.	0.6	8
158	Adiabatic quantum-flux-parametron with Ï€ Josephson junctions. Journal of Applied Physics, 2019, 125, .	2.5	8
159	Low-Autocorrelation Random Number Generator Based on Adiabatic Quantum-Flux-Parametron Logic. IEEE Transactions on Applied Superconductivity, 2021, 31, 1-5.	1.7	8
160	Buffer Reduction Via N-Phase Clocking in Adiabatic Quantum-Flux-Parametron Benchmark Circuits. IEEE Transactions on Applied Superconductivity, 2021, 31, 1-8.	1.7	8
161	ASAP. , 2020, , .		8
162	Quantization of dielectric flux in phase-quantum-tunnel junction. IEEE Transactions on Magnetics, 1987, 23, 1130-1133.	2.1	7

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163	Quantized Electrical Field Effect in Granular Superconductor Thin Films. Japanese Journal of Applied Physics, 1990, 29, 1086-1096.	1.5	7
164	Coulomb blockade and electrical field effect in nanoscale granular microbridges. Applied Physics Letters, 1995, 67, 3969-3971.	3.3	7
165	Anomalous Effect inLa2-xSrxCuO4of Doping Levelx=1/4n. Japanese Journal of Applied Physics, 1996, 35, 1221-1224.	1.5	7
166	Component development for a 16 Gb/s RSFQ-CMOS interface system. IEEE Transactions on Applied Superconductivity, 2001, 11, 735-738.	1.7	7
167	A cell-based design approach for RSFQ circuits based on binary decision diagram. IEEE Transactions on Applied Superconductivity, 2001, 11, 263-266.	1.7	7
168	Single flux quantum circuit technology innovation for backbone router applications. Physica C: Superconductivity and Its Applications, 2003, 392-396, 1478-1484.	1.2	7
169	Error Rate Test of Large-Scale SFQ Digital Circuit Systems. IEEE Transactions on Applied Superconductivity, 2005, 15, 427-430.	1.7	7
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