Johannes Partzsch

List of Publications by Year
in descending order

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42	769	687363	642732
papers	citations	13 h-index	23 g-index

42	42	42	830
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	The operating system of the neuromorphic BrainScaleS-1 system. Neurocomputing, 2022, 501, 790-810.	5.9	5
2	Real-time Hardware Implementation of ARM CoreSight Trace Decoder. IEEE Design and Test, 2021, 38, 69-77.	1.2	2
3	Analyzing ARM CoreSight ETMv4.x Data Trace Stream with a Real-time Hardware Accelerator. , 2021, , .		1
4	Comparing Loihi with a SpiNNaker 2 prototype on low-latency keyword spotting and adaptive robotic control. Neuromorphic Computing and Engineering, 2021, 1, 014002.	5.9	26
5	Delay-Based Neural Computation: Pulse Routing Architecture and Benchmark Application in FPGA. , 2021, , .		0
6	Plasticity and Adaptation in Neuromorphic Biohybrid Systems. IScience, 2020, 23, 101589.	4.1	26
7	Mean Field Approach for Configuring Population Dynamics on a Biohybrid Neuromorphic System. Journal of Signal Processing Systems, 2020, 92, 1303-1321.	2.1	2
8	Flexible and stretchable redistribution layer with embedded chips for human-machine interface. , 2020, , .		4
9	Mapping Deep Neural Networks on SpiNNaker2. , 2020, , .		3
10	Event-based Neural Network for ECG Classification with Delta Encoding and Early Stopping. , 2020, , .		6
11	Efficient Reward-Based Structural Plasticity on a SpiNNaker 2 Prototype. IEEE Transactions on Biomedical Circuits and Systems, 2019, 13, 579-591.	4.0	20
12	A Biohybrid Setup for Coupling Biological and Neuromorphic Neural Networks. Frontiers in Neuroscience, 2019, 13, 432.	2.8	24
13	Dynamic Power Management for Neuromorphic Many-Core Systems. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 2973-2986.	5.4	12
14	Memory-Efficient Deep Learning on a SpiNNaker 2 Prototype. Frontiers in Neuroscience, 2018, 12, 840.	2.8	38
15	Neuromorphic hardware in the loop: Training a deep spiking network on the BrainScaleS wafer-scale system. , 2017, , .		99
16	Exploration of FPGA architectures for tight coupled accelerators in a 22nm FDSOI technology. , 2017, , .		0
17	Live demonstration: Dynamic voltage and frequency scaling for neuromorphic many-core systems. , 2017, , .		1
18	A fixed point exponential function accelerator for a neuromorphic many-core system. , 2017, , .		21

#	Article	IF	Citations
19	Dynamic voltage and frequency scaling for neuromorphic many-core systems. , 2017, , .		3
20	A Calibration Technique for Bang-Bang ADPLLs Using Jitter Distribution Monitoring. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 3548-3552.	3.1	5
21	A Biological-Realtime Neuromorphic System in 28 nm CMOS Using Low-Leakage Switched Capacitor Circuits. IEEE Transactions on Biomedical Circuits and Systems, 2016, 10, 243-254.	4.0	77
22	Reducing the computational footprint for real-time BCPNN learning. Frontiers in Neuroscience, 2015, 9, 2.	2.8	13
23	Switched-capacitor realization of presynaptic short-term-plasticity and stop-learning synapses in 28 nm CMOS. Frontiers in Neuroscience, 2015, 9, 10.	2.8	27
24	Network-driven design principles for neuromorphic systems. Frontiers in Neuroscience, 2015, 9, 386.	2.8	4
25	Configurable analog-digital conversion using the neural engineering framework. Frontiers in Neuroscience, 2014, 8, 201.	2.8	10
26	A pulse communication flow ready for accelerated neuromorphic experiments. , 2014, , .		3
27	VLSI implementation of a conductance-based multi-synapse using switched-capacitor circuits. , 2014, , .		17
28	Configurable pulse routing architecture for accelerated multi-node neuromorphic systems. , 2014, , .		0
29	A location-independent direct link neuromorphic interface. , 2013, , .		13
30	Live demonstration: A scaled-down version of the BrainScaleS wafer-scale neuromorphic system. , 2012, , .		41
31	Accuracy evaluation of numerical methods used in state-of-the-art simulators for spiking neural networks. Journal of Computational Neuroscience, 2012, 32, 309-326.	1.0	17
32	Developing structural constraints on connectivity for biologically embedded neural networks. Biological Cybernetics, 2012, 106, 191-200.	1.3	6
33	A 32 GBit/s communication SoC for a waferscale neuromorphic system. The Integration VLSI Journal, 2012, 45, 61-75.	2.1	30
34	Analyzing the Scaling of Connectivity in Neuromorphic Hardware and in Models of Neural Networks. IEEE Transactions on Neural Networks, 2011, 22, 919-935.	4.2	39
35	A comprehensive workflow for general-purpose neural modeling with highly configurable neuromorphic hardware systems. Biological Cybernetics, 2011, 104, 263-296.	1.3	72
36	Synapse dynamics in CMOS derived from a model of neurotransmitter release. , 2011, , .		7

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37	VLSI implementation of a 2.8 Gevent/s packet-based AER interface with routing and event sorting functionality. Frontiers in Neuroscience, 2011, 5, 117.	2.8	36
38	Rate and pulse based plasticity governed by local synaptic state variables. Frontiers in Synaptic Neuroscience, 2010, 2, 33.	2.5	35
39	Replicating experimental spike and rate based neural learning in CMOS. , 2010, , .		18
40	On the Relation between Bursts and Dynamic Synapse Properties: A Modulation-Based Ansatz. Computational Intelligence and Neuroscience, 2009, 2009, 1-13.	1.7	2
41	Transient responses of activity-dependent synapses to modulated pulse trains. Neurocomputing, 2009, 73, 99-105.	5.9	1
42	BCM and Membrane Potential: Alternative Ways to Timing Dependent Plasticity. Lecture Notes in Computer Science, 2009, , 137-144.	1.3	3