Alex Orailoglu

List of Publications by Year
in descending order

53 papers	340 citations	1307594 7 h-index	1281871 11 g-index
53 all docs	53 docs citations	53 times ranked	183 citing authors

#	Article	IF	Citations
1	Unleashing the Potential of Sparse DNNs Through Synergistic Hardware-Sparsity Co-Design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 1147-1160.	2.7	2
2	Guest Editorial: Special Issue on 2020 IEEE International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS 2020). International Journal of Parallel Programming, 2022, 50, 187-188.	1.5	1
3	AdaTrust: Combinational Hardware Trojan Detection Through Adaptive Test Pattern Construction. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 544-557.	3.1	11
4	SNR: <u>S</u> queezing <u>N</u> umerical <u>R</u> ange Defuses Bit Error Vulnerability Surface in Deep Neural Networks. Transactions on Embedded Computing Systems, 2021, 20, 1-25.	2.9	14
5	Boosting Bit-Error Resilience of DNN Accelerators Through Median Feature Selection. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 3250-3262.	2.7	21
6	Taming Combinational Trojan Detection Challenges with Self-Referencing Adaptive Test Patterns. , 2020, , .		2
7	Test Pattern Superposition to Detect Hardware Trojans. , 2020, , .		6
8	Concurrent Monitoring of Operational Health in Neural Networks Through Balanced Output Partitions. , 2020, , .		10
9	Low-Cost Error Detection in Deep Neural Network Accelerators with Linear Algorithmic Checksums. Journal of Electronic Testing: Theory and Applications (JETTA), 2020, 36, 703-718.	1.2	10
10	Detecting Gas Vapor Leaks through Uncalibrated Sensor Based CPS. , 2019, , .		5
11	Shielding Logic Locking from Redundancy Attacks. , 2019, , .		5
12	Sanity-Check: Boosting the Reliability of Safety-Critical Deep Neural Network Applications. , 2019, , .		43
13	Piercing Logic Locking Keys through Redundancy Identification. , 2019, , .		39
14	Variation-Aware Hardware Trojan Detection through Power Side-channel. , 2018, , .		18
15	Ensuring system security through proximity based authentication. , 2017, , .		2
16	Detecting hardware Trojans without a Golden IC through clock-tree defined circuit partitions. , 2017, , .		13
17	Aggressive Test Cost Reductions Through Continuous Test Effectiveness Assessment. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 2093-2103.	2.7	7
18	Power-Aware Delay Test Quality Optimization for Multiple Frequency Domains. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 141-154.	2.7	0

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19	Joint Profit and Process Variation Aware High Level Synthesis With Speed Binning. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1640-1650.	3.1	3
20	Examining Timing Path Robustness Under Wide-Bandwidth Power Supply Noise Through Multi-Functional-Cycle Delay Test. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 734-746.	3.1	2
21	Full exploitation of process variation space for continuous delivery of optimal delay test quality. , 2013, , .		2
22	Towards a cost-effective hardware trojan detection methodology. , 2013, , .		1
23	Branch Prediction directed Dynamic instruction Cache Locking for embedded systems. , 2013, , .		1
24	On Diagnosis of Timing Failures in Scan Architecture. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1102-1115.	2.7	3
25	Delay test resource allocation and scheduling for multiple frequency domains. , 2012, , .		1
26	Tackling Resource Variations Through Adaptive Multicore Execution Frameworks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 132-145.	2.7	2
27	Register allocation for simultaneous reduction of energy and peak temperature on registers. , 2011, , .		1
28	Adaptive Test Framework for Achieving Target Test Quality at Minimal Cost. , 2011, , .		3
29	Full Fault Resilience and Relaxed Synchronization Requirements at the Cache-Memory Interface. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1996-2009.	3.1	1
30	Frugal but flexible multicore topologies in support of resource variation-driven adaptivity. , 2011, , .		1
31	Adaptive test optimization through real time learning of test effectiveness. , 2011, , .		5
32	Squashing code size in microcoded IPs while delivering high decompression speed. Design Automation for Embedded Systems, 2010, 14, 265-284.	1.0	0
33	Fine-grained adaptive CMP cache sharing through access history exploitation. , 2010, , .		0
34	Fully adaptive multicore architectures through statically-directed dynamic execution reconfigurations. , 2010, , .		4
35	DiSC: A New Diagnosis Method for Multiple Scan Chain Failures. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 2051-2055.	2.7	4
36	Making DNA self-assembly error-proof: Attaining small growth error rates through embedded information redundancy. , 2009, , .		0

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37	Scan Cell Positioning for Boosting the Compression of Fan-Out Networks. Journal of Computer Science and Technology, 2009, 24, 939-948.	1.5	0
38	Processor reliability enhancement through compiler-directed register file peak temperature reduction. , 2009, , .		7
39	Towards no-cost adaptive MPSoC static schedules through exploitation of logical-to-physical core mapping latitude. , 2009, , .		4
40	Low-Power Scan Testing for Test Data Compression Using a Routing-Driven Scan Architecture. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 1101-1105.	2.7	20
41	Application Specific Low Latency Instruction Cache for NAND Flash Memory Based Embedded Systems. , 2008, , .		3
42	Online test and fault-tolerance for nanoelectronic programmable logic arrays. , 2008, , .		3
43	Leveraging CMOS design tools for QCA designs. , 2008, , .		0
44	Core-Based Testing of Multiprocessor System-on-Chips Utilizing Hierarchical Functional Buses. , 2007, , .		5
45	Design automation for hybrid CMOS-nonoelectronics crossbars. , 2007, , .		3
46	Power efficient register file update approach for embedded processors. , 2007, , .		2
47	Power-Constrained SOC Test Schedules through Utilization of Functional Buses. Proceedings - IEEE International Conference on Computer Design: VLSI in Computers and Processors, 2006, , .	0.0	9
48	Efficient RT-Level Fault Diagnosis. Journal of Computer Science and Technology, 2005, 20, 166-174.	1.5	0
49	Searching for Global Test Costs Optimization in Core-Based Systems. Journal of Electronic Testing: Theory and Applications (JETTA), 2004, 20, 357-373.	1.2	1
50	Reducing Average and Peak Test Power Through Scan Chain Modification. Journal of Electronic Testing: Theory and Applications (JETTA), 2003, 19, 457-467.	1.2	13
51	Improved fault diagnosis in scan-based BIST via superposition. , 2000, , .		24
52	On-Line Fault Resilience Through Gracefully Degradable ASICs. Journal of Electronic Testing: Theory and Applications (JETTA), 1998, 12, 145-151.	1.2	1
53	Module Selection in Microarchitectural Synthesis for Multiple Critical Constraint Satisfaction. VLSI Design, 1997, 5, 167-182.	0.5	2