Yu Wang

List of Publications by Year in descending order

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Version: 2024-02-01

292 papers	9,451 citations	159585 30 h-index	118850 62 g-index
297 all docs	297 docs citations	297 times ranked	5754 citing authors

#	Article	IF	Citations
1	Dual-Timescale Resource Allocation for Collaborative Service Caching and Computation Offloading in IoT Systems. IEEE Transactions on Industrial Informatics, 2023, 19, 1735-1746.	11.3	3
2	INCAME: Interruptible CNN Accelerator for Multirobot Exploration. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 964-978.	2.7	2
3	A Unified FPGA Virtualization Framework for General-Purpose Deep Neural Networks in the Cloud. ACM Transactions on Reconfigurable Technology and Systems, 2022, 15, 1-31.	2.5	2
4	MR-GMMapping: Communication Efficient Multi-Robot Mapping System via Gaussian Mixture Model. IEEE Robotics and Automation Letters, 2022, 7, 3294-3301.	5.1	8
5	A Learning-Based AoA Estimation Method for Device-Free Localization. IEEE Communications Letters, 2022, 26, 1264-1267.	4.1	5
6	Reliability evaluation of FPGA based pruned neural networks. Microelectronics Reliability, 2022, 130, 114498.	1.7	4
7	Efficient In-Memory AES Encryption Implementation Using a General Memristive Logic: Surmounting the data movement bottleneck. IEEE Nanotechnology Magazine, 2022, 16, 24-C3.	1.3	2
8	Gibbon: Efficient Co-Exploration of NN Model and Processing-In-Memory Architecture. , 2022, , .		7
9	Exploiting Parallelism with Vertex-Clustering in Processing-In-Memory-based GCN Accelerators. , 2022, , .		2
10	DIMMining. , 2022, , .		14
11	Reliability-Aware Training and Performance Modeling for Processing-In-Memory Systems. , 2021, , .		1
12	A Survey of FPGA-Based Robotic Computing. IEEE Circuits and Systems Magazine, 2021, 21, 48-74.	2.3	38
13	Enabling Lower-Power Charge-Domain Nonvolatile In-Memory Computing With Ferroelectric FETs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 2262-2266.	3.0	18
14	3M-AI: A Multi-task and Multi-core Virtualization Framework for Multi-FPGA AI Systems in the Cloud. , 2021, , .		1
15	GAME: Gaussian Mixture Model Mapping and Navigation Engine on Embedded FPGA. , 2021, , .		3
16	MNSIM-TIME: Performance Modeling Framework for Training-In-Memory Architectures. , 2021, , .		2
17	Robotic Computing on FPGAs. Synthesis Lectures on Computer Architecture, 2021, 16, 1-218.	1.3	7
18	Ensemble of Pruned Networks for Reliable Classifiers. , 2021, , .		2

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19	Rescuing RRAM-Based Computing From Static and Dynamic Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2049-2062.	2.7	8
20	FTT-NAS: Discovering Fault-tolerant Convolutional Neural Architecture. ACM Transactions on Design Automation of Electronic Systems, 2021, 26, 1-24.	2.6	9
21	Low-Cost Multi-Agent Navigation via Reinforcement Learning With Multi-Fidelity Simulator. IEEE Access, 2021, 9, 84773-84782.	4.2	1
22	Efficient Computing Platform Design for Autonomous Driving Systems. , 2021, , .		1
23	SMMR-Explore: SubMap-based Multi-Robot Exploration System with Multi-robot Multi-target Potential Field Exploration Method. , 2021, , .		24
24	Low Bit-Width Convolutional Neural Network on RRAM. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 1414-1427.	2.7	37
25	DNNVM: End-to-End Compiler Leveraging Heterogeneous Optimizations on FPGA-Based CNN Accelerators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2668-2681.	2.7	52
26	CNN-based Monocular Decentralized SLAM on embedded FPGA. , 2020, , .		7
27	Enabling Efficient and Flexible FPGA Virtualization for Deep Learning in the Cloud. , 2020, , .		13
28	Enabling Secure NVM-Based in-Memory Neural Network Computing by Sparse Fast Gradient Encryption. IEEE Transactions on Computers, 2020, 69, 1596-1610.	3.4	15
29	INCA: INterruptible CNN Accelerator for Multi-tasking in Embedded Robots. , 2020, , .		5
30	Efficient 16 Boolean logic and arithmetic based on bipolar oxide memristors. Science China Information Sciences, 2020, 63, 1.	4.3	16
31	Soft Error Mitigation for Deep Convolution Neural Network on FPGA Accelerators. , 2020, , .		11
32	Communication Lower Bound in Convolution Accelerators. , 2020, , .		21
33	One-Shot Refresh: A Low-Power Low-Congestion Approach for Dynamic Memories. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3402-3406.	3.0	3
34	Nonparametric Topic Modeling with Neural Inference. Neurocomputing, 2020, 399, 296-306.	5.9	8
35	CNN-based Feature-point Extraction for Real-time Visual SLAM on Embedded FPGA. , 2020, , .		26
36	FTT-NAS: Discovering Fault-Tolerant Neural Architecture. , 2020, , .		20

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37	Black Box Search Space Profiling for Accelerator-Aware Neural Architecture Search. , 2020, , .		5
38	Long Live TIME: Improving Lifetime and Security for NVM-Based Training-in-Memory Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4707-4720.	2.7	9
39	Adaptive Circuit Approaches to Low-Power Multi-Level/Cell FeFET Memory. , 2020, , .		3
40	An Energy-Efficient Quantized and Regularized Training Framework For Processing-In-Memory Accelerators. , 2020, , .		18
41	33.2 A Fully Integrated Analog ReRAM Based 78.4TOPS/W Compute-In-Memory Chip with Fully Parallel MAC Computing. , 2020, , .		121
42	Distribution-Balanced Loss for Multi-label Classification in Long-Tailed Datasets. Lecture Notes in Computer Science, 2020, , 162-178.	1.3	96
43	A Generic Graph-Based Neural Architecture Encoding Scheme for Predictor-Based NAS. Lecture Notes in Computer Science, 2020, , 189-204.	1.3	29
44	FeFET-based low-power bitwise logic-in-memory with direct write-back and data-adaptive dynamic sensing interface. , 2020, , .		14
45	An Order Sampling Processing-in-Memory Architecture for Approximate Graph Pattern Mining. , 2020, , .		1
46	MNSIM 2.0: A Behavior-Level Modeling Tool for Memristor-based Neuromorphic Computing Systems. , 2020, , .		35
47	Algorithmic Fault Detection for RRAM-based Matrix Operations. ACM Transactions on Design Automation of Electronic Systems, 2020, 25, 1-31.	2.6	9
48	Adversarial Vision Challenge. The Springer Series on Challenges in Machine Learning, 2020, , 129-153.	10.4	9
49	Security Enhancement for RRAM Computing System through Obfuscating Crossbar Row Connections. , 2020, , .		4
50	Feature Variance Regularization: A Simple Way to Improve the Generalizability of Neural Networks. Proceedings of the AAAI Conference on Artificial Intelligence, 2020, 34, 4190-4197.	4.9	3
51	DSA: More Efficient Budgeted Pruning via Differentiable Sparsity Allocation. Lecture Notes in Computer Science, 2020, , 592-607.	1.3	36
52	INCAME: INterruptible CNN Accelerator for Multi-robot Exploration. , 2020, , .		0
53	Enable Efficient and Flexible FPGA Virtualization for Deep Learning in the Cloud. , 2020, , .		0
54	DualLip. , 2020, , .		12

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55	GraphSDH: A General Graph Sampling Framework with Distribution and Hierarchy. , 2020, , .		1
56	LessMine: Reducing Sample Space and Data Access for Dense Pattern Mining. , 2020, , .		0
57	Optimizing CNN Accelerator With Improved Roofline Model. , 2020, , .		2
58	GE-SpMM: General-Purpose Sparse Matrix-Matrix Multiplication on GPUs for Graph Neural Networks. , 2020, , .		42
59	Fault-Tolerant Training Enabled by On-Line Fault Detection for RRAM-Based Neural Computing Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1611-1624.	2.7	33
60	An In-depth Comparison of Compilers for Deep Neural Networks on Hardware. , 2019, , .		8
61	Multi-task ADAS system on FPGA. , 2019, , .		11
62	Memory-Bound Proof-of-Work Acceleration for Blockchain Applications. , 2019, , .		4
63	Towards artificial general intelligence with hybrid Tianjic chip architecture. Nature, 2019, 572, 106-111.	27.8	517
64	On-Chip Instruction Generation for Cross-Layer CNN Accelerator on FPGA. , 2019, , .		4
65	HyVE: Hybrid Vertex-Edge Memory Hierarchy for Energy-Efficient Graph Processing. IEEE Transactions on Computers, 2019, 68, 1131-1146.	3.4	6
66	Fault tolerance in neuromorphic computing systems. , 2019, , .		27
67	GraphSAR. , 2019, , .		34
68	A Configurable Multi-Precision CNN Computing Framework Based on Single Bit RRAM. , 2019, , .		50
69	Memristorâ€Based Efficient Inâ€Memory Logic for Cryptologic and Arithmetic Applications. Advanced Materials Technologies, 2019, 4, 1900212.	5.8	33
70	Learning the sparsity for ReRAM. , 2019, , .		55
71	[DL] A Survey of FPGA-based Neural Network Inference Accelerators. ACM Transactions on Reconfigurable Technology and Systems, 2019, 12, 1-26.	2.5	150
72	Augmentation Invariant Training. , 2019, , .		3

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73	A digitalized RRAM-based Spiking Neuron Network system with 3-bit weight and unsupervised online learning scheme. , 2019, , .		0
74	A General Logic Synthesis Framework for Memristor-based Logic Design. , 2019, , .		5
75	HDC-IM: Hyperdimensional Computing In-Memory Architecture based on RRAM. , 2019, , .		6
76	Enabling Secure in-Memory Neural Network Computing by Sparse Fast Gradient Encryption. , 2019, , .		21
77	GraphH: A Processing-in-Memory Architecture for Large-Scale Graph Processing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 640-653.	2.7	75
78	TIME: A Training-in-Memory Architecture for RRAM-Based Deep Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 834-847.	2.7	44
79	DNNVM. , 2019, , .		7
80	A Fine-Grained Sparse Accelerator for Multi-Precision DNN. , 2019, , .		2
81	Compressed CNN Training with FPGA-based Accelerator. , 2019, , .		14
82	PAGANI Toolkit: Parallel graphâ€theoretical analysis package for brain network big data. Human Brain Mapping, 2018, 39, 1869-1885.	3.6	12
83	Real-time object detection towards high power efficiency. , 2018, , .		19
84	Rescuing memristor-based computing with non-linear resistance levels. , 2018, , .		7
85	A peripheral circuit reuse structure integrated with a retimed data flow for low power RRAM crossbar-based CNN. , 2018, , .		10
86	Bidirectional Database Storage and SQL Query Exploiting RRAM-Based Process-in-Memory Structure. ACM Transactions on Storage, 2018, 14, 1-19.	2.1	5
87	Towards Real-Time Object Detection on Embedded Systems. IEEE Transactions on Emerging Topics in Computing, 2018, 6, 417-431.	4.6	58
88	Angel-Eye: A Complete Design Flow for Mapping CNN Onto Embedded FPGA. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 35-47.	2.7	382
89	Hardware Trojan Detection in Third-Party Digital Intellectual Property Cores by Multilevel Feature Analysis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1370-1383.	2.7	42
90	Stuck-at Fault Tolerance in RRAM Computing Systems. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 102-115.	3.6	88

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91	Fault Tolerance for RRAM-Based Matrix Operations. , 2018, , .		22
92	Mixed size crossbar based RRAM CNN accelerator with overlapped mapping method. , 2018, , .		30
93	Long live TIME. , 2018, , .		30
94	An Efficient Reconfigurable Framework for General Purpose CNN-RNN Models on FPGAs. , 2018, , .		6
95	GraphIA. , 2018, , .		10
96	Real-Time Object Detection and Semantic Segmentation Hardware System with Deep Learning Networks. , 2018, , .		13
97	Instruction Driven Cross-layer CNN Accelerator for Fast Detection on FPGA. ACM Transactions on Reconfigurable Technology and Systems, 2018, 11, 1-23.	2.5	14
98	NewGraph: Balanced Large-Scale Graph Processing on FPGAs with Low Preprocessing Overheads. , 2018, , .		0
99	HyVE: Hybrid vertex-edge memory hierarchy for energy-efficient graph processing. , 2018, , .		13
100	Low power driven loop tiling for RRAM crossbar-based CNN. , 2018, , .		1
101	Training low bitwidth convolutional neural network on RRAM. , 2018, , .		17
102	RRAM Based Buffer Design for Energy Efficient CNN Accelerator. , 2018, , .		5
103	Hu-Fu: Hardware and Software Collaborative Attack Framework Against Neural Networks. , 2018, , .		29
104	Design of fault-tolerant neuromorphic computing systems. , 2018, , .		14
105	Binary convolutional neural network on RRAM. , 2017, , .		119
106	Computation-oriented fault-tolerance schemes for RRAM computing systems. , 2017, , .		31
107	ESE. , 2017, , .		414
108	A Deep Learning Approach for Blind Drift Calibration of Sensor Networks. IEEE Sensors Journal, 2017, 17, 4158-4171.	4.7	59

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109	Low-overhead implementation of logic encryption using gate replacement techniques. , 2017, , .		9
110	Software-Hardware Codesign for Efficient Neural Network Acceleration. IEEE Micro, 2017, 37, 18-25.	1.8	65
111	Circuit design for beyond von Neumann applications using emerging memory: From nonvolatile logics to neuromorphic computing. , 2017, , .		21
112	The First 25 Years of the FPL Conference. ACM Transactions on Reconfigurable Technology and Systems, 2017, 10, 1-17.	2.5	1
113	ForeGraph. , 2017, , .		100
114	A General Framework for Hardware Trojan Detection in Digital Circuits by Statistical Learning Algorithms. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1633-1646.	2.7	23
115	Fault-Tolerant Training with On-Line Fault Detection for RRAM-Based Neural Computing Systems. , 2017, , .		105
116	Exploring the Granularity of Sparsity in Convolutional Neural Networks. , 2017, , .		124
117	MNSIM: Simulation Platform for Memristor-based Neuromorphic Computing System. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, , 1-1.	2.7	42
118	Exploiting Stable Data Dependency in Stream Processing Acceleration on FPGAs. Transactions on Embedded Computing Systems, 2017, 16, 1-26.	2.9	0
119	A 462GOPs/J RRAM-based nonvolatile intelligent processor for energy harvesting IoE system featuring nonvolatile logics and processing-in-memory. , 2017, , .		21
120	An FPGA Design Framework for CNN Sparsification and Acceleration. , 2017, , .		17
121	A ReRAM-Based Nonvolatile Flip-Flop With Self-Write-Termination Scheme for Frequent-OFF Fast-Wake-Up Nonvolatile Processors. IEEE Journal of Solid-State Circuits, 2017, 52, 2194-2207.	5.4	41
122	A Compact Memristor-Based Dynamic Synapse for Spiking Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1353-1366.	2.7	81
123	Energy Efficient RRAM Crossbar-Based Approximate Computing for Smart Cameras. , 2017, , 109-133.		1
124	Instruction driven cross-layer CNN accelerator with winograd transformation on FPGA. , 2017, , .		27
125	Energy-efficient SQL query exploiting RRAM-based process-in-memory structure. , 2017, , .		5
126	A 462GOPs/J RRAM-based nonvolatile intelligent processor for energy harvesting IoE system featuring nonvolatile logics and processing-in-memory. , 2017, , .		3

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127	Streaming sorting network based BWT acceleration on FPGA for lossless compression. , 2017, , .		3
128	Energy Efficient Spiking Neural Network Design with RRAM Devices. , 2017, , 245-259.		1
129	A data locality-aware design framework for reconfigurable sparse matrix-vector multiplication kernel. , 2016, , .		8
130	RRAM based learning acceleration. , 2016, , .		2
131	Going Deeper with Embedded FPGA Platform for Convolutional Neural Network. , 2016, , .		836
132	NXgraph: An efficient graph processing system on a single machine. , 2016, , .		63
133	Angel-Eye: A Complete Design Flow for Mapping CNN onto Customized Hardware. , 2016, , .		52
134	Approximate Frequent Itemset Mining for streaming data on FPGA. , 2016, , .		1
135	SRI-SURF: A better SURF powered by scaled-RAM interpolator on FPGA. , 2016, , .		1
136	Switched by input. , 2016, , .		76
137	Low power Convolutional Neural Networks on a chip. , 2016, , .		27
138	Heterogeneous systems with reconfigurable neuromorphic computing accelerators. , 2016, , .		6
139	Real-Time Pedestrian Detection and Tracking on Customized Hardware. , 2016, , .		4
140	PRIME: A Novel Processing-in-Memory Architecture for Neural Network Computation in ReRAM-Based Main Memory. , 2016, , .		238
141	From model to FPGA: Software-hardware co-design for efficient neural network acceleration. , 2016, , .		14
142	All Spin Artificial Neural Networks Based on Compound Spintronic Synapse and Neuron. IEEE Transactions on Biomedical Circuits and Systems, 2016, 10, 828-836.	4.0	84
143	Performance-centric register file design for GPUs using racetrack memory. , 2016, , .		4
144	Harmonica: A Framework of Heterogeneous Computing Systems With Memristor-Based Neuromorphic Computing Accelerators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 617-628.	5.4	49

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145	Modeling Random Telegraph Noise as a Randomness Source and its Application in True Random Number Generation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1435-1448.	2.7	23
146	A Unified Methodology for Designing Hardware Random Number Generators Based on Any Probability Distribution. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 783-787.	3.0	8
147	Technological Exploration of RRAM Crossbar Array for Matrix-Vector Multiplication. Journal of Computer Science and Technology, 2016, 31, 3-19.	1.5	117
148	Exploring the Precision Limitation for RRAM-Based Analog Approximate Computing. IEEE Design and Test, 2016, 33, 51-58.	1.2	15
149	FPGP. , 2016, , .		91
150	PRIME. Computer Architecture News, 2016, 44, 27-39.	2.5	823
151	MNSIM: Simulation Platform for Memristor-based Neuromorphic Computing System. , 2016, , .		27
152	Sparsity-Oriented Sparse Solver Design for Circuit Simulation. , 2016, , .		2
153	Scaling-up resistive synaptic arrays for neuro-inspired architecture: Challenges and prospect. , 2015, , .		128
154	Testâ€“Retest Reliability of Graph Metrics in Highâ€resolution Functional Connectomics: A Restingâ€State Functional <scp>MRI</scp> Study. CNS Neuroscience and Therapeutics, 2015, 21, 802-816.	3.9	41
155	Spiking Neural Network with RRAM: Can We Use It for Real-World Application?. , 2015, , .		25
156	Integrated Photonic Reservoir Computing based on Hierarchical Time-multiplexing Structure. , 2015, , .		0
157	Technological exploration of RRAM crossbar array for matrix-vector multiplication. , 2015, , .		16
158	Energy Efficient RRAM Spiking Neural Network for Real Time Classification. , 2015, , .		35
159	Merging the interface. , 2015, , .		73
160	A self-aware data compression system on FPGA in Hadoop. , 2015, , .		4
161	Significant papers from the first 25 years of the FPL conference. , 2015, , .		1
162	FASTrust: Feature analysis for third-party IP trust verification. , 2015, , .		28

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163	An FPGA-based real-time simultaneous localization and mapping system. , 2015, , .		9
164	Rebooting Computing and Low-Power Image Recognition Challenge. , 2015, , .		12
165	Real-Time High-Quality Stereo Vision System in FPGA. IEEE Transactions on Circuits and Systems for Video Technology, 2015, 25, 1696-1708.	8.3	86
166	GPU-Accelerated Sparse LU Factorization for Circuit Simulation with Performance Modeling. IEEE Transactions on Parallel and Distributed Systems, 2015, 26, 786-795.	5.6	52
167	A STT-RAM-based low-power hybrid register file for GPGPUs. , 2015, , .		23
168	Hi-fi playback. , 2015, , .		58
169	RENO. , 2015, , .		111
170	Modeling and optimization of low power resonant clock mesh. , 2015, , .		2
171	HS3-DPG: Hierarchical Simulation for 3-D P/G Network. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2307-2311.	3.1	1
172	Energy-efficient neuromorphic computation based on compound spin synapse with stochastic learning. , 2015, , .		13
173	Coordinated static and dynamic cache bypassing for GPUs. , 2015, , .		104
174	FPGA Acceleration of Recurrent Neural Network Based Language Model. , 2015, , .		77
175	RRAM-Based Analog Approximate Computing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1905-1917.	2.7	100
176	Whitespace-Aware TSV Arrangement in 3-D Clock Tree Synthesis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1842-1853.	3.1	4
177	A Fast Parallel Sparse Solver for SPICE-Based Circuit Simulators. , 2015, , .		5
178	ICE: Inline calibration for memristor crossbar-based computing engine. , 2014, , .		5
179	PS3-RAM: A Fast Portable and Scalable Statistical STT-RAM Reliability/Energy Analysis Method. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1644-1656.	2.7	14
180	On-Chip Hybrid Power Supply System for Wireless Sensor Nodes. ACM Journal on Emerging Technologies in Computing Systems, 2014, 10, 1-22.	2.3	0

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181	Run-Time Technique for Simultaneous Aging and Power Optimization in GPGPUs. , 2014, , .		24
182	Online scheduling for FPGA computation in the Cloud. , 2014, , .		16
183	Enabling FPGAs in the cloud. , 2014, , .		139
184	Design Methodologies for 3D Mixed Signal Integrated Circuits. , 2014, , .		4
185	Accelerating frequent item counting with FPGA. , 2014, , .		16
186	Hardware Acceleration for an Accurate Stereo Vision System Using Mini-Census Adaptive Support Region. Transactions on Embedded Computing Systems, 2014, 13, 1-24.	2.9	29
187	Energy efficient spiking neural network design with RRAM devices. , 2014, , .		8
188	Integrated photonic reservoir computing based on hierarchical time-multiplexing structure. Optics Express, 2014, 22, 31356.	3.4	49
189	The stochastic modeling of TiO<inf>2</inf> memristor and its usage in neuromorphic system design. , 2014, , .		16
190	Statistical analysis of random telegraph noise in digital circuits. , 2014, , .		5
191	A universal FPGA-based floating-point matrix processor for mobile systems. , 2014, , .		5
192	ICE: Inline calibration for memristor crossbar-based computing engine. , 2014, , .		11
193	Training itself: Mixed-signal training acceleration for memristor-based neural network. , 2014, , .		62
194	Efficient region-aware P/G TSV planning for 3D ICs. , 2014, , .		6
195	GraphGen: An FPGA Framework for Vertex-Centric Graph Computation. , 2014, , .		75
196	Large scale recurrent neural network on GPU. , 2014, , .		45
197	Energy efficient neural networks for big data analytics. , 2014, , .		6
198	TSV-aware topology generation for 3D Clock Tree Synthesis. , 2013, , .		6

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199	A 1.9ÂGHz ADPLL with 130 reference cycles settling time in 0.18ÂÎ¼m CMOS technology. Analog Integrated Circuits and Signal Processing, 2013, 76, 81-89.	1.4	2
200	NICSLU: An Adaptive Sparse Matrix Solver for Parallel Circuit Simulation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 261-274.	2.7	57
201	Assessment of Circuit Optimization Techniques Under NBTI. IEEE Design and Test, 2013, 30, 40-49.	1.2	17
202	BER guaranteed optimization and implementation of parallel turbo decoding on GPU. , 2013, , .		2
203	On-Chip Sensor Network for Efficient Management of Power Gating-Induced Power/Ground Noise in Multiprocessor System on Chip. IEEE Transactions on Parallel and Distributed Systems, 2013, 24, 767-777.	5.6	4
204	ADAMS: Asymmetric differential STT-RAM cell structure for reliable and high-performance applications. , 2013, , .		11
205	HS3DPG: Hierarchical simulation for 3D P/G network. , 2013, , .		3
206	Real-time high-quality stereo vision system in FPGA. , 2013, , .		18
207	Memristor-based approximated computation. , 2013, , .		37
208	Accelerating subsequence similarity search based on dynamic time warping distance with FPGA. , 2013, , .		27
209	DTW-Based Subsequence Similarity Search on AMD Heterogeneous Computing Platform. , 2013, , .		1
210	Whitespace-aware TSV arrangement in 3D clock tree synthesis. , 2013, , .		6
211	Nonzero pattern analysis and memory access optimization in GPU-based sparse LU factorization for circuit simulation. , 2013, , .		1
212	UNIFICATION OF PR REGION FLOORPLANNING AND FINE-GRAINED PLACEMENT FOR DYNAMIC PARTIALLY RECONFIGURABLE FPGAS. Journal of Circuits, Systems and Computers, 2013, 22, 1350020.	1.5	3
213	Evaluation and mitigation of performance degradation under random telegraph noise for digital circuits. IET Circuits, Devices and Systems, 2013, 7, 273-282.	1.4	0
214	A Hybrid CPU-GPU Accelerated Framework for Fast Mapping of High-Resolution Human Brain Connectome. PLoS ONE, 2013, 8, e62789.	2.5	22
215	Pub/Sub on stream. , 2012, , .		8
216	Sparse LU factorization for parallel circuit simulation on GPU. , 2012, , .		33

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217	Parallel FPGA-based all pairs shortest paths for sparse networks: A human brain connectome case study. , 2012, , .		14
218	Parallel Circuit Simulation on Multi/Many-core Systems. , 2012, , .		2
219	Probabilistic Brain Fiber Tractography on GPUs. , 2012, , .		6
220	FPGA based memory efficient high resolution stereo vision system for video tolling. , 2012, , .		14
221	A Reconfigurable Computing Approach for Efficient and Scalable Parallel Graph Exploration. , 2012, , .		44
222	Thermal-aware power network design for IR drop reduction in 3D ICs. , 2012, , .		8
223	An adaptive LU factorization algorithm for parallel circuit simulation. , 2012, , .		17
224	Temporal Performance Degradation under RTN: Evaluation and Mitigation for Nanoscale Circuits. , 2012, , .		7
225	PS3-RAM. , 2012, , .		36
226	Parametric Yield-Driven Resource Binding in High-Level Synthesis with Multi-Vth/VddLibrary and Device Sizing. Journal of Electrical and Computer Engineering, 2012, 2012, 1-14.	0.9	1
227	Variation-Aware Supply Voltage Assignment for Simultaneous Power and Aging Optimization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 2143-2147.	3.1	23
228	Yield-aware time-efficient testing and self-fixing design for TSV-based 3D ICs. , 2012, , .		12
229	Temperature-Aware NBTI Modeling and the Impact of Standby Leakage Reduction Techniques on Circuit Performance Degradation. IEEE Transactions on Dependable and Secure Computing, 2011, 8, 756-769.	5.4	24
230	Gemma in April: A matrix-like parallel programming architecture on OpenCL. , 2011, , .		0
231	Circuit-level delay modeling considering both TDDB and NBTI. , 2011, , .		13
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