Yu Wang

List of Publications by Year in descending order

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292 papers	9,451 citations	159585 30 h-index	118850 62 g-index
297 all docs	297 docs citations	297 times ranked	5754 citing authors

#	Article	IF	Citations
1	Going Deeper with Embedded FPGA Platform for Convolutional Neural Network. , 2016, , .		836
2	PRIME. Computer Architecture News, 2016, 44, 27-39.	2.5	823
3	Towards artificial general intelligence with hybrid Tianjic chip architecture. Nature, 2019, 572, 106-111.	27.8	517
4	ESE. , 2017, , .		414
5	Angel-Eye: A Complete Design Flow for Mapping CNN Onto Embedded FPGA. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 35-47.	2.7	382
6	PRIME: A Novel Processing-in-Memory Architecture for Neural Network Computation in ReRAM-Based Main Memory. , 2016, , .		238
7	[DL] A Survey of FPGA-based Neural Network Inference Accelerators. ACM Transactions on Reconfigurable Technology and Systems, 2019, 12, 1-26.	2.5	150
8	Enabling FPGAs in the cloud. , 2014, , .		139
9	Scaling-up resistive synaptic arrays for neuro-inspired architecture: Challenges and prospect. , 2015, , .		128
10	Exploring the Granularity of Sparsity in Convolutional Neural Networks. , 2017, , .		124
11	FPMR. , 2010, , .		122
12	33.2 A Fully Integrated Analog ReRAM Based 78.4TOPS/W Compute-In-Memory Chip with Fully Parallel MAC Computing. , 2020, , .		121
13	Binary convolutional neural network on RRAM. , 2017, , .		119
14	Technological Exploration of RRAM Crossbar Array for Matrix-Vector Multiplication. Journal of Computer Science and Technology, 2016, 31, 3-19.	1.5	117
15	RENO. , 2015, , .		111
16	Fault-Tolerant Training with On-Line Fault Detection for RRAM-Based Neural Computing Systems. , 2017, , .		105
17	Coordinated static and dynamic cache bypassing for GPUs. , 2015, , .		104
18	RRAM-Based Analog Approximate Computing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1905-1917.	2.7	100

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19	ForeGraph. , 2017, , .		100
20	Distribution-Balanced Loss for Multi-label Classification in Long-Tailed Datasets. Lecture Notes in Computer Science, 2020, , 162-178.	1.3	96
21	FPGP. , 2016, , .		91
22	Stuck-at Fault Tolerance in RRAM Computing Systems. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 102-115.	3.6	88
23	Real-Time High-Quality Stereo Vision System in FPGA. IEEE Transactions on Circuits and Systems for Video Technology, 2015, 25, 1696-1708.	8.3	86
24	All Spin Artificial Neural Networks Based on Compound Spintronic Synapse and Neuron. IEEE Transactions on Biomedical Circuits and Systems, 2016, 10, 828-836.	4.0	84
25	A Compact Memristor-Based Dynamic Synapse for Spiking Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1353-1366.	2.7	81
26	FPGA Acceleration of Recurrent Neural Network Based Language Model. , 2015, , .		77
27	Switched by input. , 2016, , .		76
28	GraphGen: An FPGA Framework for Vertex-Centric Graph Computation. , 2014, , .		75
29	GraphH: A Processing-in-Memory Architecture for Large-Scale Graph Processing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 640-653.	2.7	75
30	Merging the interface. , 2015, , .		73
31	Software-Hardware Codesign for Efficient Neural Network Acceleration. IEEE Micro, 2017, 37, 18-25.	1.8	65
32	NXgraph: An efficient graph processing system on a single machine. , 2016, , .		63
33	Training itself: Mixed-signal training acceleration for memristor-based neural network. , 2014, , .		62
34	A Deep Learning Approach for Blind Drift Calibration of Sensor Networks. IEEE Sensors Journal, 2017, 17, 4158-4171.	4.7	59
35	Hi-fi playback. , 2015, , .		58
36	Towards Real-Time Object Detection on Embedded Systems. IEEE Transactions on Emerging Topics in Computing, 2018, 6, 417-431.	4.6	58

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37	NICSLU: An Adaptive Sparse Matrix Solver for Parallel Circuit Simulation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 261-274.	2.7	57
38	On the efficacy of input Vector Control to mitigate NBTI effects and leakage power. , 2009, , .		56
39	Learning the sparsity for ReRAM. , 2019, , .		55
40	GPU-Accelerated Sparse LU Factorization for Circuit Simulation with Performance Modeling. IEEE Transactions on Parallel and Distributed Systems, 2015, 26, 786-795.	5.6	52
41	Angel-Eye: A Complete Design Flow for Mapping CNN onto Customized Hardware. , 2016, , .		52
42	DNNVM: End-to-End Compiler Leveraging Heterogeneous Optimizations on FPGA-Based CNN Accelerators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2668-2681.	2.7	52
43	A Configurable Multi-Precision CNN Computing Framework Based on Single Bit RRAM. , 2019, , .		50
44	Temperature-aware NBTI modeling and the impact of input vector control on performance degradation. , 2007, , .		49
45	Leakage Power and Circuit Aging Cooptimization by Gate Replacement Techniques. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 615-628.	3.1	49
46	Integrated photonic reservoir computing based on hierarchical time-multiplexing structure. Optics Express, 2014, 22, 31356.	3.4	49
47	Harmonica: A Framework of Heterogeneous Computing Systems With Memristor-Based Neuromorphic Computing Accelerators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 617-628.	5.4	49
48	Large scale recurrent neural network on GPU. , 2014, , .		45
49	A Reconfigurable Computing Approach for Efficient and Scalable Parallel Graph Exploration. , 2012, , .		44
50	TIME: A Training-in-Memory Architecture for RRAM-Based Deep Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 834-847.	2.7	44
51	MNSIM: Simulation Platform for Memristor-based Neuromorphic Computing System. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, , 1-1.	2.7	42
52	Hardware Trojan Detection in Third-Party Digital Intellectual Property Cores by Multilevel Feature Analysis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1370-1383.	2.7	42
53	GE-SpMM: General-Purpose Sparse Matrix-Matrix Multiplication on GPUs for Graph Neural Networks. , 2020, , .		42
54	Three-dimensional integrated circuits (3D IC) Floorplan and Power/Ground Network Co-synthesis. , 2010, , .		41

#	Article	IF	Citations
55	Testâ€“Retest Reliability of Graph Metrics in Highâ€resolution Functional Connectomics: A Restingâ€State Functional <scp>MRI</scp> Study. CNS Neuroscience and Therapeutics, 2015, 21, 802-816.	3.9	41
56	A ReRAM-Based Nonvolatile Flip-Flop With Self-Write-Termination Scheme for Frequent-OFF Fast-Wake-Up Nonvolatile Processors. IEEE Journal of Solid-State Circuits, 2017, 52, 2194-2207.	5.4	41
57	Modeling of PMOS NBTI Effect Considering Temperature Variation. , 2007, , .		39
58	A Survey of FPGA-Based Robotic Computing. IEEE Circuits and Systems Magazine, 2021, 21, 48-74.	2.3	38
59	Memristor-based approximated computation. , 2013, , .		37
60	Low Bit-Width Convolutional Neural Network on RRAM. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 1414-1427.	2.7	37
61	PS3-RAM. , 2012, , .		36
62	DSA: More Efficient Budgeted Pruning via Differentiable Sparsity Allocation. Lecture Notes in Computer Science, 2020, , 592-607.	1.3	36
63	An EScheduler-Based Data Dependence Analysis and Task Scheduling for Parallel Circuit Simulation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 702-706.	3.0	35
64	Energy Efficient RRAM Spiking Neural Network for Real Time Classification. , 2015, , .		35
65	MNSIM 2.0: A Behavior-Level Modeling Tool for Memristor-based Neuromorphic Computing Systems. , 2020, , .		35
66	GraphSAR. , 2019, , .		34
67	Sparse LU factorization for parallel circuit simulation on GPU. , 2012, , .		33
68	Fault-Tolerant Training Enabled by On-Line Fault Detection for RRAM-Based Neural Computing Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1611-1624.	2.7	33
69	Memristorâ€Based Efficient Inâ€Memory Logic for Cryptologic and Arithmetic Applications. Advanced Materials Technologies, 2019, 4, 1900212.	5.8	33
70	Efficient PageRank and SpMV Computation on AMD GPUs. , 2010, , .		32
71	Computation-oriented fault-tolerance schemes for RRAM computing systems. , 2017, , .		31
72	Mixed size crossbar based RRAM CNN accelerator with overlapped mapping method. , 2018, , .		30

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73	Long live TIME. , 2018, , .		30
74	Hardware Acceleration for an Accurate Stereo Vision System Using Mini-Census Adaptive Support Region. Transactions on Embedded Computing Systems, 2014, 13, 1-24.	2.9	29
75	Hu-Fu: Hardware and Software Collaborative Attack Framework Against Neural Networks. , 2018, , .		29
76	A Generic Graph-Based Neural Architecture Encoding Scheme for Predictor-Based NAS. Lecture Notes in Computer Science, 2020, , 189-204.	1.3	29
77	FASTrust: Feature analysis for third-party IP trust verification. , 2015, , .		28
78	Accelerating subsequence similarity search based on dynamic time warping distance with FPGA. , 2013, , .		27
79	Low power Convolutional Neural Networks on a chip. , 2016, , .		27
80	Instruction driven cross-layer CNN accelerator with winograd transformation on FPGA. , 2017, , .		27
81	Fault tolerance in neuromorphic computing systems. , 2019, , .		27
82	MNSIM: Simulation Platform for Memristor-based Neuromorphic Computing System. , 2016, , .		27
83	CNN-based Feature-point Extraction for Real-time Visual SLAM on Embedded FPGA. , 2020, , .		26
84	Spiking Neural Network with RRAM: Can We Use It for Real-World Application?. , 2015, , .		25
85	Temperature-Aware NBTI Modeling and the Impact of Standby Leakage Reduction Techniques on Circuit Performance Degradation. IEEE Transactions on Dependable and Secure Computing, 2011, 8, 756-769.	5.4	24
86	Run-Time Technique for Simultaneous Aging and Power Optimization in GPGPUs. , 2014, , .		24
87	SMMR-Explore: SubMap-based Multi-Robot Exploration System with Multi-robot Multi-target Potential Field Exploration Method. , 2021, , .		24
88	FPGA and GPU implementation of large scale SpMV. , 2010, , .		23
89	Variation-Aware Supply Voltage Assignment for Simultaneous Power and Aging Optimization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 2143-2147.	3.1	23
90	A STT-RAM-based low-power hybrid register file for GPGPUs. , 2015, , .		23

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91	Modeling Random Telegraph Noise as a Randomness Source and its Application in True Random Number Generation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1435-1448.	2.7	23
92	A General Framework for Hardware Trojan Detection in Digital Circuits by Statistical Learning Algorithms. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1633-1646.	2.7	23
93	A Hybrid CPU-GPU Accelerated Framework for Fast Mapping of High-Resolution Human Brain Connectome. PLoS ONE, 2013, 8, e62789.	2.5	22
94	Fault Tolerance for RRAM-Based Matrix Operations. , 2018, , .		22
95	Circuit design for beyond von Neumann applications using emerging memory: From nonvolatile logics to neuromorphic computing. , 2017, , .		21
96	A 462GOPs/J RRAM-based nonvolatile intelligent processor for energy harvesting IoE system featuring nonvolatile logics and processing-in-memory. , 2017, , .		21
97	Enabling Secure in-Memory Neural Network Computing by Sparse Fast Gradient Encryption. , 2019, , .		21
98	Communication Lower Bound in Convolution Accelerators. , 2020, , .		21
99	FTT-NAS: Discovering Fault-Tolerant Neural Architecture. , 2020, , .		20
100	Real-time object detection towards high power efficiency. , 2018, , .		19
101	Real-time high-quality stereo vision system in FPGA. , 2013, , .		18
102	An Energy-Efficient Quantized and Regularized Training Framework For Processing-In-Memory Accelerators. , 2020, , .		18
103	Enabling Lower-Power Charge-Domain Nonvolatile In-Memory Computing With Ferroelectric FETs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 2262-2266.	3.0	18
104	An adaptive LU factorization algorithm for parallel circuit simulation. , 2012, , .		17
105	Assessment of Circuit Optimization Techniques Under NBTI. IEEE Design and Test, 2013, 30, 40-49.	1.2	17
106	An FPGA Design Framework for CNN Sparsification and Acceleration. , 2017, , .		17
107	Training low bitwidth convolutional neural network on RRAM. , 2018, , .		17
108	A Novel Gate-Level NBTI Delay Degradation Model with Stacking Effect. Lecture Notes in Computer Science, 2007, , 160-170.	1.3	17

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109	Fast-locking all-digital phase-locked loop with digitally controlled oscillator tuning word estimating and presetting. IET Circuits, Devices and Systems, 2010, 4, 207.	1.4	16
110	Online scheduling for FPGA computation in the Cloud. , 2014, , .		16
111	Accelerating frequent item counting with FPGA. , 2014, , .		16
112	The stochastic modeling of TiO<inf>2</inf> memristor and its usage in neuromorphic system design. , 2014, , .		16
113	Technological exploration of RRAM crossbar array for matrix-vector multiplication. , 2015, , .		16
114	Efficient 16 Boolean logic and arithmetic based on bipolar oxide memristors. Science China Information Sciences, 2020, 63, 1.	4.3	16
115	Exploring the Precision Limitation for RRAM-Based Analog Approximate Computing. IEEE Design and Test, 2016, 33, 51-58.	1.2	15
116	Enabling Secure NVM-Based in-Memory Neural Network Computing by Sparse Fast Gradient Encryption. IEEE Transactions on Computers, 2020, 69, 1596-1610.	3.4	15
117	Parallel FPGA-based all pairs shortest paths for sparse networks: A human brain connectome case study. , 2012, , .		14
118	FPGA based memory efficient high resolution stereo vision system for video tolling. , 2012, , .		14
119	PS3-RAM: A Fast Portable and Scalable Statistical STT-RAM Reliability/Energy Analysis Method. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1644-1656.	2.7	14
120	From model to FPGA: Software-hardware co-design for efficient neural network acceleration. , 2016, , .		14
121	Instruction Driven Cross-layer CNN Accelerator for Fast Detection on FPGA. ACM Transactions on Reconfigurable Technology and Systems, 2018, 11, 1-23.	2.5	14
122	Design of fault-tolerant neuromorphic computing systems. , 2018, , .		14
123	FeFET-based low-power bitwise logic-in-memory with direct write-back and data-adaptive dynamic sensing interface. , 2020, , .		14
124	Compressed CNN Training with FPGA-based Accelerator. , 2019, , .		14
125	DIMMining. , 2022, , .		14
126	Circuit-level delay modeling considering both TDDB and NBTI. , 2011, , .		13

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127	Energy-efficient neuromorphic computation based on compound spin synapse with stochastic learning. , 2015, , .		13
128	Real-Time Object Detection and Semantic Segmentation Hardware System with Deep Learning Networks. , 2018, , .		13
129	HyVE: Hybrid vertex-edge memory hierarchy for energy-efficient graph processing. , 2018, , .		13
130	Enabling Efficient and Flexible FPGA Virtualization for Deep Learning in the Cloud. , 2020, , .		13
131	Gate replacement techniques for simultaneous leakage and aging optimization. , 2009, , .		12
132	Yield-aware time-efficient testing and self-fixing design for TSV-based 3D ICs. , 2012, , .		12
133	Rebooting Computing and Low-Power Image Recognition Challenge. , 2015, , .		12
134	PAGANI Toolkit: Parallel graphâ€theoretical analysis package for brain network big data. Human Brain Mapping, 2018, 39, 1869-1885.	3.6	12
135	DualLip. , 2020, , .		12
136	A power gating scheme for ground bounce reduction during mode transition. , 2007, , .		11
137	Variation-aware supply voltage assignment for minimizing circuit degradation and leakage. , 2009, , .		11
138	New-Age: A Negative Bias Temperature Instability-Estimation Framework for Microarchitectural Components. International Journal of Parallel Programming, 2009, 37, 417-431.	1.5	11
139	NBTI-aware statistical circuit delay assessment. , 2009, , .		11
140	Power Gating Aware Task Scheduling in MPSoC. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1801-1812.	3.1	11
141	ADAMS: Asymmetric differential STT-RAM cell structure for reliable and high-performance applications. , 2013, , .		11
142	ICE: Inline calibration for memristor crossbar-based computing engine. , 2014, , .		11
143	Multi-task ADAS system on FPGA. , 2019, , .		11
144	Soft Error Mitigation for Deep Convolution Neural Network on FPGA Accelerators. , 2020, , .		11

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145	A peripheral circuit reuse structure integrated with a retimed data flow for low power RRAM crossbar-based CNN. , 2018, , .		10
146	GraphIA. , 2018, , .		10
147	SIGNAL-PATH-LEVEL DUAL-Vt ASSIGNMENT FOR LEAKAGE POWER REDUCTION. Journal of Circuits, Systems and Computers, 2006, 15, 197-216.	1.5	9
148	On-line MPSoC Scheduling Considering Power Gating Induced Power/Ground Noise. , 2009, , .		9
149	An FPGA-based real-time simultaneous localization and mapping system. , 2015, , .		9
150	Low-overhead implementation of logic encryption using gate replacement techniques. , 2017, , .		9
151	Long Live TIME: Improving Lifetime and Security for NVM-Based Training-in-Memory Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4707-4720.	2.7	9
152	FTT-NAS: Discovering Fault-tolerant Convolutional Neural Architecture. ACM Transactions on Design Automation of Electronic Systems, 2021, 26, 1-24.	2.6	9
153	Algorithmic Fault Detection for RRAM-based Matrix Operations. ACM Transactions on Design Automation of Electronic Systems, 2020, 25, 1-31.	2.6	9
154	Adversarial Vision Challenge. The Springer Series on Challenges in Machine Learning, 2020, , 129-153.	10.4	9
155	Pub/Sub on stream. , 2012, , .		8
156	Thermal-aware power network design for IR drop reduction in 3D ICs. , 2012, , .		8
157	Energy efficient spiking neural network design with RRAM devices. , 2014, , .		8
158	A data locality-aware design framework for reconfigurable sparse matrix-vector multiplication kernel. , 2016, , .		8
159	A Unified Methodology for Designing Hardware Random Number Generators Based on Any Probability Distribution. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 783-787.	3.0	8
160	An In-depth Comparison of Compilers for Deep Neural Networks on Hardware. , 2019, , .		8
161	Nonparametric Topic Modeling with Neural Inference. Neurocomputing, 2020, 399, 296-306.	5.9	8
162	Rescuing RRAM-Based Computing From Static and Dynamic Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2049-2062.	2.7	8

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163	MR-GMMapping: Communication Efficient Multi-Robot Mapping System via Gaussian Mixture Model. IEEE Robotics and Automation Letters, 2022, 7, 3294-3301.	5.1	8
164	A framework for estimating NBTI degradation of microarchitectural components. , 2009, , .		7
165	Hardware computing for brain network analysis. , 2010, , .		7
166	Temporal Performance Degradation under RTN: Evaluation and Mitigation for Nanoscale Circuits. , 2012, , .		7
167	Rescuing memristor-based computing with non-linear resistance levels. , 2018, , .		7
168	CNN-based Monocular Decentralized SLAM on embedded FPGA. , 2020, , .		7
169	Robotic Computing on FPGAs. Synthesis Lectures on Computer Architecture, 2021, 16, 1-218.	1.3	7
170	DNNVM. , 2019, , .		7
171	Temperature-Aware NBTI Modeling Techniques in Digital Circuits. IEICE Transactions on Electronics, 2009, E92-C, 875-886.	0.6	7
172	Gibbon: Efficient Co-Exploration of NN Model and Processing-In-Memory Architecture. , 2022, , .		7
173	The NBTI Impact on RF Front End in Wireless Sensor Networks. , 2009, , .		6
174	Making Human Connectome Faster: GPU Acceleration of Brain Network Analysis. , 2010, , .		6
175	A Hardware-Software Collaborated Method for Soft-Error Tolerant MPSoC. , 2011, , .		6
176	Rethinking thermal via planning with timing-power-temperature dependence for 3D ICs. , 2011, , .		6
177	Probabilistic Brain Fiber Tractography on GPUs. , 2012, , .		6
178	TSV-aware topology generation for 3D Clock Tree Synthesis. , 2013, , .		6
179	Whitespace-aware TSV arrangement in 3D clock tree synthesis. , 2013, , .		6
180	Efficient region-aware P/G TSV planning for 3D ICs. , 2014, , .		6

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181	Energy efficient neural networks for big data analytics. , 2014, , .		6
182	Heterogeneous systems with reconfigurable neuromorphic computing accelerators. , 2016, , .		6
183	An Efficient Reconfigurable Framework for General Purpose CNN-RNN Models on FPGAs. , 2018, , .		6
184	HyVE: Hybrid Vertex-Edge Memory Hierarchy for Energy-Efficient Graph Processing. IEEE Transactions on Computers, 2019, 68, 1131-1146.	3.4	6
185	HDC-IM: Hyperdimensional Computing In-Memory Architecture based on RRAM. , 2019, , .		6
186	Dynamic TDM virtual circuit implementation for NoC. , 2008, , .		5
187	RankBoost Acceleration on both NVIDIA CUDA and ATI Stream Platforms. , 2009, , .		5
188	Simulation and analysis of P/G noise in TSV based 3D MPSoC. , 2010, , .		5
189	The impact of correlation between NBTI and TDDB on the performance of digital circuits. , 2011, , .		5
190	ICE: Inline calibration for memristor crossbar-based computing engine. , 2014, , .		5
191	Statistical analysis of random telegraph noise in digital circuits. , 2014, , .		5
192	A universal FPGA-based floating-point matrix processor for mobile systems. , 2014, , .		5
193	Energy-efficient SQL query exploiting RRAM-based process-in-memory structure. , 2017, , .		5
194	Bidirectional Database Storage and SQL Query Exploiting RRAM-Based Process-in-Memory Structure. ACM Transactions on Storage, 2018, 14, 1-19.	2.1	5
195	RRAM Based Buffer Design for Energy Efficient CNN Accelerator. , 2018, , .		5
196	A General Logic Synthesis Framework for Memristor-based Logic Design. , 2019, , .		5
197	INCA: INterruptible CNN Accelerator for Multi-tasking in Embedded Robots. , 2020, , .		5
198	Black Box Search Space Profiling for Accelerator-Aware Neural Architecture Search. , 2020, , .		5

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199	A Fast Parallel Sparse Solver for SPICE-Based Circuit Simulators. , 2015, , .		5
200	A Learning-Based AoA Estimation Method for Device-Free Localization. IEEE Communications Letters, 2022, 26, 1264-1267.	4.1	5
201	An FPGA-based accelerator for LambdaRank in Web search engines. ACM Transactions on Reconfigurable Technology and Systems, 2011, 4, 1-19.	2.5	4
202	On-Chip Sensor Network for Efficient Management of Power Gating-Induced Power/Ground Noise in Multiprocessor System on Chip. IEEE Transactions on Parallel and Distributed Systems, 2013, 24, 767-777.	5.6	4
203	Design Methodologies for 3D Mixed Signal Integrated Circuits. , 2014, , .		4
204	A self-aware data compression system on FPGA in Hadoop. , 2015, , .		4
205	Whitespace-Aware TSV Arrangement in 3-D Clock Tree Synthesis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1842-1853.	3.1	4
206	Real-Time Pedestrian Detection and Tracking on Customized Hardware. , 2016, , .		4
207	Performance-centric register file design for GPUs using racetrack memory. , 2016, , .		4
208	Memory-Bound Proof-of-Work Acceleration for Blockchain Applications. , 2019, , .		4
209	On-Chip Instruction Generation for Cross-Layer CNN Accelerator on FPGA. , 2019, , .		4
210	Security Enhancement for RRAM Computing System through Obfuscating Crossbar Row Connections. , 2020, , .		4
211	Reliability evaluation of FPGA based pruned neural networks. Microelectronics Reliability, 2022, 130, 114498.	1.7	4
212	A fast-locking all-digital phase-locked loop with a novel counter-based mode switching controller. , 2009, , .		3
213	A heterogeneous accelerator platform for multi-subject voxel-based brain network analysis. , 2011, , .		3
214	HS3DPG: Hierarchical simulation for 3D P/G network. , 2013, , .		3
215	UNIFICATION OF PR REGION FLOORPLANNING AND FINE-GRAINED PLACEMENT FOR DYNAMIC PARTIALLY RECONFIGURABLE FPGAS. Journal of Circuits, Systems and Computers, 2013, 22, 1350020.	1.5	3
216	A 462GOPs/J RRAM-based nonvolatile intelligent processor for energy harvesting IoE system featuring nonvolatile logics and processing-in-memory. , 2017, , .		3

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217	Streaming sorting network based BWT acceleration on FPGA for lossless compression. , 2017, , .		3
218	Augmentation Invariant Training. , 2019, , .		3
219	One-Shot Refresh: A Low-Power Low-Congestion Approach for Dynamic Memories. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3402-3406.	3.0	3
220	Adaptive Circuit Approaches to Low-Power Multi-Level/Cell FeFET Memory. , 2020, , .		3
221	GAME: Gaussian Mixture Model Mapping and Navigation Engine on Embedded FPGA. , 2021, , .		3
222	Thermal-Aware Incremental Floorplanning for 3D ICs Based on MILP Formulation. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2009, E92-A, 2979-2989.	0.3	3
223	Feature Variance Regularization: A Simple Way to Improve the Generalizability of Neural Networks. Proceedings of the AAAI Conference on Artificial Intelligence, 2020, 34, 4190-4197.	4.9	3
224	Dual-Timescale Resource Allocation for Collaborative Service Caching and Computation Offloading in IoT Systems. IEEE Transactions on Industrial Informatics, 2023, 19, 1735-1746.	11.3	3
225	Output Remapping Technique for Soft-Error Rate Reduction in Critical Paths. , 2008, , .		2
226	Two-Phase Fine-Grain Sleep Transistor Insertion Technique in Leakage Critical Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 1101-1113.	3.1	2
227	Floorplan and Power/Ground network co-design using guided incremental floorplanning. , 2009, , .		2
228	FPGA-based acceleration of neural network for ranking in web search engine with a streaming architecture. , 2009, , .		2
229	Cost-Aware Lifetime Yield Analysis of Heterogeneous 3D On-chip Cache. , 2009, , .		2
230	SERSim: a soft error rate simulator and a case study for a 32-bit OpenRisc 1200 microprocessor. International Journal of Electronics, 2010, 97, 441-455.	1.4	2
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