David Z Pan

List of Publications by Year
in descending order

172 papers	3,655 citations	218677 26 h-index	276875 41 g-index
176 all docs	176 docs citations	176 times ranked	2152 citing authors

#	Article	IF	Citations
1	Tutorial and Perspectives on MAGICAL: A Silicon-Proven Open-Source Analog IC Layout System. IEEE Transactions on Circuits and Systems II: Express Briefs, 2023, 70, 715-720.	3.0	1
2	ELight: Toward Efficient and Aging-Resilient Photonic In-Memory Neurocomputing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 820-833.	2.7	1
3	Interactive Analog Layout Editing With Instant Placement and Routing Legalization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 698-711.	2.7	1
4	SqueezeLight: A Multi-Operand Ring-Based Optical Neural Network With Cross-Layer Scalability. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 807-819.	2.7	2
5	An Efficient Analog Circuit Sizing Method Based on Machine Learning Assisted Global Optimization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1209-1221.	2.7	18
6	Identification of 90 NAFLD GWAS loci and establishment of NAFLD PRS and causal role of NAFLD in coronary artery disease. Human Genetics and Genomics Advances, 2022, 3, 100056.	1.7	10
7	elfPlace: Electrostatics-Based Placement for Large-Scale Heterogeneous FPGAs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 155-168.	2.7	11
8	MLCAD: A Survey of Research in Machine Learning for CAD Keynote Paper. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 3162-3181.	2.7	22
9	A Broadband Spectrum Channelizer With PWM-LO-Based Sub-Band Gain Control. IEEE Journal of Solid-State Circuits, 2022, 57, 781-792.	5.4	2
10	Reinforcement Learning for Electronic Design Automation: Case Studies and Perspectives: (Invited) Tj ETQq0 0 0 rgBT /Overlock 10 Tf 50		3
11	DREAMPlaceFPGA: An Open-Source Analytical Placer for Large Scale Heterogeneous FPGAs using Deep-Learning Toolkit. , 2022, , .		5
12	AutoCRAFT: Layout Automation for Custom Circuits in Advanced FinFET Technologies. , 2022, , .		4
13	Light in AI: Toward Efficient Neurocomputing With Optical Neural Networksâ€"A Tutorial. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2581-2585.	3.0	4
14	Long-range chromosomal interactions increase and mark repressed gene expression during adipogenesis. Epigenetics, 2022, 17, 1849-1862.	2.7	1
15	GAN-SRAF: Subresolution Assist Feature Generation Using Generative Adversarial Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 373-385.	2.7	11
16	DREAMPlace: Deep Learning Toolkit-Enabled GPU Acceleration for Modern VLSI Placement. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 748-761.	2.7	51
17	MAGICAL: An Open- Source Fully Automated Analog IC Layout System from Netlist to GDSII. IEEE Design and Test, 2021, 38, 19-26.	1.2	23
18	Toward Hardware-Efficient Optical Neural Networks: Beyond FFT Architecture via Joint Learnability. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1796-1809.	2.7	13

#	Article	IF	Citations
19	O2NN: Optical Neural Networks with Differential Detection-Enabled Optical Operands. , 2021, , .		7
20	SqueezeLight: Towards Scalable Optical Neural Networks with Multi-Operand Ring Resonators. , 2021, , .		14
21	Toward Highâ€Speed and Energyâ€Efficient Computing: A WDMâ€Based Scalable Onâ€Chip Silicon Integrated Optical Comparator. Laser and Photonics Reviews, 2021, 15, 2000275.	8.7	11
22	Identification of TBX15 as an adipose master trans regulator of abdominal obesity genes. Genome Medicine, 2021, 13, 123.	8.2	23
23	Delving into Macro Placement with Reinforcement Learning. , 2021, , .		5
24	An Efficient Automatic Structure Design Method of Silicon-on-Insulator Lateral Power Device Considering RESURF Constraint. IEEE Transactions on Electron Devices, 2021, 68, 4593-4597.	3.0	4
25	Experimental Demonstration of a WDM-based Integrated Optical Decoder for Compact Optical Computing. , 2021, , .		0
26	OpenMPL: An Open-Source Layout Decomposer. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2331-2344.	2.7	7
27	Semisupervised Hotspot Detection With Self-Paced Multitask Learning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 1511-1523.	2.7	14
28	An OTA-Less Second-Order VCO-Based CT $DeltaSigma$ Modulator Using an Inherent Passive Integrator and Capacitive Feedback. IEEE Journal of Solid-State Circuits, 2020, 55, 1337-1350.	5.4	11
29	An Energy-Efficient Comparator With Dynamic Floating Inverter Amplifier. IEEE Journal of Solid-State Circuits, 2020, 55, 1011-1022.	5.4	107
30	A 0.025-mm² 0.8-V 78.5-dB SNDR VCO-Based Sensor Readout Circuit in a Hybrid PLL-$DeltaSigma$ M Structure. IEEE Journal of Solid-State Circuits, 2020, 55, 666-679.	5.4	37
31	Analysis of Microresonator-Based Logic Gate for High-Speed Optical Computing in Integrated Photonics. IEEE Journal of Selected Topics in Quantum Electronics, 2020, 26, 1-8.	2.9	9
32	Sequential Logic and Pipelining in Chip-Based Electronic-Photonic Digital Computing. IEEE Photonics Journal, 2020, 12, 1-11.	2.0	4
33	FLOPS: EFficient On-Chip Learning for OPtical Neural Networks Through Stochastic Zeroth-Order Optimization. , 2020, , .		11
34	Closing the Design Loop: Bayesian Optimization Assisted Hierarchical Analog Layout Synthesis. , 2020, , .		12
35	SHIELDeNN: Online Accelerated Framework for Fault-Tolerant Deep Neural Network Architectures. , 2020, , .		12
36	A 13.5-ENOB, 107-Î¼W Noise-Shaping SAR ADC With PVT-Robust Closed-Loop Dynamic Amplifier. IEEE Journal of Solid-State Circuits, 2020, 55, 3248-3259.	5.4	47

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37	Automatic Selection of Structure Parameters of Silicon on Insulator Lateral Power Device Using Bayesian Optimization. IEEE Electron Device Letters, 2020, 41, 1288-1291.	3.9	14
38	Electronic-photonic arithmetic logic unit for high-speed computing. Nature Communications, 2020, 11, 2154.	12.8	84
39	9.5 A 13.5b-ENOB Second-Order Noise-Shaping SAR with PVT-Robust Closed-Loop Dynamic Amplifier. , 2020, , .		31
40	ABCDPlace: Accelerated Batch-Based Concurrent Detailed Placement on Multithreaded CPUs and GPUs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 5083-5096.	2.7	27
41	ROQ: A Noise-Aware Quantization Scheme Towards Robust Optical Neural Networks with Low-bit Controls. , 2020, , .		9
42	An Energy-Efficient Time-Domain Incremental Zoom Capacitance-to-Digital Converter. IEEE Journal of Solid-State Circuits, 2020, 55, 3064-3075.	5.4	19
43	Powernet: SOI Lateral Power Device Breakdown Prediction With Deep Neural Networks. IEEE Access, 2020, 8, 25372-25382.	4.2	38
44	Virtual-Tile-Based Flip-Flop Alignment Methodology for Clock Network Power Optimization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1256-1268.	3.1	3
45	TimingCamouflage+: Netlist Security Enhancement With Unconventional Timing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4482-4495.	2.7	5
46	Report on the 38th ACM/IEEE International Conference on Computer-Aided Design (ICCAD 2019). IEEE Design and Test, 2020, 37, 121-122.	1.2	0
47	Towards Area-Efficient Optical Neural Networks: An FFT-based Architecture. , 2020, , .		33
48	S³DET: Detecting System Symmetry Constraints for Analog Circuits with Graph Similarity. , 2020, , .		19
49	High-Definition Routing Congestion Prediction for Large-Scale FPGAs. , 2020, , .		35
50	TEMPO: Fast Mask Topography Effect Modeling with Deep Learning. , 2020, , .		11
51	Wavelength-division-multiplexing (WDM)-based integrated electronicâ€“photonic switching network (EPSN) for high-speed data processing and transportation. Nanophotonics, 2020, 9, 4579-4588.	6.0	16
52	An Efficient Training Framework for Reversible Neural Architectures. Lecture Notes in Computer Science, 2020, , 275-289.	1.3	0
53	DREAMPlace 2.0: Open-Source GPU-Accelerated Global and Detailed Placement for Large-Scale VLSI Designs. , 2020, , .		6
54	Integrated WDM-based Optical Comparator for High-speed Computing. , 2020, , .		2

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55	Practical Split Manufacturing Optimization. , 2020, , 9-38.		0
56	Compact Design of On-chip Elman Optical Recurrent Neural Network. , 2020, , .		7
57	Wavelength-division-multiplexing-based electronic-photonic network for high-speed computing (Conference Presentation). , 2020, , .		2
58	DREAMPlace 3.0. , 2020, , .		11
59	Re-examining VLSI manufacturing and yield through the lens of deep learning. , 2020, , .		2
60	Synergistic Topology Generation and Route Synthesis for On-Chip Performance-Critical Signal Groups. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1147-1160.	2.7	7
61	On the Approximation Resiliency of Logic Locking and IC Camouflaging Schemes. IEEE Transactions on Information Forensics and Security, 2019, 14, 347-359.	6.9	46
62	Data Efficient Lithography Modeling With Transfer Learning and Active Data Selection. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1900-1913.	2.7	29
63	A Practical Split Manufacturing Framework for Trojan Prevention via Simultaneous Wire Lifting and Cell Insertion. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1585-1598.	2.7	12
64	WellGAN. , 2019, , .		42
65	On the Impossibility of Approximation-Resilient Circuit Locking. , 2019, , .		28
66	Exploiting Wavelength Division Multiplexing for Optical Logic Synthesis. , 2019, , .		7
67	GAN-SRAF. , 2019, , .		17
68	Breakdown Voltage Prediction of SOI Lateral Power Device Using Deep Neural Network. , 2019, , .		8
69	IP Protection and Supply Chain Security through Logic Obfuscation. ACM Transactions on Design Automation of Electronic Systems, 2019, 24, 1-36.	2.6	61
70	Rethinking Sparsity in Performance Modeling for Analog and Mixed Circuits using Spike and Slab Models. , 2019, , .		5
71	LithoGAN. , 2019, , .		48
72	A shape-driven spreading algorithm using linear programming for global placement. , 2019, , .		1

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73	DREAMPlace. , 2019, , .		56
74	Reverse geneâ€“environment interaction approach to identify variants influencing body-mass index in humans. Nature Metabolism, 2019, 1, 630-642.	11.9	14
75	A New Physical Understanding of Lateral Step Doping Technique via Effective Concentration Profile Concept. IEEE Transactions on Electron Devices, 2019, 66, 2353-2358.	3.0	6
76	Device Layer-Aware Analytical Placement for Analog Circuits. , 2019, , .		15
77	Hardware-software co-design of slimmed optical neural networks. , 2019, , .		25
78	Simultaneous Placement and Clock Tree Construction for Modern FPGAs. , 2019, , .		10
79	FPGA-Accelerated Spreading for Global Placement. , 2019, , .		2
80	GeniusRoute: A New Analog Routing Paradigm Using Generative Neural Network Guidance. , 2019, , .		39
81	elfPlace: Electrostatics-based Placement for Large-Scale Heterogeneous FPGAs. , 2019, , .		19
82	Fully Integrated 20 Gbit/s Silicon Optical Computing Chip for 4-Bit Full Adders. , 2019, , .		0
83	KC2: Key-Condition Crunching for Fast Sequential Circuit Deobfuscation. , 2019, , .		59
84	Power and Accuracy Co-Optimization of an Optical Full Adder via Optimization Algorithms. , 2019, , .		1
85	A New Paradigm for FPGA Placement Without Explicit Packing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 2113-2126.	2.7	18
86	A New Low Turn-Off Loss SOI Lateral Insulated Gate Bipolar Transistor With Buried Variation of Lateral Doping Layer. IEEE Journal of the Electron Devices Society, 2019, 7, 62-69.	2.1	6
87	Provably Secure Camouflaging Strategy for IC Protection. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1399-1412.	2.7	32
88	Machine Learning in Physical Verification, Mask Synthesis, and Physical Design. , 2019, , 95-115.		4
89	MAGICAL: Toward Fully Automated Analog IC Layout Leveraging Human and Machine Intelligence: Invited Paper. , 2019, , .		39
90	Lithography hotspot detection using a double inception module architecture. Journal of Micro/ Nanolithography, MEMS, and MOEMS, 2019, 18, 1.	0.9	12

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91	SoulNet: ultrafast optical source optimization utilizing generative neural networks for advanced lithography. Journal of Micro/ Nanolithography, MEMS, and MOEMS, 2019, 18, 1.	0.9	2
92	Integration of human adipocyte chromosomal interactions with adipose gene expression prioritizes obesity-related genes from GWAS. Nature Communications, 2018, 9, 1512.	12.8	75
93	A New Physical Insight for the 3-D-Layout-Induced Cylindrical Breakdown in Lateral Power Devices on SOI Substrate. IEEE Transactions on Electron Devices, 2018, 65, 1843-1848.	3.0	6
94	MrDP: Multiple-Row Detailed Placement of Heterogeneous-Sized Cells for Advanced Nodes. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1237-1250.	2.7	21
95	Thermal Stress and Reliability Analysis of TSV-Based 3-D ICs With a Novel Adaptive Strategy Finite Element Method. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1312-1325.	3.1	8
96	Effective Doping Concentration Theory: A New Physical Insight for the Double-RESURF Lateral Power Devices on SOI Substrate. IEEE Transactions on Electron Devices, 2018, 65, 648-654.	3.0	23
97	A Novel Variation of Lateral Doping Technique in SOI LDMOS With Circular Layout. IEEE Transactions on Electron Devices, 2018, 65, 1447-1452.	3.0	21
98	Comparison of microrings and microdisks for high-speed optical modulation in silicon photonics. Applied Physics Letters, 2018, 112, 111108.	3.3	27
99	Logic synthesis for energy-efficient photonic integrated circuits. , 2018, , .		12
100	TILA-S: Timing-Driven Incremental Layer Assignment Avoiding Slew Violations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 231-244.	2.7	14
101	UTPlaceF: A Routability-Driven FPGA Placer With Physical and Congestion Aware Packing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 869-882.	2.7	47
102	Interlayer Cooling Network Design for High-Performance 3D ICs Using Channel Patterning and Pruning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 770-781.	2.7	8
103	Machine Learning for Yield Learning and Optimization. , 2018, , .		13
104	TimingSAT: Decamouflaging Timing-based Logic Obfuscation. , 2018, , .		12
105	Effective Concentration Profile: Mechanism of Gate Field-Plate Assistant Effect in SOI Lateral Power Devices. IEEE Transactions on Electron Devices, 2018, 65, 4476-4482.	3.0	8
106	GDP: GPU accelerated Detailed Placement. , 2018, , .		11
107	Role of Shape Factor in Forming Surface Electric Field Basin in RESURF Lateral Power Devices and its Optimization Design. IEEE Journal of the Electron Devices Society, 2018, 6, 1147-1153.	2.1	5
108	Directed self-assembly for advanced chips. Nature Electronics, 2018, 1, 530-531.	26.0	6

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109	A 13-ENOB Second-Order Noise-Shaping SAR ADC Realizing Optimized NTF Zeros Using the Error-Feedback Structure. IEEE Journal of Solid-State Circuits, 2018, 53, 3484-3496.	5.4	80
110	UTPlaceF 2.0. ACM Transactions on Design Automation of Electronic Systems, 2018, 23, 1-23.	2.6	17
111	Layout Synthesis for Topological Quantum Circuits With 1-D and 2-D Architectures. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1574-1587.	2.7	7
112	Silicon microdisk-based full adders for optical computing. Optics Letters, 2018, 43, 983.	3.3	47
113	An Improved Domain Decomposition Method for Drop Impact Reliability Analysis of 3-D ICs. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2018, 8, 1788-1799.	2.5	2
114	TimingCamouflage: Improving circuit security against counterfeiting by unconventional timing. , 2018, , .		29
115	Subresolution Assist Feature Generation With Supervised Data Learning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1225-1236.	2.7	15
116	Cut Redistribution and Insertion for Advanced 1-D Layout Design via Network Flow Optimization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1613-1626.	3.1	0
117	Automated logic synthesis for electro-optic logic-based integrated optical computing. Optics Express, 2018, 26, 28002.	3.4	27
118	Triple Patterning Aware Detailed Placement Toward Zero Cross-Row Middle-of-Line Conflict. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1140-1152.	2.7	9
119	Redundant Local-Loop Insertion for Unidirectional Routing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1113-1125.	2.7	3
120	Triple/quadruple patterning layout decomposition via linear programming and iterative rounding. Journal of Micro/ Nanolithography, MEMS, and MOEMS, 2017, 16, 023507.	0.9	8
121	Incremental Layer Assignment Driven by an External Signoff Timing Engine. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1126-1139.	2.7	4
122	High Performance Dummy Fill Insertion With Coupling and Uniformity Constraints. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1532-1544.	2.7	10
123	Cyclic Obfuscation for Creating SAT-Unresolvable Circuits. , 2017, , .		116
124	AppSAT: Approximately deobfuscating integrated circuits. , 2017, , .		215
125	Optical computing on silicon-on-insulator-based photonic integrated circuits. , 2017, , .		7
126	Provably secure camouflaging strategy for IC protection. , 2016, , .		73

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127	A Novel 3-D Analytical Method for Curvature Effect-Induced Electric Field Crowding in SOI Lateral Power Device. IEEE Transactions on Electron Devices, 2016, 63, 4359-4365.	3.0	8
128	Polynomial Time Algorithm for Area and Power Efficient Adder Synthesis in High-Performance Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 820-831.	2.7	14
129	CSL: Coordinated and scalable logic synthesis techniques for effective NBTI reduction. , 2015, , .		2
130	Self-Aligned Double Patterning Aware Pin Access and Standard Cell Layout Co-Optimization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 699-712.	2.7	38
131	Methodology for Standard Cell Compliance and Detailed Placement for Triple Patterning Lithography. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 726-739.	2.7	33
132	Layout Decomposition for Triple Patterning Lithography. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 433-446.	2.7	54
133	Clock Tree Resynthesis for Multi-Corner Multi-Mode Timing Closure. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 589-602.	2.7	26
134	Polynomial time algorithm for area and power efficient adder synthesis in high-performance designs. , 2015, , .		5
135	Pushing multiple patterning in sub-10nm. , 2015, , .		26
136	Evolving challenges and techniques for nanometer SoC clock network synthesis. , 2014, , .		5
137	Electromigration Study for Multiscale Power/Ground Vias in TSV-Based 3-D ICs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1873-1885.	2.7	12
138	Triple patterning lithography layout decomposition using end-cutting. Journal of Micro/Nanolithography, MEMS, and MOEMS, 2014, 14, 011002.	0.9	12
139	Towards Optimal Performance-Area Trade-Off in Adders by Synthesis of Parallel Prefix Structures. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1517-1530.	2.7	27
140	Reliability Aware Gate Sizing Combating NBTI and Oxide Breakdown. , 2014, , .		10
141	An accurate semi-analytical framework for full-chip TSV-induced stress modeling. , 2013, , .		1
142	Design for Manufacturing With Emerging Nanolithography. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 1453-1472.	2.7	100
143	Chemical-Mechanical Polishing-Aware Application-Specific 3D NoC Design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 940-951.	2.7	0
144	Impact of Mechanical Stress on the Full Chip Timing for Through-Silicon-Via-based 3-D ICs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 905-917.	2.7	14

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145	Skew Management of NBTI Impacted Gated Clock Trees. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 918-927.	2.7	6
146	A high-performance triple patterning layout decomposer with balanced density. , 2013, , .		35
147	Robust and resilient designs from the bottom-up: Technology, CAD, circuit, and system issues. , 2012, , .		12
148	TSV Stress-Aware Full-Chip Mechanical Reliability Analysis and Optimization for 3-D IC. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1194-1207.	2.7	44
149	UNISM: Unified Scheduling and Mapping for General Networks on Chip. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1496-1509.	3.1	49
150	E-Beam Lithography Stencil Planning and Optimization With Overlapped Characters. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 167-179.	2.7	32
151	Electromigration modeling and full-chip reliability analysis for BEOL interconnect in TSV-based 3D ICs. , 2011, , .		28
152	CELONCEL: Effective design technique for 3-D monolithic integration targeting high performance integrated circuits. , 2011, , .		36
153	A fast simulation framework for full-chip thermo-mechanical stress and reliability analysis of through-silicon-via based 3D ICs. , 2011, , .		11
154	Doppler: DPL-aware and OPC-friendly gridless detailed routing with mask density balancing. , 2011, , .		0
155	Modeling of electromigration in through-silicon-via based 3D IC. , 2011, , .		47
156	A Voltage-Frequency Island Aware Energy Optimization Framework for Networks-on-Chip. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2011, 1, 420-432.	3.6	30
157	Application-Aware NoC Design for Efficient SDRAM Access. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 1521-1533.	2.7	12
158	TSV stress aware timing analysis with applications to 3D-IC layout optimization. , 2010, , .		90
159	Stress-driven 3D-IC placement with TSV keep-out zone and regularity study. , 2010, , .		60
160	A3MAP: Architecture-Aware Analytic Mapping for Networks-on-Chip. , 2010, , .		11
161	Double Patterning Layout Decomposition for Simultaneous Conflict and Stitch Minimization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 185-196.	2.7	57
162	Stress Aware Layout Optimization Leveraging Active Area Dependent Mobility Enhancement. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1533-1545.	2.7	3

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163	Voltage and frequency island optimizations for many-core/networks-on-chip designs. , 2010, , .		4
164	A High-Performance Droplet Routing Algorithm for Digital Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1714-1724.	2.7	119
165	DPlace2.0: A stable and efficient analytical placement based on diffusion. , 2008, , .		2
166	Synthetic Biology Design and Analysis: A Case Study of Frequency Entrained Biological Clock. , 2008, , .		0
167	Fast Substrate Noise Aware Floorplanning for Mixed Signal SOC Designs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 1713-1717.	3.1	2
168	A Voltage-Frequency Island aware energy optimization framework for networks-on-chip. , 2008, , .		4
169	Layout Level Timing Optimization by Leveraging Active Area Dependent Mobility of Strained-Silicon Devices. , 2008, , .		5
170	TIP-OPC: a new topological invariant paradigm for pixel based optical proximity correction. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	1
171	Diffusion-Based Placement Migration With Application on Legalization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 2158-2172.	2.7	11
172	A novel intensity based optical proximity correction algorithm with speedup in lithography simulation. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	4