Subhasish Mitra

List of Publications by Year
in descending order

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296	12,375	41344	46799
papers	citations	49 h-index	89 g-index

301	301	301	7326
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Logic Bug Detection and Localization Using Symbolic Quick Error Detection. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2024, , 1-1.	2.7	12
2	An Exhaustive Approach to Detecting Transient Execution Side Channels in RTL Designs of Processors. IEEE Transactions on Computers, 2023, 72, 222-235.	3.4	8
3	Dynamics of a single bubble rising in a quiescent medium. Experimental Thermal and Fluid Science, 2022, 132, 110546.	2.7	7
4	Bandgap Extraction at 10 K to Enable Leakage Control in Carbon Nanotube MOSFETs. IEEE Electron Device Letters, 2022, 43, 490-493.	3.9	11
5	Effect of turbulence dispersion on bubble-particle collision efficiency. Minerals Engineering, 2022, 177, 107374.	4.3	9
6	CHIMERA: A 0.92-TOPS, 2.2-TOPS/W Edge AI Accelerator With 2-MByte On-Chip Foundry Resistive RAM for Efficient Training and Inference. IEEE Journal of Solid-State Circuits, 2022, 57, 1013-1026.	5.4	15
7	Numerical Study into Gravity Separation of Phosphorus from BOS Slag during Solidification. ISIJ International, 2021, 61, 705-714.	1.4	2
8	Four-Bits-Per-Memory One-Transistor-and-Eight-Resistive-Random-Access-Memory (1T8R) Array. IEEE Electron Device Letters, 2021, 42, 335-338.	3.9	21
9	Iron Ore Sintering in Milli-Pot: Comparison to Pilot Scale and Identification of Maximum Resistance to Air Flow. ISIJ International, 2021, 61, 1469-1478.	1.4	2
10	CHIMERA: A 0.92 TOPS, 2.2 TOPS/W Edge AI Accelerator with 2 MByte On-Chip Foundry Resistive RAM for Efficient Training and Inference. , 2021, , .		28
11	Split-Chip Design to Prevent IP Reverse Engineering. IEEE Design and Test, 2021, 38, 109-118.	1.2	5
12	Determining Drag Coefficient of Simplified Dendritic Particles in Metallurgical Systems. Metallurgical and Materials Transactions A: Physical Metallurgy and Materials Science, 2021, 52, 4841.	2.2	2
13	RADAR: A Fast and Energy-Efficient Programming Technique for Multiple Bits-Per-Cell RRAM Arrays. IEEE Transactions on Electron Devices, 2021, 68, 4397-4403.	3.0	24
14	Illusion of large on-chip memory by networked computing chips for neural network inference. Nature Electronics, 2021, 4, 71-80.	26.0	15
15	Direct visualisation of bubble-particle interactions in presence of cavitation bubbles in an ultrasonic flotation cell. Minerals Engineering, 2021, 174, 107258.	4.3	18
16	Effect of bubble surface loading on bubble rise velocity. Minerals Engineering, 2021, 174, 107252.	4.3	5
17	Spatially patterned bi-electrode epiretinal stimulation for axon avoidance at cellular resolution. Journal of Neural Engineering, 2021, 18, 066007.	3.5	9
18	Cross-Layer Resilience Against Soft Errors: Key Insights. Embedded Systems, 2021, , 249-275.	0.6	0

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19	Automatic Identification of Axon Bundle Activation for Epiretinal Prosthesis. IEEE Transactions on Neural Systems and Rehabilitation Engineering, 2021, 29, 2496-2502.	4.9	9
20	Analysis of particle dispersion coefficient in solid-liquid fluidised beds. Powder Technology, 2020, 365, 60-73.	4.2	9
21	Estimation of dispersion coefficient in a solid-liquid fluidised bed system. Powder Technology, 2020, 374, 560-576.	4.2	6
22	Development of a flotation recovery model with CFD predicted collision efficiency. Minerals Engineering, 2020, 159, 106615.	4.3	15
23	A 35.6 TOPS/W/mmÂ² 3-Stage Pipelined Computational SRAM With Adjustable Form Factor for Highly Data-Centric Applications. IEEE Solid-State Circuits Letters, 2020, 3, 286-289.	2.0	10
24	Molybdenum oxide on carbon nanotube: Doping stability and correlation with work function. Journal of Applied Physics, 2020, 128, 045111.	2.5	6
25	A Formal Approach for Detecting Vulnerabilities to Transient Execution Attacks in Out-of-Order Processors. , 2020, , .		14
26	Sensory Particles with Optical Telemetry. , 2020, , .		1
27	Hyperdimensional computing nanosystem: in-memory computing using monolithic 3D integration of RRAM and CNFET. , 2020, , 195-219.		2
28	A Density Metric for Semiconductor Technology [Point of View]. Proceedings of the IEEE, 2020, 108, 478-482.	21.3	25
29	Reconfigurable tiles of computing-in-memory SRAM architecture for scalable vectorization. , 2020, , .		7
30	Pressure-drop Modelling in the Softening and Melting Test for Ferrous Burden. ISIJ International, 2020, 60, 1416-1426.	1.4	6
31	A-QED Verification of Hardware Accelerators. , 2020, , .		6
32	Sub-0.5 nm Interfacial Dielectric Enables Superior Electrostatics: 65 mV/dec Top-Gated Carbon Nanotube FETs at 15 nm Gate Length. , 2020, , .		14
33	Heterogeneous 3D Nano-systems: The N3XT Approach?. The Frontiers Collection, 2020, , 127-151.	0.2	6
34	DECOY: DEflection-Driven HLS-Based Computation Partitioning for Obfuscating Intellectual PropertY. , 2020, , .		17
35	Hybrid Quick Error Detection: Validation and Debug of SoCs Through High-Level Synthesis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1345-1358.	2.7	1
36	Beyond-Silicon Devices: Considerations for Circuits and Architectures. , 2019, , 1-19.		0

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37	A Data-Compressive Wired-OR Readout for Massively Parallel Neural Recording. IEEE Transactions on Biomedical Circuits and Systems, 2019, 13, 1128-1140.	4.0	17
38	Review of Methodologies for Pre- and Post-Silicon Analog Verification in Mixed-Signal SOCs. , 2019, , .		8
39	Optimization of Electrical Stimulation for a High-Fidelity Artificial Retina. , 2019, , .		24
40	Low-Temperature Side Contact to Carbon Nanotube Transistors: Resistance Distributions Down to 10 nm Contact Length. Nano Letters, 2019, 19, 1083-1089.	9.1	42
41	Cross-Layer Resilience. , 2019, , .		5
42	Processor Hardware Security Vulnerabilities and their Detection by Unique Program Execution Checking. , 2019, , .		22
43	A Data-Compressive Wired-OR Readout for Massively Parallel Neural Recording. , 2019, , .		5
44	14.3 A 43pJ/Cycle Non-Volatile Microcontroller with 4.7Î¼s Shutdown/Wake-up Integrating 2.3-bit/Cell Resistive RAM and Resilience Techniques. , 2019, , .		13
45	Resistive RAM Endurance: Array-Level Characterization and Correction Techniques Targeting Deep Learning Applications. IEEE Transactions on Electron Devices, 2019, 66, 1281-1288.	3.0	43
46	Symbolic QED Pre-silicon Verification for Automotive Microcontroller Cores: Industrial Case Study. , 2019, , .		3
47	Unlocking the Power of Formal Hardware Verification with CoSA and Symbolic QED: Invited Paper. , 2019, , .		0
48	High-Density Multiple Bits-per-Cell 1T4R RRAM Array with Gradual SET/RESET and its Effectiveness for Deep Learning. , 2019, , .		35
49	Monolithic 3-D Integration. IEEE Micro, 2019, 39, 16-27.	1.8	24
50	Memory Sizing of a Scalable SRAM In-Memory Computing Tile Based Architecture. , 2019, , .		17
51	The N3XT Approach to Energy-Efficient Abundant-Data Computing. Proceedings of the IEEE, 2019, 107, 19-48.	21.3	71
52	Analysis of dynamic interactions in a bubble-particle system in presence of an acoustic field. Minerals Engineering, 2019, 131, 111-123.	4.3	6
53	Resistive RAM With Multiple Bits Per Cell: Array-Level Demonstration of 3 Bits Per Cell. IEEE Transactions on Electron Devices, 2019, 66, 641-646.	3.0	43
54	Modulation of turbulent flow field in an oscillating grid system owing to single bubble rise. Chemical Engineering Science, 2018, 185, 26-49.	3.8	13

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55	Tolerating Soft Errors in Processor Cores Using CLEAR (Cross-Layer Exploration for Architecting) Tj ETQq1 1 0.784314 rgBT /Overlock 10 1839-1852.	2.7	14
56	Brain-inspired computing exploiting carbon nanotube FETs and resistive RAM: Hyperdimensional computing case study. , 2018, , .		84
57	Evaporation of a suspended binary mixture droplet in a heated flowing gas stream. Experimental Thermal and Fluid Science, 2018, 91, 329-344.	2.7	17
58	A Novel Measurement of Voidage in Coke and Ferrous Layers in Softening and Melting under Load Test Using Synchrotron X-ray and Neutron Computed Tomography. ISIJ International, 2018, 58, 2150-2152.	1.4	6
59	Hyperdimensional Computing Exploiting Carbon Nanotube FETs, Resistive RAM, and Their Monolithic 3D Integration. IEEE Journal of Solid-State Circuits, 2018, 53, 3183-3196.	5.4	49
60	Understanding Energy Efficiency Benefits of Carbon Nanotube Field-Effect Transistors for Digital VLSI. IEEE Nanotechnology Magazine, 2018, 17, 1259-1269.	2.0	87
61	TRIG: Hardware Accelerator for Inference-Based Applications and Experimental Demonstration Using Carbon Nanotube FETs. , 2018, , .		3
62	ETISS-ML: A multi-level instruction set simulator with RTL-level fault injection support for the evaluation of cross-layer resiliency techniques. , 2018, , .		7
63	Effect of bubble on the pressure spectra of oscillating grid turbulent flow at low Taylor-Reynolds number. Chemical Engineering Science, 2018, 190, 28-39.	3.8	7
64	TRIG. , 2018, , .		6
65	Dynamic Surface Wetting and Heat Transfer in a Droplet-Particle System of Less Than Unity Size Ratio. Frontiers in Chemistry, 2018, 6, 259.	3.6	22
66	Symbolic quick error detection using symbolic initial state for pre-silicon verification. , 2018, , .		9
67	Coming Up N3XT, After 2D Scaling of Si CMOS. , 2018, , .		7
68	A review of CFD modelling studies on the flotation process. Minerals Engineering, 2018, 127, 153-177.	4.3	73
69	Evaporation of a sessile binary droplet on a heated spherical particle. Experimental Thermal and Fluid Science, 2018, 99, 558-571.	2.7	14
70	Segregation and dispersion studies in binary solid-liquid fluidised beds: A theoretical and computational study. Powder Technology, 2017, 314, 400-411.	4.2	22
71	System-Level Effects of Soft Errors in Uncore Components. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1497-1510.	2.7	13
72	Settling/rising of a foreign particle in solid-liquid fluidized beds: Application of dynamic mesh technique. Chemical Engineering Science, 2017, 170, 139-153.	3.8	12

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73	Hysteresis-Free Carbon Nanotube Field-Effect Transistors. ACS Nano, 2017, 11, 4785-4791.	14.6	50
74	Resistive RAM-Centric Computing: Design and Modeling Methodology. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2263-2273.	5.4	61
75	Activation of ganglion cells and axon bundles using epiretinal electrical stimulation. Journal of Neurophysiology, 2017, 118, 1457-1471.	1.8	64
76	Interactions in droplet and particle system of near unity size ratio. Chemical Engineering Science, 2017, 170, 154-175.	3.8	40
77	Edward J. McCluskey 1929-2016. IEEE Design and Test, 2017, 34, 94-98.	1.2	1
78	Expansion behaviour of a binary solid-liquid fluidised bed with different solid mass ratio. Advanced Powder Technology, 2017, 28, 3111-3129.	4.1	21
79	3D nanosystems enable embedded abundant-data computing. , 2017, , .		6
80	E-QED: Electrical Bug Localization During Post-silicon Validation Enabled by Quick Error Detection and Formal Methods. Lecture Notes in Computer Science, 2017, , 104-125.	1.3	7
81	A Systems Approach to Computing in Beyond CMOS Fabrics. , 2017, , .		1
82	Interaction of a spherical particle with a neutrally buoyant immiscible droplet in salt solution. Chemical Engineering Science, 2017, 172, 182-198.	3.8	10
83	Three-dimensional integration of nanotechnologies for computing and data storage on a single chip. Nature, 2017, 547, 74-78.	27.8	577
84	Carbon Nanotubes for Monolithic 3D ICs. , 2017, , 315-333.		2
85	Cross-Layer Resilience in Low-Voltage Digital Systems: Key Insights. , 2017, , .		3
86	Resilience in next-generation embedded systems*. , 2017, , 295-334.		0
87	A review of the mechanisms and models of bubble-particle detachment in froth flotation. Separation and Purification Technology, 2016, 170, 155-172.	7.9	111
88	Transforming nanodevices into nanosystems: The N3XT 1,000X. , 2016, , .		0
89	Computing with Carbon Nanotubes. IEEE Spectrum, 2016, 53, 26-52.	0.7	7
90	Nano-engineered architectures for ultra-low power wireless body sensor nodes. , 2016, , .		7

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91	Transforming nanodevices to next generation nanosystems. , 2016, , .		0
92	Hyperdimensional computing with 3D VRRAM in-memory kernels: Device-architecture co-design for energy-efficient, error-resilient language recognition. , 2016, , .		95
93	Interaction dynamics of a spherical particle with a suspended liquid film. AICHE Journal, 2016, 62, 295-314.	3.6	15
94	On wetting characteristics of droplet on a spherical particle in film boiling regime. Chemical Engineering Science, 2016, 149, 181-203.	3.8	61
95	CLEAR. , 2016, , .		45
96	Experimental investigation on modulation of homogeneous and isotropic turbulence in the presence of single particle using time-resolved PIV. Chemical Engineering Science, 2016, 153, 308-329.	3.8	17
97	Symbolic Quick Error Detection for Pre-Silicon and Post-Silicon Validation: Frequently Asked Questions. IEEE Design and Test, 2016, 33, 55-62.	1.2	0
98	Low-power, high-performance S-NDR oscillators for stereo (3D) vision using directly-coupled oscillator networks. , 2016, , .		8
99	Hysteresis in Carbon Nanotube Transistors: Measurement and Analysis of Trap Density, Energy Level, and Spatial Distribution. ACS Nano, 2016, 10, 4599-4608.	14.6	62
100	Time-Based Sensor Interface Circuits in CMOS and Carbon Nanotube Technologies. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 577-586.	5.4	20
101	TPAD: Hardware Trojan Prevention and Detection for Trusted Integrated Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 521-534.	2.7	79
102	Efficient metallic carbon nanotube removal for highly-scaled technologies. , 2015, , .		25
103	Efficient Soft Error Vulnerability Estimation of Complex Designs. , 2015, , .		14
104	Monolithic 3D Integration: A Path from Concept to Reality. , 2015, , .		31
105	Quick Error Detection Tests with Fast Runtimes for Effective Post-Silicon Validation and Debug. , 2015, , .		11
106	Partitioning Electrostatic and Mechanical Domains in Nanoelectromechanical Relays. Journal of Microelectromechanical Systems, 2015, 24, 592-598.	2.5	8
107	Rapid Co-Optimization of Processing and Circuit Design to Overcome Carbon Nanotube Variations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1082-1095.	2.7	36
108	A structured approach to post-silicon validation and debug using symbolic quick error detection. , 2015, , .		13

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109	From nanodevices to nanosystems: The N3XT information technology. , 2015, , .		0
110	High performance, integrated 1T1R oxide-based oscillator: Stack engineering for low-power operation in neural network applications. , 2015, , .		9
111	From nanodevices to nanosystems: The N3XT information technology. , 2015, , .		1
112	New Logic Synthesis as Nanotechnology Enabler. Proceedings of the IEEE, 2015, 103, 2168-2195.	21.3	53
113	Energy-Efficient Abundant-Data Computing: The N3XT 1,000x. Computer, 2015, 48, 24-33.	1.1	156
114	NSF expedition on variability-aware software: Recent results and contributions. IT - Information Technology, 2015, 57, 181-198.	0.9	10
115	Collision behaviour of a smaller particle into a larger stationary droplet. Advanced Powder Technology, 2015, 26, 280-295.	4.1	41
116	The Trojan-proof chip. IEEE Spectrum, 2015, 52, 46-51.	0.7	38
117	Comparison of vaporization models for feed droplet in fluid catalytic cracking risers. Chemical Engineering Research and Design, 2015, 101, 82-97.	5.6	16
118	Comparison of specific energy dissipation rate calculation methodologies utilising 2D PIV velocity measurement. Chemical Engineering Science, 2015, 137, 752-767.	3.8	24
119	Modelling the Motion of a Collected Particle over a Bubble Surface. Procedia Engineering, 2015, 102, 1346-1355.	1.2	8
120	Multiple Independent Gate FETs: How many gates do we need?. , 2015, , .		7
121	Hybrid quick error detection (H-QED). , 2015, , .		13
122	Understanding soft errors in uncore components. , 2015, , .		17
123	Instantaneous bond number for a particle detaching from a bubble. International Journal of Mineral Processing, 2015, 142, 22-29.	2.6	8
124	Time-based sensor interface circuits in carbon nanotube technology. , 2015, , .		1
125	Evaporation of a droplet on a heated spherical particle. Chemical Engineering Journal, 2015, 278, 309-319.	12.7	28
126	Monolithic 3D integration advances and challenges: From technology to system levels. , 2014, , .		17

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127	Robust design and experimental demonstrations of carbon nanotube digital circuits. , 2014, , .		3
128	System Level Benchmarking with Yield-Enhanced Standard Cell Library for Carbon Nanotube VLSI Circuits. ACM Journal on Emerging Technologies in Computing Systems, 2014, 10, 1-19.	2.3	8
129	Guest Editorial: Robust and energy-secure systems. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2014, 4, 165-168.	3.6	0
130	Addressing failures in exascale computing. International Journal of High Performance Computing Applications, 2014, 28, 129-173.	3.7	265
131	QED post-silicon validation and debug: Invited abstract. , 2014, , .		0
132	Monolithic 3D integration of logic and memory: Carbon nanotube FETs, resistive RAM, and silicon FETs. , 2014, , .		105
133	High-performance carbon nanotube field-effect transistors. , 2014, , .		37
134	Sensor-to-Digital Interface Built Entirely With Carbon Nanotube FETs. IEEE Journal of Solid-State Circuits, 2014, 49, 190-201.	5.4	101
135	Rethinking error injection for effective resilience. , 2014, , .		10
136	Effective Post-Silicon Validation of System-on-Chips Using Quick Error Detection. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1573-1590.	2.7	38
137	The resilience wall: Cross-layer solution strategies. , 2014, , .		12
138	QED post-silicon validation and debug: Frequently asked questions. , 2014, , .		4
139	Carbon nanotubes for high-performance logic. MRS Bulletin, 2014, 39, 719-726.	3.5	11
140	Carbon Nanotube Circuit Integration up to Sub-20 nm Channel Lengths. ACS Nano, 2014, 8, 3434-3443.	14.6	70
141	Monolithic three-dimensional integration of carbon nanotube FETs with silicon CMOS. , 2014, , .		21
142	Modelling of the interaction between a falling n-heptane droplet and hot solid surface. Chemical Engineering Science, 2014, 116, 23-37.	3.8	7
143	Detachment of a bubble anchored to a vertical cylindrical surface in quiescent liquid and grid generated turbulence. Canadian Journal of Chemical Engineering, 2014, 92, 2067-2077.	1.7	9
144	Quantitative evaluation of soft error injection techniques for robust system design. , 2013, , .		172

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145	Reliability of graphene interconnects and n-type doping of carbon nanotube transistors. , 2013, , .		0
146	Self-repair of uncore components in robust system-on-chips: An OpenSPARC T2 case study. , 2013, , .		17
147	Overcoming Post-Silicon Validation Challenges through Quick Error Detection (QED). , 2013, , .		6
148	Early-life-failure detection using SAT-based ATPG. , 2013, , .		16
149	Combinational Logic Design Using Six-Terminal NEM Relays. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 653-666.	2.7	32
150	Laterally actuated nanoelectromechanical relays with compliant, low resistance contact. , 2013, , .		4
151	Carbon nanotube computer. Nature, 2013, 501, 526-530.	27.8	903
152	Carbon Nanotube Circuits: Opportunities and Challenges. , 2013, , .		3
153	Detection of early-life failures in high-K metal-gate transistors and ultra low-K inter-metal dielectrics. , 2013, , .		6
154	Experimental demonstration of a fully digital capacitive sensor interface built entirely using carbon-nanotube FETs. , 2013, , .		18
155	Droplet impact dynamics on a spherical particle. Chemical Engineering Science, 2013, 100, 105-119.	3.8	122
156	Laterally Actuated Platinum-Coated Polysilicon NEM Relays. Journal of Microelectromechanical Systems, 2013, 22, 768-778.	2.5	34
157	Rapid exploration of processing and design guidelines to overcome carbon nanotube variations. , 2013, , .		14
158	Sacha. , 2013, , .		8
159	Dual-beam, six-terminal nanoelectromechanical relays. , 2013, , .		0
160	Monolithic three-dimensional integration of carbon nanotube FET complementary logic circuits. , 2013, , .		19
161	Carbon nanotube imperfection-immune digital VLSI. , 2013, , .		0
162	Single-Tube Characterization Methodology for Experimental and Analytical Evaluation of Carbon Nanotube Synthesis. Japanese Journal of Applied Physics, 2012, 51, 04DB02.	1.5	0

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163	Quick detection of difficult bugs for effective post-silicon validation. , 2012, , .		24
164	Cooling three-dimensional integrated circuits using power delivery networks. , 2012, , .		28
165	Wafer-Scale Fabrication and Characterization of Thin-Film Transistors with Polythiophene-Sorted Semiconducting Carbon Nanotube Networks. ACS Nano, 2012, 6, 451-458.	14.6	50
166	Nano-Electro-Mechanical relays for FPGA routing: Experimental demonstration and a design technique. , 2012, , .		28
167	Template Patterning: Flexible Control of Block Copolymer Directed Self-Assembly using Small, Topographical Templates: Potential Lithography Solution for Integrated Circuit Contact Hole Patterning (Adv. Mater. 23/2012). Advanced Materials, 2012, 24, 3082-3082.	21.0	2
168	ERSA: Error Resilient System Architecture for Probabilistic Applications. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 546-558.	2.7	77
169	Carbon Nanotube Robust Digital VLSI. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 453-471.	2.7	104
170	Single-Tube Characterization Methodology for Experimental and Analytical Evaluation of Carbon Nanotube Synthesis. Japanese Journal of Applied Physics, 2012, 51, 04DB02.	1.5	0
171	Integration of nanoelectromechanical (NEM) relays with silicon CMOS with functional CMOS-NEM circuit. , 2011, , .		49
172	Overcoming carbon nanotube variations through co-optimized technology and circuit design. , 2011, , .		27
173	Carbon nanotube electronics - Materials, devices, circuits, design, modeling, and performance projection. , 2011, , .		22
174	Scalable Carbon Nanotube Computational and Storage Circuits Immune to Metallic and Mispositioned Carbon Nanotubes. IEEE Nanotechnology Magazine, 2011, 10, 744-750.	2.0	54
175	The case for RAMCloud. Communications of the ACM, 2011, 54, 121-130.	4.5	119
176	Architecture and performance evaluation of 3D CMOS-NEM FPGA. , 2011, , .		10
177	Linear Increases in Carbon Nanotube Density Through Multiple Transfer Technique. Nano Letters, 2011, 11, 1881-1886.	9.1	69
178	Robust System Design to Overcome CMOS Reliability Challenges. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2011, 1, 30-41.	3.6	60
179	Characterization and Implementation of Fault-Tolerant Vertical Links for 3-D Networks-on-Chip. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 124-134.	2.7	54
180	Self-Tuning for Maximized Lifetime Energy-Efficiency in the Presence of Circuit Aging. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 760-773.	2.7	79

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181	Characterization and Design of Logic Circuits in the Presence of Carbon Nanotube Density Variations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 1103-1113.	2.7	41
182	Robust System Design. IPSJ Transactions on System LSI Design Methodology, 2011, 4, 2-30.	0.8	4
183	The effect of amine protonation on the electrical properties of spin-assembled single-walled carbon nanotube networks. Nanotechnology, 2011, 22, 125201.	2.6	9
184	Dual sidewall lateral nanoelectromechanical relays with beam isolation. , 2011, , .		9
185	Carbon electronics — From material synthesis to circuit demonstration. , 2011, , .		1
186	Air-stable technique for fabricating n-type carbon nanotube FETs. , 2011, , .		10
187	Carbon nanotube imperfection-immune digital VLSI: Frequently asked questions updated. , 2011, , .		4
188	Imperfection-Immune Carbon Nanotube VLSI Circuits. , 2011, , 277-305.		2
189	Carbon nanotube correlation. , 2010, , .		48
190	Post-silicon validation opportunities, challenges and recent advances. , 2010, , .		116
191	BLoG. , 2010, , .		30
192	ACCNT: A Metallic-CNT-Tolerant Design Methodology for Carbon Nanotube VLSI: Analyses and Design Guidelines. IEEE Transactions on Electron Devices, 2010, 57, 2284-2295.	3.0	22
193	Carbon nanotube circuits: Living with imperfections and variations. , 2010, , .		11
194	Cross-layer resilience challenges: Metrics and optimization. , 2010, , .		24
195	Gate-oxide early-life failure identification using delay shifts. , 2010, , .		8
196	Cross-layer error resilience for robust systems. , 2010, , .		15
197	The case for RAMClouds. Operating Systems Review (ACM), 2010, 43, 92-105.	1.9	344
198	Robust System Design. , 2010, , .		8

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199	Design and Validation of Robust Systems. , 2010, , .		1
200	Efficient FPGAs using nanoelectromechanical relays. , 2010, , .		62
201	Concurrent autonomous self-test for uncore components in system-on-chips. , 2010, , .		25
202	Titanium nitride sidewall stringer process for lateral nanoelectromechanical relays. , 2010, , .		8
203	ERSA: Error Resilient System Architecture for probabilistic applications. , 2010, , .		145
204	Efficient metallic carbon nanotube removal readily scalable to wafer-level VLSI CNFET circuits. , 2010, , .		27
205	Optimized self-tuning for circuit aging. , 2010, , .		19
206	Low-cost gate-oxide early-life failure detection in robust systems. , 2010, , .		32
207	QED: Quick Error Detection tests for effective post-silicon validation. , 2010, , .		54
208	Experimental study of gate oxide early-life failures. Reliability Physics Symposium, 2009 IEEE International, 2009, , .	0.0	19
209	Carbon nanotube circuits in the presence of carbon nanotube density variations. , 2009, , .		70
210	Design Methodology and Protection Strategy for ESD-CDM Robust Digital System Design in 90-nm and 130-nm Technologies. IEEE Transactions on Electron Devices, 2009, 56, 275-283.	3.0	9
211	ACCNTâ€"A Metallic-CNT-Tolerant Design Methodology for Carbon-Nanotube VLSI: Concepts and Experimental Demonstration. IEEE Transactions on Electron Devices, 2009, 56, 2969-2978.	3.0	36
212	Solution Assembly of Organized Carbon Nanotube Networks for Thin-Film Transistors. ACS Nano, 2009, 3, 4089-4097.	14.6	82
213	Digital VLSI logic technology using Carbon Nanotube FETs. , 2009, , .		39
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