Subhasish Mitra

List of Publications by Year
in descending order

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296	12,375	41344	46799
papers	citations	49 h-index	89 g-index

301	301	301	7326
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Carbon nanotube computer. Nature, 2013, 501, 526-530.	27.8	903
2	Three-dimensional integration of nanotechnologies for computing and data storage on a single chip. Nature, 2017, 547, 74-78.	27.8	577
3	Robust system design with built-in soft-error resilience. Computer, 2005, 38, 43-52.	1.1	450
4	Circuit Failure Prediction and Its Application to Transistor Aging. VLSI Test Symposium (VTS), Proceedings, IEEE, 2007, , .	1.0	375
5	The case for RAMClouds. Operating Systems Review (ACM), 2010, 43, 92-105.	1.9	344
6	Addressing failures in exascale computing. International Journal of High Performance Computing Applications, 2014, 28, 129-173.	3.7	265
7	ED/sup 4/I: error detection by diverse data and duplicated instructions. IEEE Transactions on Computers, 2002, 51, 180-199.	3.4	216
8	Which concurrent error detection scheme to choose ?. , 0, , .		197
9	X-Compact: An Efficient Response Compaction Technique. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2004, 23, 421-432.	2.7	192
10	Sequential Element Design With Built-In Soft Error Resilience. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2006, 14, 1368-1378.	3.1	177
11	Wafer-Scale Growth and Transfer of Aligned Single-Walled Carbon Nanotubes. IEEE Nanotechnology Magazine, 2009, 8, 498-504.	2.0	175
12	Quantitative evaluation of soft error injection techniques for robust system design. , 2013, , .		172
13	CMOS-Analogous Wafer-Scale Nanotube-on-Insulator Approach for Submicrometer Devices and Integrated Circuits Using Aligned Nanotubes. Nano Letters, 2009, 9, 189-197.	9.1	161
14	Energy-Efficient Abundant-Data Computing: The N3XT 1,000x. Computer, 2015, 48, 24-33.	1.1	156
15	Radiation-Induced Soft Error Rates of Advanced CMOS Bulk Devices. , 2006, , .		149
16	ERSA: Error Resilient System Architecture for probabilistic applications. , 2010, , .		145
17	Circuit-Level Performance Benchmarking and Scalability Analysis of Carbon Nanotube Transistor Circuits. IEEE Nanotechnology Magazine, 2009, 8, 37-45.	2.0	125
18	CASP. , 2008, , .		123

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19	Droplet impact dynamics on a spherical particle. Chemical Engineering Science, 2013, 100, 105-119.	3.8	122
20	The case for RAMCloud. Communications of the ACM, 2011, 54, 121-130.	4.5	119
21	Post-silicon validation opportunities, challenges and recent advances. , 2010, , .		116
22	Optimized Circuit Failure Prediction for Aging: Practicality and Promise. , 2008, , .		111
23	A review of the mechanisms and models of bubble-particle detachment in froth flotation. Separation and Purification Technology, 2016, 170, 155-172.	7.9	111
24	Monolithic 3D integration of logic and memory: Carbon nanotube FETs, resistive RAM, and silicon FETs. , 2014, , .		105
25	Carbon Nanotube Robust Digital VLSI. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 453-471.	2.7	104
26	Sensor-to-Digital Interface Built Entirely With Carbon Nanotube FETs. IEEE Journal of Solid-State Circuits, 2014, 49, 190-201.	5.4	101
27	Combinational Logic Soft Error Correction. , 2006, , .		97
28	Hyperdimensional computing with 3D VRRAM in-memory kernels: Device-architecture co-design for energy-efficient, error-resilient language recognition. , 2016, , .		95
29	Design Methods for Misaligned and Mispositioned Carbon-Nanotube Immune Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1725-1736.	2.7	93
30	Carbon Nanotube Transistor Circuits: Circuit-Level Performance Benchmarking and Design Options for Living with Imperfections. Digest of Technical Papers - IEEE International Solid-State Circuits Conference, 2007, , .	0.0	91
31	Reconfigurable architecture for autonomous self-repair. IEEE Design and Test of Computers, 2004, 21, 228-240.	1.0	90
32	Delay defect characteristics and testing strategies. IEEE Design and Test of Computers, 2003, 20, 8-16.	1.0	88
33	Understanding Energy Efficiency Benefits of Carbon Nanotube Field-Effect Transistors for Digital VLSI. IEEE Nanotechnology Magazine, 2018, 17, 1259-1269.	2.0	87
34	XPAND: an efficient test stimulus compression technique. IEEE Transactions on Computers, 2006, 55, 163-173.	3.4	85
35	Brain-inspired computing exploiting carbon nanotube FETs and resistive RAM: Hyperdimensional computing case study. , 2018, , .		84
36	Solution Assembly of Organized Carbon Nanotube Networks for Thin-Film Transistors. ACS Nano, 2009, 3, 4089-4097.	14.6	82

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37	VMR: VLSI-compatible metallic carbon nanotube removal for imperfection-immune cascaded multi-stage digital logic circuits using Carbon Nanotube FETs. , 2009, , .		82
38	Common-mode failures in redundant VLSI systems: a survey. IEEE Transactions on Reliability, 2000, 49, 285-295.	4.6	80
39	Self-Tuning for Maximized Lifetime Energy-Efficiency in the Presence of Circuit Aging. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 760-773.	2.7	79
40	TPAD: Hardware Trojan Prevention and Detection for Trusted Integrated Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 521-534.	2.7	79
41	ERSA: Error Resilient System Architecture for Probabilistic Applications. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 546-558.	2.7	77
42	IFRA. , 2008, , .		75
43	Threshold Voltage and Onâ€“Off Ratio Tuning for Multiple-Tube Carbon Nanotube FETs. IEEE Nanotechnology Magazine, 2009, 8, 4-9.	2.0	75
44	Post-Silicon Bug Localization in Processors Using Instruction Footprint Recording and Analysis (IFRA). IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 1545-1558.	2.7	75
45	A review of CFD modelling studies on the flotation process. Minerals Engineering, 2018, 127, 153-177.	4.3	73
46	The N3XT Approach to Energy-Efficient Abundant-Data Computing. Proceedings of the IEEE, 2019, 107, 19-48.	21.3	71
47	Carbon nanotube circuits in the presence of carbon nanotube density variations. , 2009, , .		70
48	Carbon Nanotube Circuit Integration up to Sub-20 nm Channel Lengths. ACS Nano, 2014, 8, 3434-3443.	14.6	70
49	Linear Increases in Carbon Nanotube Density Through Multiple Transfer Technique. Nano Letters, 2011, 11, 1881-1886.	9.1	69
50	Verification-Guided Soft Error Resilience. , 2007, , .		68
51	Overcoming Early-Life Failure and Aging for Robust Systems. IEEE Design and Test of Computers, 2009, 26, 28-39.	1.0	64
52	Activation of ganglion cells and axon bundles using epiretinal electrical stimulation. Journal of Neurophysiology, 2017, 118, 1457-1471.	1.8	64
53	Recent Advances and New Avenues in Hardware-Level Reliability Support. IEEE Micro, 2005, 25, 18-29.	1.8	62
54	Efficient FPGAs using nanoelectromechanical relays. , 2010, , .		62

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55	Hysteresis in Carbon Nanotube Transistors: Measurement and Analysis of Trap Density, Energy Level, and Spatial Distribution. ACS Nano, 2016, 10, 4599-4608.	14.6	62
56	On wetting characteristics of droplet on a spherical particle in film boiling regime. Chemical Engineering Science, 2016, 149, 181-203.	3.8	61
57	Resistive RAM-Centric Computing: Design and Modeling Methodology. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2263-2273.	5.4	61
58	Robust System Design to Overcome CMOS Reliability Challenges. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2011, 1, 30-41.	3.6	60
59	Nanoelectromechanical (NEM) relays integrated with CMOS SRAM for improved stability and low leakage. , 2009, , .		58
60	Packet-based input test data compression techniques. , 0, , .		56
61	A design diversity metric and analysis of redundant systems. IEEE Transactions on Computers, 2002, 51, 498-510.	3.4	56
62	Device study, chemical doping, and logic circuits based on transferred aligned single-walled carbon nanotubes. Applied Physics Letters, 2008, 93, .	3.3	54
63	Probabilistic Analysis and Design of Metallic-Carbon-Nanotube-Tolerant Digital Logic Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 1307-1320.	2.7	54
64	Testing for Transistor Aging. , 2009, , .		54
65	QED: Quick Error Detection tests for effective post-silicon validation. , 2010, , .		54
66	Scalable Carbon Nanotube Computational and Storage Circuits Immune to Metallic and Mispositioned Carbon Nanotubes. IEEE Nanotechnology Magazine, 2011, 10, 744-750.	2.0	54
67	Characterization and Implementation of Fault-Tolerant Vertical Links for 3-D Networks-on-Chip. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 124-134.	2.7	54
68	Built-In Soft Error Resilience for Robust System Design. , 2007, , .		53
69	New Logic Synthesis as Nanotechnology Enabler. Proceedings of the IEEE, 2015, 103, 2168-2195.	21.3	53
70	Dependable computing and online testing in adaptive and configurable systems. IEEE Design and Test of Computers, 2000, 17, 29-41.	1.0	52
71	Historical Perspective on Scan Compression. IEEE Design and Test of Computers, 2008, 25, 114-120.	1.0	51
72	VAST: Virtualization-Assisted Concurrent Autonomous Self-Test. , 2008, , .		50

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73	Wafer-Scale Fabrication and Characterization of Thin-Film Transistors with Polythiophene-Sorted Semiconducting Carbon Nanotube Networks. ACS Nano, 2012, 6, 451-458.	14.6	50
74	Hysteresis-Free Carbon Nanotube Field-Effect Transistors. ACS Nano, 2017, 11, 4785-4791.	14.6	50
75	Integration of nanoelectromechanical (NEM) relays with silicon CMOS with functional CMOS-NEM circuit. , 2011, , .		49
76	Hyperdimensional Computing Exploiting Carbon Nanotube FETs, Resistive RAM, and Their Monolithic 3D Integration. IEEE Journal of Solid-State Circuits, 2018, 53, 3183-3196.	5.4	49
77	Logic soft errors in sub-65nm technologies design and CAD challenges. , 2005, , .		48
78	Carbon nanotube correlation. , 2010, , .		48
79	Efficient seed utilization for reseeding based compression [logic testing]. , 0, , .		47
80	Test data compression. IEEE Design and Test of Computers, 2003, 20, 76-87.	1.0	46
81	Integrated wafer-scale growth and transfer of directional Carbon Nanotubes and misaligned-Carbon-Nanotube-immune logic structures. , 2008, , .		45
82	CLEAR. , 2016, , .		45
83	Resistive RAM Endurance: Array-Level Characterization and Correction Techniques Targeting Deep Learning Applications. IEEE Transactions on Electron Devices, 2019, 66, 1281-1288.	3.0	43
84	Resistive RAM With Multiple Bits Per Cell: Array-Level Demonstration of 3 Bits Per Cell. IEEE Transactions on Electron Devices, 2019, 66, 641-646.	3.0	43
85	Low-Temperature Side Contact to Carbon Nanotube Transistors: Resistance Distributions Down to 10 nm Contact Length. Nano Letters, 2019, 19, 1083-1089.	9.1	42
86	Characterization and Design of Logic Circuits in the Presence of Carbon Nanotube Density Variations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 1103-1113.	2.7	41
87	Collision behaviour of a smaller particle into a larger stationary droplet. Advanced Powder Technology, 2015, 26, 280-295.	4.1	41
88	Soft Error Resilient System Design through Error Correction. , 2006, , .		40
89	Interactions in droplet and particle system of near unity size ratio. Chemical Engineering Science, 2017, 170, 154-175.	3.8	40
90	Digital VLSI logic technology using Carbon Nanotube FETs. , 2009, , .		39

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91	Effective Post-Silicon Validation of System-on-Chips Using Quick Error Detection. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1573-1590.	2.7	38
92	The Trojan-proof chip. IEEE Spectrum, 2015, 52, 46-51.	0.7	38
93	High-performance carbon nanotube field-effect transistors. , 2014, , .		37
94	A design diversity metric and reliability analysis for redundant systems. , 0, , .		36
95	ACCNTâ€"A Metallic-CNT-Tolerant Design Methodology for Carbon-Nanotube VLSI: Concepts and Experimental Demonstration. IEEE Transactions on Electron Devices, 2009, 56, 2969-2978.	3.0	36
96	Circuit aging prediction for low-power operation. , 2009, , .		36
97	Rapid Co-Optimization of Processing and Circuit Design to Overcome Carbon Nanotube Variations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1082-1095.	2.7	36
98	Fault grading FPGA interconnect test configurations. , 0, , .		35
99	Logic soft errors a major barrier to robust platform design. , 0, , .		35
100	Gate-Oxide Early Life Failure Prediction. VLSI Test Symposium (VTS), Proceedings, IEEE, 2008, , .	1.0	35
101	High-Density Multiple Bits-per-Cell 1T4R RRAM Array with Gradual SET/RESET and its Effectiveness for Deep Learning. , 2019, , .		35
102	Test vector compression using EDA-ATE synergies. , 0, , .		34
103	The Search for Alternative Computational Paradigms. IEEE Design and Test of Computers, 2008, 25, 334-343.	1.0	34
104	Laterally Actuated Platinum-Coated Polysilicon NEM Relays. Journal of Microelectromechanical Systems, 2013, 22, 768-778.	2.5	34
105	X-Tolerant Test Response Compaction. IEEE Design and Test of Computers, 2005, 22, 566-574.	1.0	33
106	Automated design of misaligned-carbon-nanotube-immune circuits. Proceedings - Design Automation Conference, 2007, , .	0.0	33
107	Operating system scheduling for efficient online self-test in robust systems. , 2009, , .		32
108	Low-cost gate-oxide early-life failure detection in robust systems. , 2010, , .		32

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109	Combinational Logic Design Using Six-Terminal NEM Relays. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 653-666.	2.7	32
110	Monolithic 3D Integration: A Path from Concept to Reality. , 2015, , .		31
111	Application-independent testing of FPGA interconnects. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2005, 24, 1774-1783.	2.7	30
112	BLoG. , 2010, , .		30
113	Cooling three-dimensional integrated circuits using power delivery networks. , 2012, , .		28
114	Nano-Electro-Mechanical relays for FPGA routing: Experimental demonstration and a design technique. , 2012, , .		28
115	Evaporation of a droplet on a heated spherical particle. Chemical Engineering Journal, 2015, 278, 309-319.	12.7	28
116	CHIMERA: A 0.92 TOPS, 2.2 TOPS/W Edge AI Accelerator with 2 MByte On-Chip Foundry Resistive RAM for Efficient Training and Inference. , 2021, , .		28
117	XMAX: X-tolerant architecture for MAXimal test compression. , 0, , .		27
118	Efficient metallic carbon nanotube removal readily scalable to wafer-level VLSI CNFET circuits. , 2010, , .		27
119	Overcoming carbon nanotube variations through co-optimized technology and circuit design. , 2011, , .		27
120	Concurrent autonomous self-test for uncore components in system-on-chips. , 2010, , .		25
121	Efficient metallic carbon nanotube removal for highly-scaled technologies. , 2015, , .		25
122	A Density Metric for Semiconductor Technology [Point of View]. Proceedings of the IEEE, 2020, 108, 478-482.	21.3	25
123	Cross-layer resilience challenges: Metrics and optimization. , 2010, , .		24
124	Quick detection of difficult bugs for effective post-silicon validation. , 2012, , .		24
125	Comparison of specific energy dissipation rate calculation methodologies utilising 2D PIV velocity measurement. Chemical Engineering Science, 2015, 137, 752-767.	3.8	24
126	Optimization of Electrical Stimulation for a High-Fidelity Artificial Retina. , 2019, , .		24

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127	Monolithic 3-D Integration. IEEE Micro, 2019, 39, 16-27.	1.8	24
128	RADAR: A Fast and Energy-Efficient Programming Technique for Multiple Bits-Per-Cell RRAM Arrays. IEEE Transactions on Electron Devices, 2021, 68, 4397-4403.	3.0	24
129	ACCNT: A Metallic-CNT-Tolerant Design Methodology for Carbon Nanotube VLSI: Analyses and Design Guidelines. IEEE Transactions on Electron Devices, 2010, 57, 2284-2295.	3.0	22
130	Carbon nanotube electronics - Materials, devices, circuits, design, modeling, and performance projection. , 2011, , .		22
131	Segregation and dispersion studies in binary solid-liquid fluidised beds: A theoretical and computational study. Powder Technology, 2017, 314, 400-411.	4.2	22
132	Dynamic Surface Wetting and Heat Transfer in a Droplet-Particle System of Less Than Unity Size Ratio. Frontiers in Chemistry, 2018, 6, 259.	3.6	22
133	Processor Hardware Security Vulnerabilities and their Detection by Unique Program Execution Checking. , 2019, , .		22
134	Monolithic three-dimensional integration of carbon nanotube FETs with silicon CMOS. , 2014, , .		21
135	Expansion behaviour of a binary solid-liquid fluidised bed with different solid mass ratio. Advanced Powder Technology, 2017, 28, 3111-3129.	4.1	21
136	Four-Bits-Per-Memory One-Transistor-and-Eight-Resistive-Random-Access-Memory (1T8R) Array. IEEE Electron Device Letters, 2021, 42, 335-338.	3.9	21
137	Time-Based Sensor Interface Circuits in CMOS and Carbon Nanotube Technologies. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 577-586.	5.4	20
138	Experimental study of gate oxide early-life failures. Reliability Physics Symposium, 2009 IEEE International, 2009, , .	0.0	19
139	Optimized self-tuning for circuit aging. , 2010, , .		19
140	Monolithic three-dimensional integration of carbon nanotube FET complementary logic circuits. , 2013, , .		19
141	Techniques and Algorithms for Fault Grading of FPGA Interconnect Test Configurations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2004, 23, 261-272.	2.7	18
142	Application-Dependent Delay Testing of FPGAs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 553-563.	2.7	18
143	Experimental demonstration of a fully digital capacitive sensor interface built entirely using carbon-nanotube FETs. , 2013, , .		18
144	Direct visualisation of bubble-particle interactions in presence of cavitation bubbles in an ultrasonic flotation cell. Minerals Engineering, 2021, 174, 107258.	4.3	18

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145	Optimized reseeding by seed ordering and encoding. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2005, 24, 264-270.	2.7	17
146	CASP: Concurrent Autonomous Chip Self-Test Using Stored Test Patterns. , 2008, , .		17
147	Self-repair of uncore components in robust system-on-chips: An OpenSPARC T2 case study. , 2013, , .		17
148	Monolithic 3D integration advances and challenges: From technology to system levels. , 2014, , .		17
149	Understanding soft errors in uncore components. , 2015, , .		17
150	Experimental investigation on modulation of homogeneous and isotropic turbulence in the presence of single particle using time-resolved PIV. Chemical Engineering Science, 2016, 153, 308-329.	3.8	17
151	Evaporation of a suspended binary mixture droplet in a heated flowing gas stream. Experimental Thermal and Fluid Science, 2018, 91, 329-344.	2.7	17
152	A Data-Compressive Wired-OR Readout for Massively Parallel Neural Recording. IEEE Transactions on Biomedical Circuits and Systems, 2019, 13, 1128-1140.	4.0	17
153	Memory Sizing of a Scalable SRAM In-Memory Computing Tile Based Architecture. , 2019, , .		17
154	DECOY: DEflection-Driven HLS-Based Computation Partitioning for Obfuscating Intellectual PropertY. , 2020, , .		17
155	Early-life-failure detection using SAT-based ATPG. , 2013, , .		16
156	Comparison of vaporization models for feed droplet in fluid catalytic cracking risers. Chemical Engineering Research and Design, 2015, 101, 82-97.	5.6	16
157	Combinational logic synthesis for diversity in duplex systems. , 0, , .		15
158	Cross-layer error resilience for robust systems. , 2010, , .		15
159	Interaction dynamics of a spherical particle with a suspended liquid film. AICHE Journal, 2016, 62, 295-314.	3.6	15
160	Development of a flotation recovery model with CFD predicted collision efficiency. Minerals Engineering, 2020, 159, 106615.	4.3	15
161	Illusion of large on-chip memory by networked computing chips for neural network inference. Nature Electronics, 2021, 4, 71-80.	26.0	15
162	CHIMERA: A 0.92-TOPS, 2.2-TOPS/W Edge AI Accelerator With 2-MByte On-Chip Foundry Resistive RAM for Efficient Training and Inference. IEEE Journal of Solid-State Circuits, 2022, 57, 1013-1026.	5.4	15

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163	Efficient multiplexer synthesis techniques. IEEE Design and Test of Computers, 2000, 17, 90-97.	1.0	14
164	Rapid exploration of processing and design guidelines to overcome carbon nanotube variations. , 2013, , .		14
165	Efficient Soft Error Vulnerability Estimation of Complex Designs. , 2015, , .		14
166	Tolerating Soft Errors in Processor Cores Using CLEAR (Cross-Layer Exploration for Architecting) Tj ETQq0 0 0 rgBT /Overlock 10 Tf 50 62 1839-1852.	2.7	14
167	Evaporation of a sessile binary droplet on a heated spherical particle. Experimental Thermal and Fluid Science, 2018, 99, 558-571.	2.7	14
168	A Formal Approach for Detecting Vulnerabilities to Transient Execution Attacks in Out-of-Order Processors. , 2020, , .		14
169	Sub-0.5 nm Interfacial Dielectric Enables Superior Electrostatics: 65 mV/dec Top-Gated Carbon Nanotube FETs at 15 nm Gate Length. , 2020, , .		14
170	Circuit failure prediction for robust system design in scaled CMOS. , 2008, , .		13
171	A structured approach to post-silicon validation and debug using symbolic quick error detection. , 2015, , .		13
172	Hybrid quick error detection (H-QED). , 2015, , .		13
173	System-Level Effects of Soft Errors in Uncore Components. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1497-1510.	2.7	13
174	Modulation of turbulent flow field in an oscillating grid system owing to single bubble rise. Chemical Engineering Science, 2018, 185, 26-49.	3.8	13
175	14.3 A 43pJ/Cycle Non-Volatile Microcontroller with 4.7Î¼s Shutdown/Wake-up Integrating 2.3-bit/Cell Resistive RAM and Resilience Techniques. , 2019, , .		13
176	Efficient design diversity estimation for combinational circuits. IEEE Transactions on Computers, 2004, 53, 1483-1492.	3.4	12
177	The resilience wall: Cross-layer solution strategies. , 2014, , .		12
178	Settling/rising of a foreign particle in solid-liquid fluidized beds: Application of dynamic mesh technique. Chemical Engineering Science, 2017, 170, 139-153.	3.8	12
179	Logic Bug Detection and Localization Using Symbolic Quick Error Detection. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2024, , 1-1.	2.7	12
180	Carbon nanotube circuits: Living with imperfections and variations. , 2010, , .		11

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181	Carbon nanotubes for high-performance logic. MRS Bulletin, 2014, 39, 719-726.	3.5	11
182	Quick Error Detection Tests with Fast Runtimes for Effective Post-Silicon Validation and Debug. , 2015, , .		11
183	Bandgap Extraction at 10 K to Enable Leakage Control in Carbon Nanotube MOSFETs. IEEE Electron Device Letters, 2022, 43, 490-493.	3.9	11
184	Fault escapes in duplex systems. , 0, , .		10
185	Architecture and performance evaluation of 3D CMOS-NEM FPGA. , 2011, , .		10
186	Air-stable technique for fabricating n-type carbon nanotube FETs. , 2011, , .		10
187	Rethinking error injection for effective resilience. , 2014, , .		10
188	NSF expedition on variability-aware software: Recent results and contributions. IT - Information Technology, 2015, 57, 181-198.	0.9	10
189	Interaction of a spherical particle with a neutrally buoyant immiscible droplet in salt solution. Chemical Engineering Science, 2017, 172, 182-198.	3.8	10
190	A 35.6 TOPS/W/mmÂ² 3-Stage Pipelined Computational SRAM With Adjustable Form Factor for Highly Data-Centric Applications. IEEE Solid-State Circuits Letters, 2020, 3, 286-289.	2.0	10
191	Design Guidelines for Metallic-Carbon-Nanotube-Tolerant Digital Logic Circuits. , 2008, , .		9
192	Design Methodology and Protection Strategy for ESD-CDM Robust Digital System Design in 90-nm and 130-nm Technologies. IEEE Transactions on Electron Devices, 2009, 56, 275-283.	3.0	9
193	Monolithic three-dimensional integrated circuits using carbon nanotube FETs and interconnects. , 2009, , .		9
194	The effect of amine protonation on the electrical properties of spin-assembled single-walled carbon nanotube networks. Nanotechnology, 2011, 22, 125201.	2.6	9
195	Dual sidewall lateral nanoelectromechanical relays with beam isolation. , 2011, , .		9
196	Detachment of a bubble anchored to a vertical cylindrical surface in quiescent liquid and grid generated turbulence. Canadian Journal of Chemical Engineering, 2014, 92, 2067-2077.	1.7	9
197	High performance, integrated 1T1R oxide-based oscillator: Stack engineering for low-power operation in neural network applications. , 2015, , .		9
198	Symbolic quick error detection using symbolic initial state for pre-silicon verification. , 2018, , .		9

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199	Analysis of particle dispersion coefficient in solid-liquid fluidised beds. Powder Technology, 2020, 365, 60-73.	4.2	9
200	Spatially patterned bi-electrode epiretinal stimulation for axon avoidance at cellular resolution. Journal of Neural Engineering, 2021, 18, 066007.	3.5	9
201	Automatic Identification of Axon Bundle Activation for Epiretinal Prosthesis. IEEE Transactions on Neural Systems and Rehabilitation Engineering, 2021, 29, 2496-2502.	4.9	9
202	Effect of turbulence dispersion on bubble-particle collision efficiency. Minerals Engineering, 2022, 177, 107374.	4.3	9
203	Scan synthesis for one-hot signals. , 0, , .		8
204	Diversity techniques for concurrent error detection. , 0, , .		8
205	Gate-oxide early-life failure identification using delay shifts. , 2010, , .		8
206	Robust System Design. , 2010, , .		8
207	Titanium nitride sidewall stringer process for lateral nanoelectromechanical relays. , 2010, , .		8
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209	System Level Benchmarking with Yield-Enhanced Standard Cell Library for Carbon Nanotube VLSI Circuits. ACM Journal on Emerging Technologies in Computing Systems, 2014, 10, 1-19.	2.3	8
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213	Low-power, high-performance S-NDR oscillators for stereo (3D) vision using directly-coupled oscillator networks. , 2016, , .		8
214	Review of Methodologies for Pre- and Post-Silicon Analog Verification in Mixed-Signal SOCs. , 2019, , .		8
215	An Exhaustive Approach to Detecting Transient Execution Side Channels in RTL Designs of Processors. IEEE Transactions on Computers, 2023, 72, 222-235.	3.4	8
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