Eby G Friedman

List of Publications by Year
in descending order

180 papers	5,820 citations	236925 25 h-index	95266 68 g-index
183 all docs	183 docs citations	183 times ranked	2974 citing authors

#	Article	IF	Citations
1	SPROUTâ€"Smart Power Routing Tool for Board-Level Exploration and Prototyping. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2263-2275.	2.7	9
2	Superconductive IC Manufacturing. , 2022, , 85-93.		0
3	Rapid Single Flux Quantum (RSFQ) Circuits. , 2022, , 55-73.		0
4	Inductive Coupling Noise in Multilayer Superconductive ICs. , 2022, , 123-132.		0
5	Partitioning RSFQ Circuits for Current Recycling. , 2022, , 185-195.		2
6	Compact Model of Superconductor-Ferromagnetic Transistor. , 2022, , 115-121.		0
7	Wave Pipelining in DSFQ Circuits. , 2022, , 155-168.		0
8	Design for Testability of SFQ Circuits. , 2022, , 209-221.		0
9	Superconductive Circuits. , 2022, , 39-53.		0
10	Synchronization. , 2022, , 75-83.		0
11	EDA for Superconductive Electronics. , 2022, , 95-114.		0
12	Physics and Devices of Superconductive Electronics. , 2022, , 15-38.		0
13	Dynamic Single Flux Quantum Majority Gates. , 2022, , 141-154.		0
14	GALS Clocking and Shared Interconnect for Large Scale SFQ Systems. , 2022, , 197-207.		0
15	Design Guidelines for ERSFQ Bias Networks. , 2022, , 169-184.		0
16	QuCTSâ€"Single-Flux Quantum Clock Tree Synthesis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 3346-3358.	2.7	13
17	Single Flux Quantum Integrated Circuit Design. , 2022, , .		26
18	Wave Pipelining in DSFQ Circuits. IEEE Transactions on Applied Superconductivity, 2022, 32, 1-6.	1.7	0

#	Article	IF	Citations
19	Flux Mitigation in Wide Superconductive Striplines. IEEE Transactions on Applied Superconductivity, 2022, 32, 1-6.	1.7	7
20	Surface Inductance of Superconductive Striplines. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2952-2956.	3.0	6
21	Superconductive Logic Using 2ï•â€"Josephson Junctions With Half Flux Quantum Pulses. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2533-2537.	3.0	2
22	Thermal Modeling of Rapid Single Flux Quantum Circuit Structures. IEEE Transactions on Electron Devices, 2022, 69, 2718-2724.	3.0	2
23	Inductive noise coupling in multilayer superconductive ICs. Microelectronics Journal, 2022, 126, 105336.	2.0	2
24	MTJ-Based Dithering for Stochastic Analog-to-Digital Conversion. , 2021, , .		0
25	Tile-Based Power Delivery Networks for High Current, Voltage Stacked Systems. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2021, 11, 1097-1105.	2.5	0
26	Inductive Noise Coupling in Superconductive Passive Transmission Lines. , 2021, , .		7
27	Partitioning RSFQ Circuits for Current Recycling. IEEE Transactions on Applied Superconductivity, 2021, 31, 1-6.	1.7	18
28	Logic Locking in Single Flux Quantum Circuits. IEEE Transactions on Applied Superconductivity, 2021, 31, 1-5.	1.7	13
29	Splitter Trees in Single Flux Quantum Circuits. IEEE Transactions on Applied Superconductivity, 2021, 31, 1-6.	1.7	22
30	Design Automation of Superconductive Digital Circuits: A review. IEEE Nanotechnology Magazine, 2021, 15, 54-67.	1.3	8
31	SPROUT - Smart Power ROUting Tool for Board-Level Exploration and Prototyping. , 2021, , .		11
32	Toward Increasing the Difficulty of Reverse Engineering of RSFQ Circuits. IEEE Transactions on Applied Superconductivity, 2020, 30, 1-13.	1.7	14
33	Assembly Process and Electrical Properties of Top-Transferred Graphene on Carbon Nanotubes for Carbon-Based 3-D Interconnects. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2020, 10, 516-524.	2.5	8
34	Power Delivery Exploration Methodology Based on Constrained Optimization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 1916-1924.	2.7	11
35	Distributed Pass Gates in Power Delivery Systems With Digital Low-Dropout Regulators. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 414-420.	3.1	1
36	EMI Suppression With Distributed LLC Resonant Converter for High-Voltage VR-on-Package. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2020, 10, 263-271.	2.5	3

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37	Bias Distribution in ERSFQ VLSI Circuits. , 2020, , .		17
38	Challenges in High Current On-Chip Voltage Stacked Systems. , 2020, , .		2
39	Distributed Port Assignment for Extraction of Power Delivery Networks. , 2020, , .		1
40	Design Methodology for Distributed Large-Scale ERSFQ Bias Networks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2438-2447.	3.1	34
41	Effective Resistance of Finite Two-Dimensional Grids Based on Infinity Mirror Technique. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3224-3233.	5.4	10
42	Repeater Insertion in SFQ Interconnect. IEEE Transactions on Applied Superconductivity, 2020, 30, 1-8.	1.7	31
43	Asynchronous Dynamic Single-Flux Quantum Majority Gates. IEEE Transactions on Applied Superconductivity, 2020, 30, 1-7.	1.7	25
44	Distributed Spintronic/CMOS Sensor Network for Thermal-Aware Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1505-1512.	3.1	2
45	Global interconnects in VLSI complexity single flux quantum systems. , 2020, , .		13
46	Sense Amplifier for Spin-Based Cryogenic Memory Cells. IEEE Transactions on Applied Superconductivity, 2019, 29, 1-4.	1.7	11
47	Globally Asynchronous, Locally Synchronous Clocking and Shared Interconnect for Large-Scale SFQ Systems. IEEE Transactions on Applied Superconductivity, 2019, 29, 1-5.	1.7	20
48	Effective Resistance of Two-Dimensional Truncated Infinite Mesh Structures. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 4368-4376.	5.4	8
49	Stability of On-Chip Power Delivery Systems With Multiple Low-Dropout Regulators. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1779-1789.	3.1	7
50	PMTJ Temperature Sensor Utilizing VCMA. , 2019, , .		2
51	Interconnect Routing for Large-Scale RSFQ Circuits. IEEE Transactions on Applied Superconductivity, 2019, 29, 1-5.	1.7	47
52	Power Noise and Near-Field EMI of High-Current System-in-Package With VR Top and Bottom Placements. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2019, 9, 712-718.	2.5	10
53	Electrical and Thermal Models of CNT TSV and Graphite Interface. IEEE Transactions on Electron Devices, 2018, 65, 1880-1886.	3.0	5
54	Energy-Efficient Write Scheme for Nonvolatile Resistive Crossbar Arrays With Selectors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 711-719.	3.1	12

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55	Exploratory design of on-chip power delivery for 14, 10, and 7 nm and beyond FinFET ICs. The Integration VLSI Journal, 2018, 61, 11-19.	2.1	7
56	Memristor-Based Circuit Design for Multilayer Neural Networks. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 677-686.	5.4	158
57	Versatile Framework for Power Delivery Exploration. , 2018, , .		4
58	Hybrid Write Bias Scheme for Non-Volatile Resistive Crossbar Arrays. , 2018, , .		5
59	Behavioral Verilog-A Model of Superconductor-Ferromagnetic Transistor. , 2018, , .		8
60	Modeling Size Limitations of Resistive Crossbar Array With Cell Selectors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 286-293.	3.1	11
61	Hexagonal TSV Bundle Topology for 3-D ICs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 11-15.	3.0	16
62	Synaptic Characteristics of Ag/AgInSbTe/Ta-Based Memristor for Pattern Recognition Applications. IEEE Transactions on Electron Devices, 2017, 64, 1806-1811.	3.0	87
63	Memristive Model for Synaptic Circuits. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 767-771.	3.0	103
64	Design for Testability of SFQ Circuits. IEEE Transactions on Applied Superconductivity, 2017, 27, 1-7.	1.7	25
65	On the stability of distributed on-chip low dropout regulators. , 2017, , .		1
66	Test point insertion for RSFQ circuits. , 2017, , .		8
67	Distributed sinusoidal resonant converter with high step-down ratio. , 2017, , .		3
68	Layer ordering to minimize TSVs in heterogeneous 3-D ICs. , 2016, , .		2
69	On-Chip Power Delivery and Management. , 2016, , .		70
70	All-Spin-Orbit Switching of Perpendicular Magnetization. IEEE Transactions on Electron Devices, 2016, 63, 4499-4505.	3.0	15
71	Power noise in 14, 10, and 7 nm FinFET CMOS technologies. , 2016, , .		1
72	Design models of resistive crossbar arrays with selector devices. , 2016, , .		1

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73	Reducing Switching Latency and Energy in STT-MRAM Caches With Field-Assisted Writing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 129-138.	3.1	23
74	Noise Coupling Models in Heterogeneous 3-D ICs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2778-2786.	3.1	7
75	Stability of Distributed Power Delivery Systems With Multiple Parallel On-Chip LDO Regulators. IEEE Transactions on Power Electronics, 2016, 31, 5625-5634.	7.9	23
76	Back to the Future: Current-Mode Processor in the Era of Deeply Scaled CMOS. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1266-1279.	3.1	16
77	Power Efficient Level Shifter for 16 nm FinFET Near Threshold Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 774-778.	3.1	19
78	PNS-FCR: Flexible Charge Recycling Dynamic Circuit Technique for Low-Power Microprocessors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 613-624.	3.1	3
79	Inductive coupling effects in large TSV arrays. , 2015, , .		0
80	Distributed LDO regulators in a 28 nm power delivery system. Analog Integrated Circuits and Signal Processing, 2015, 83, 295-309.	1.4	19
81	VTEAM: A General Model for Voltage-Controlled Memristors. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 786-790.	3.0	525
82	Multistate Register Based on Resistive RAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1750-1759.	3.1	9
83	Experimental Analysis of Thermal Coupling in 3-D Integrated Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2077-2089.	3.1	9
84	3-D floorplanning algorithm to minimize thermal interactions. , 2015, , .		3
85	Energy-Efficient Nonvolatile Flip-Flop With Subnanosecond Data Backup Time for Fine-Grain Power Gating. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 1154-1158.	3.0	23
86	MOS Current Mode Logic Near Threshold Circuits. Journal of Low Power Electronics and Applications, 2014, 4, 138-152.	2.0	9
87	Thermal conduction path analysis in 3-D ICs. , 2014, , .		9
88	Computationally efficient clustering of power supplies in heterogeneous real time systems. , 2014, , .		1
89	Field driven STT-MRAM cell for reduced switching latency and energy. , 2014, , .		3
90	Dynamic power management with power network-on-chip. , 2014, , .		7

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91	Memristor-Based Multithreading. IEEE Computer Architecture Letters, 2014, 13, 41-44.	1.5	18
92	Digitally Controlled Pulse Width Modulator for On-Chip Power Management. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 2527-2534.	3.1	16
93	Memristive multistate pipeline register. , 2014, , .		1
94	MAGICâ€"Memristor-Aided Logic. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 895-899.	3.0	542
95	Sub-crosspoint RRAM decoding for improved area efficiency. , 2014, , .		1
96	Memristor-Based Material Implication (IMPLY) Logic: Design Principles and Methodologies. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 2054-2066.	3.1	453
97	Power Network Optimization Based on Link Breaking Methodology. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 983-987.	3.1	11
98	Performance characteristics of 14 nm near threshold MCML circuits. , 2013, , .		1
99	Active Filter-Based Hybrid On-Chip DCâ€"DC Converter for Point-of-Load Voltage Regulation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 680-691.	3.1	38
100	TEAM: ThrEshold Adaptive Memristor Model. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 211-221.	5.4	601
101	Power Noise in TSV-Based 3-D Integrated Circuits. IEEE Journal of Solid-State Circuits, 2013, 48, 587-597.	5.4	18
102	Digitally controlled wide range pulse width modulator for on-chip power supplies. , 2013, , .		6
103	Heterogeneous Methodology for Energy Efficient Distribution of On-Chip Power Supplies. IEEE Transactions on Power Electronics, 2013, 28, 4267-4280.	7.9	49
104	Current profile of a microcontroller to determine electromagnetic emissions. , 2013, , .		3
105	Energy metrics for power efficient crosslink and mesh topologies. , 2012, , .		0
106	Arithmetic encoding for memristive multi-bit storage. , 2012, , .		4
107	An area efficient on-chip hybrid voltage regulator. , 2012, , .		13
108	STT-MRAM memory cells with enhanced on/off ratio. , 2012, , .		3

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109	Distributed power delivery for energy efficient and low power systems. , 2012, , .		0
110	Recent progress on 3-D integrated intra-chip free-space optical interconnect. , 2012, , .		6
111	Distributed On-Chip Power Delivery. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2012, 2, 704-713.	3.6	52
112	Design methodology to distribute on-chip power in next generation integrated circuits. , 2012, , .		2
113	Models of memristors for SPICE simulations. , 2012, , .		48
114	MRL &#x2014; Memristor Ratioed Logic. , 2012, , .		111
115	Efficient algorithms for fast IR drop analysis exploiting locality. The Integration VLSI Journal, 2012, 45, 149-161.	2.1	25
116	A Distributed Filter Within a Switching Converter for Application to 3-D Integrated Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1075-1085.	3.1	6
117	Distributed power network co-design with on-chip power supplies and decoupling capacitors. , 2011, , .		18
118	Clock Distribution Networks in 3-D Integrated Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 2256-2266.	3.1	38
119	Clock distribution models of 3-D integrated systems. , 2011, , .		1
120	Memristor-based IMPLY logic design procedure. , 2011, , .		91
121	A 3-D Integrated Intrachip Free-Space Optical Interconnect for Many-Core Chips. IEEE Photonics Technology Letters, 2011, 23, 164-166.	2.5	22
122	Linear and Switch-Mode Conversion in 3-D Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 2095-2108.	3.1	3
123	Low Power Clock Network Design. Journal of Low Power Electronics and Applications, 2011, 1, 219-246.	2.0	8
124	Effective Resistance of a Two Layer Mesh. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 739-743.	3.0	21
125	Methodology for multi-layer interdigitated power and ground network design. , 2010, , .		4
126	Fast algorithms for power grid analysis based on effective resistance. , 2010, , .		10

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127	Power grid analysis based on a macro circuit model. , 2010, , .		3
128	Globally integrated power and clock distribution network. , 2010, , .		2
129	Compact substrate models for efficient noise coupling and signal isolation analysis. , 2010, , .		7
130	Corrections to "Unified Logical Effort—A Method for Delay Evaluation and Minimization in Logic Paths With RC Interconnect"[May 10 689-696]. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1262-1262.	3.1	0
131	Unified Logical Effort—A Method for Delay Evaluation and Minimization in Logic Paths With RC Interconnect. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 689-696.	3.1	24
132	An area efficient fully monolithic hybrid voltage regulator. , 2010, , .		14
133	Simultaneous co-design of distributed on-chip power supplies and decoupling capacitors. , 2010, , .		6
134	On-chip DC-DC converters for three-dimensional ICs. , 2009, , .		7
135	Minimizing noise via shield and repeater insertion. , 2009, , .		1
136	Shielding methodologies in the presence of power/ground noise. , 2009, , .		2
137	Closed-Form Expressions of 3-D Via Resistance, Inductance, and Capacitance. IEEE Transactions on Electron Devices, 2009, 56, 1873-1881.	3.0	179
138	Interconnect-Based Design Methodologies for Three-Dimensional Integrated Circuits. Proceedings of the IEEE, 2009, 97, 123-140.	21.3	107
139	Inductance Model of Interdigitated Power and Ground Distribution Networks. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 585-589.	3.0	5
140	Worst Case Power/Ground Noise Estimation Using an Equivalent Transition Time for Resonance. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 997-1004.	5.4	30
141	Identification of Dominant Noise Source and Parameter Sensitivity for Substrate Coupling. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 1559-1564.	3.1	5
142	Methodology for Efficient Substrate Noise Analysis in Large-Scale Mixed-Signal Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 1405-1418.	3.1	17
143	Effective Capacitance of Inductive Interconnects for Short-Circuit Power Analysis. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 26-30.	3.0	7
144	Nanoscale on-chip decoupling capacitors. , 2008, , .		0

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145	Effective Radii of On-Chip Decoupling Capacitors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 894-907.	3.1	77
146	Dominant Substrate Noise Coupling Mechanism for Multiple Switching Gates. , 2008, , .		1
147	Efficient Distributed On-Chip Decoupling Capacitors for Nanoscale ICs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 1717-1721.	3.1	5
148	Methodology for placing localized guard rings to reduce substrate noise in mixed-signal circuits. , 2008, , .		0
149	On-Chip Power Distribution Grids With Multiple Supply Voltages for High-Performance Integrated Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 908-921.	3.1	16
150	Equivalent rise time for resonance in power/ground noise estimation. , 2008, , .		3
151	Transient simulation of on-chip transmission lines via exact pole extraction. , 2008, , .		1
152	Electrical modeling and characterization of 3-D vias. , 2008, , .		50
153	Clock distribution networks for 3-D ictegrated Circuits. , 2008, , .		36
154	Pseudo-random clocking to enhance signal integrity. , 2008, , .		3
155	Clock distribution architectures for 3-D SOI integrated circuits. , 2008, , .		4
156	Input port reduction for efficient substrate extraction in large scale ICâ€™s. , 2008, , .		2
157	Substrate Noise Reduction Based On Noise Aware Cell Design. , 2007, , .		1
158	Exploiting Setupâ€"Hold-Time Interdependence in Static Timing Analysis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1114-1125.	2.7	52
159	Quasi-Resonant Interconnects: A Low Power Design Methodology. , 2007, , .		2
160	Efficient placement of distributed on-chip decoupling capacitors in nanoscale ICs. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	11
161	Design Methodology for Global Resonant ${m H}$-Tree Clock Distribution Networks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 135-148.	3.1	53
162	3-D Topologies for Networks-on-Chip. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 1081-1090.	3.1	323

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163	3-D Topologies for Networks-on-Chip. , 2006, , .		37
164	On-Chip Optical Interconnect Roadmap: Challenges and Critical Directions. IEEE Journal of Selected Topics in Quantum Electronics, 2006, 12, 1699-1705.	2.9	327
165	Clock Feedthrough in CMOS Analog Transmission Gate Switches. Analog Integrated Circuits and Signal Processing, 2005, 44, 271-281.	1.4	17
166	Cascode Monolithic DC-DC Converter for Reliable Operation at High Input Voltages. Analog Integrated Circuits and Signal Processing, 2005, 42, 231-238.	1.4	14
167	Resistive Power in CMOS Circuits. Analog Integrated Circuits and Signal Processing, 2004, 41, 5-11.	1.4	1
168	Complex Â±1 Multiplier Based on Signed-Binary Transformations. Journal of Signal Processing Systems, 2004, 38, 13-24.	1.0	1
169	Optimum wire sizing of RLC interconnect with repeaters. The Integration VLSI Journal, 2004, 38, 205-225.	2.1	46
170	Frequency Characteristics of High Speed Power Distribution Grids. Analog Integrated Circuits and Signal Processing, 2003, 35, 207-214.	1.4	5
171	Title is missing!. Analog Integrated Circuits and Signal Processing, 2002, 31, 209-224.	1.4	1
172	Title is missing!. Analog Integrated Circuits and Signal Processing, 2002, 31, 249-259.	1.4	11
173	Placement of Substrate Contacts to Minimize Substrate Noise in Mixed-Signal Integrated Circuits. Analog Integrated Circuits and Signal Processing, 2001, 28, 253-264.	1.4	10
174	Applying Analog Techniques in Digital CMOS Buffers to Improve Speed and Noise Immunity. Analog Integrated Circuits and Signal Processing, 2001, 27, 273-277.	1.4	2
175	Automated Synthesis of Skew-Based Clock Distribution Networks. VLSI Design, 1998, 7, 31-57.	0.5	5
176	Timing of Multi-Gigahertz Rapid Single Flux Quantum Digital Circuits. Journal of Signal Processing Systems, 1997, 16, 247-276.	1.0	69
177	Title is missing!. Journal of Signal Processing Systems, 1997, 16, 149-161.	1.0	10
178	Ramp Input Response of RC Tree Networks. Analog Integrated Circuits and Signal Processing, 1997, 14, 53-58.	1.4	26
179	Delay and Power Expressions for a CMOS Inverter Driving a Resistive-Capacitive Load. Analog Integrated Circuits and Signal Processing, 1997, 14, 29-39.	1.4	64
180	The limiting performance of a CMOS bistable register based on waveform considerations. International Journal of Electronics, 1992, 73, 371-384.	1.4	1