Woo Young Choi

List of Publications by Year
in descending order

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157 papers	3,891 citations	331670 21 h-index	133252 59 g-index
159 all docs	159 docs citations	159 times ranked	1798 citing authors

#	Article	IF	Citations
1	Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec. IEEE Electron Device Letters, 2007, 28, 743-745.	3.9	1,537
2	Hetero-Gate-Dielectric Tunneling Field-Effect Transistors. IEEE Transactions on Electron Devices, 2010, 57, 2317-2319.	3.0	394
3	Demonstration of L-Shaped Tunnel Field-Effect Transistors. IEEE Transactions on Electron Devices, 2016, 63, 1774-1778.	3.0	250
4	Negative Capacitance in Organic/Ferroelectric Capacitor to Implement Steep Switching MOS Devices. Nano Letters, 2015, 15, 4553-4556.	9.1	162
5	Design optimization of gate-all-around (GAA) MOSFETs. IEEE Nanotechnology Magazine, 2006, 5, 186-191.	2.0	98
6	Analytical model of single-gate silicon-on-insulator (SOI) tunneling field-effect transistors (TFETs). Solid-State Electronics, 2011, 63, 110-114.	1.4	87
7	100-nm n-/p-channel I-MOS using a novel self-aligned structure. IEEE Electron Device Letters, 2005, 26, 261-263.	3.9	71
8	Effects of Device Geometry on Hetero-Gate-Dielectric Tunneling Field-Effect Transistors. IEEE Electron Device Letters, 2012, 33, 1459-1461.	3.9	71
9	Influence of Inversion Layer on Tunneling Field-Effect Transistors. IEEE Electron Device Letters, 2011, 32, 1191-1193.	3.9	57
10	Design Guideline of Si-Based L-Shaped Tunneling Field-Effect Transistors. Japanese Journal of Applied Physics, 2012, 51, 06FE09.	1.5	54
11	Design Guideline of Si-Based L-Shaped Tunneling Field-Effect Transistors. Japanese Journal of Applied Physics, 2012, 51, 06FE09.	1.5	54
12	Work-Function Variation Effects of Tunneling Field-Effect Transistors (TFETs). IEEE Electron Device Letters, 2013, 34, 942-944.	3.9	51
13	Nano-Electro-Mechanical Nonvolatile Memory (NEMory) Cell Design and Scaling. IEEE Transactions on Electron Devices, 2008, 55, 3482-3488.	3.0	46
14	70-nm impact-ionization metal-oxide-semiconductor (I-MOS) devices integrated with tunneling field-effect transistors (TFETs). , 0, , .		43
15	A Novel Biasing Scheme for I-MOS (Impact-Ionization MOS) Devices. IEEE Nanotechnology Magazine, 2005, 4, 322-325.	2.0	42
16	Compact Nano-Electro-Mechanical Non-Volatile Memory (NEMory) for 3D Integration. , 2007, , .		39
17	Demonstration of hetero-gate-dielectric tunneling field-effect transistors (HG TFETs). Nano Convergence, 2016, 3, 13.	12.1	39
18	Dual-dielectric-constant spacer hetero-gate-dielectric tunneling field-effect transistors. Semiconductor Science and Technology, 2013, 28, 052001.	2.0	37

#	Article	IF	Citations
19	Monolithic Three-Dimensional 65-nm CMOS-Nanoelectromechanical Reconfigurable Logic for Sub-1.2-V Operation. IEEE Electron Device Letters, 2017, 38, 1317-1320.	3.9	31
20	Three-Dimensional Integration of Complementary Metal-Oxide-Semiconductor-Nanoelectromechanical Hybrid Reconfigurable Circuits. IEEE Electron Device Letters, 2015, 36, 887-889.	3.9	28
21	Comparative Study of Tunneling Field-Effect Transistors and Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2010, 49, 04DJ12.	1.5	25
22	Investigation on the Corner Effect of <I>L</I>-Shaped Tunneling Field-Effect Transistors and Their Fabrication Method. Journal of Nanoscience and Nanotechnology, 2013, 13, 6376-6381.	0.9	23
23	Nonvolatile Nanoelectromechanical Memory Switches for Low-Power and High-Speed Field-Programmable Gate Arrays. IEEE Transactions on Electron Devices, 2015, 62, 673-679.	3.0	23
24	Electrical characteristics of FinFET with vertically nonuniform source/drain doping profile. IEEE Nanotechnology Magazine, 2002, 1, 233-237.	2.0	22
25	A Novel Capacitorless 1T DRAM Cell for Data Retention Time Improvement. IEEE Nanotechnology Magazine, 2011, 10, 462-466.	2.0	21
26	Hump Effects of Germanium/Silicon Heterojunction Tunnel Field-Effect Transistors. IEEE Transactions on Electron Devices, 2016, 63, 2583-2588.	3.0	20
27	Design and Fabrication of Asymmetric MOSFETs Using a Novel Self-Aligned Structure. IEEE Transactions on Electron Devices, 2007, 54, 2969-2974.	3.0	17
28	Effect of Device Parameters on the Breakdown Voltage of Impact-Ionization Metalâ€“Oxideâ€“Semiconductor Devices. Japanese Journal of Applied Physics, 2009, 48, 040203.	1.5	17
29	Design Guidelines for Gate-Normal Hetero-Gate-Dielectric (GHG) Tunnel Field-Effect Transistors (TFETs). IEEE Access, 2020, 8, 67617-67624.	4.2	17
30	Novel Tunneling Devices with Multi-Functionality. Japanese Journal of Applied Physics, 2007, 46, 2622-2625.	1.5	16
31	Integration Process of Impact-Ionization Metalâ€“Oxideâ€“Semiconductor Devices with Tunneling Field-Effect-Transistors and Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2007, 46, 122-124.	1.5	15
32	Influence of Intercell Trapped Charge on Vertical NAND Flash Memory. IEEE Electron Device Letters, 2017, 38, 164-167.	3.9	15
33	Vertical-Structured Electron-Hole Bilayer Tunnel Field-Effect Transistor for Extremely Low-Power Operation With High Scalability. IEEE Transactions on Electron Devices, 2018, 65, 2010-2015.	3.0	15
34	Stable Threshold Voltage Extraction Using Tikhonov's Regularization Theory. IEEE Transactions on Electron Devices, 2004, 51, 1833-1839.	3.0	14
35	80nm self-aligned complementary I-MOS using double sidewall spacer and elevated drain structure and its applicability to amplifiers with high linearity. , 0, , .		14
36	Improved compact model for double-gate tunnel field-effect transistors by the rigorous consideration of gate fringing field. Japanese Journal of Applied Physics, 2017, 56, 084301.	1.5	13

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37	Nanoelectromechanical Memory Cell (T Cell) for Low-Cost Embedded Nonvolatile Memory Applications. IEEE Transactions on Electron Devices, 2011, 58, 1264-1267.	3.0	12
38	Encapsulation of NEM Memory Switches for Monolithic-Three-Dimensional (M3D) CMOSâ€“NEM Hybrid Circuits. Micromachines, 2018, 9, 317.	2.9	12
39	Novel Gate-All-Around Metalâ€“Oxideâ€“Semiconductor Field Effect Transistors with Self-Aligned Structure. Japanese Journal of Applied Physics, 2007, 46, 2046-2049.	1.5	11
40	Design and scaling of nano-electro-mechanical non-volatile memory (NEMory) cells. Current Applied Physics, 2010, 10, 311-316.	2.4	11
41	Three-Dimensional Stackable Electromechanical Nonvolatile Memory Cell (H Cell) for Four-Bit Operation. IEEE Electron Device Letters, 2010, 31, 29-31.	3.9	11
42	Scaling Trend of Nanoelectromechanical (NEM) Nonvolatile Memory Cells Based on Finite Element Analysis (FEA). IEEE Nanotechnology Magazine, 2011, 10, 647-651.	2.0	10
43	Radio Frequency Performance of Hetero-Gate-Dielectric Tunneling Field-Effect Transistors. Japanese Journal of Applied Physics, 2011, 50, 124301.	1.5	10
44	A unified model for unipolar resistive random access memory. Applied Physics Letters, 2012, 100, .	3.3	10
45	Active directional beaming by mechanical actuation of double-sided plasmonic surface gratings. Optics Letters, 2013, 38, 3827.	3.3	10
46	Radio Frequency Performance of Hetero-Gate-Dielectric Tunneling Field-Effect Transistors. Japanese Journal of Applied Physics, 2011, 50, 124301.	1.5	10
47	Applications of impact-ionization metalâ€“oxide-semiconductor (I-MOS) devices to circuit design. Current Applied Physics, 2010, 10, 444-451.	2.4	9
48	Subthreshold-swing-adjustable tunneling-field-effect-transistor-based random-access memory for nonvolatile operation. Applied Physics Letters, 2016, 108, .	3.3	9
49	Switching Voltage Analysis of Nanoelectromechanical Memory Switches for Monolithic 3-D CMOS-NEM Hybrid Reconfigurable Logic Circuits. IEEE Transactions on Electron Devices, 2018, 65, 3780-3785.	3.0	9
50	Scaling Trends of Monolithic 3-D Complementary Metalâ€“Oxideâ€“Semiconductor Nanoelectromechanical Reconfigurable Logic Circuits. IEEE Transactions on Electron Devices, 2020, 67, 3861-3867.	3.0	9
51	Characteristics of Gate-All-Around Hetero-Gate-Dielectric Tunneling Field-Effect Transistors. Japanese Journal of Applied Physics, 2012, 51, 06FE03.	1.5	9
52	In-Memory Nearest Neighbor Search With Nanoelectromechanical Ternary Content-Addressable Memory. IEEE Electron Device Letters, 2022, 43, 154-157.	3.9	9
53	Side-Gate Design Optimization of 50 nm MOSFETs with Electrically Induced Source/Drain. Japanese Journal of Applied Physics, 2002, 41, 2345-2347.	1.5	8
54	30â€…nm self-aligned FinFET with large sourceâˆ•drain fan-out structure. Electronics Letters, 2003, 39, 1154.	1.0	8

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55	A new fabrication method for self-aligned nanoscale I-MOS (impact-ionization MOS). , 0, , .		8
56	Effect of source extension junction depth and substrate doping concentration on I-MOS device characteristics. IEEE Transactions on Electron Devices, 2006, 53, 1282-1285.	3.0	8
57	Low-Power Circuit Applicability of Hetero-Gate-Dielectric Tunneling Field-Effect Transistors (HG) Tj ETQq1 1 0.784314 rgBT /Overlock	0.6	8
58	Impact of gate dielectric constant variation on tunnel field-effect transistors (TFETs). Solid-State Electronics, 2016, 116, 88-94.	1.4	8
59	Capacitorless Dynamic Random Access Memory Cell with Highly Scalable Surrounding Gate Structure. Japanese Journal of Applied Physics, 2007, 46, 2143-2147.	1.5	7
60	Reliability of Nanoelectromechanical Nonvolatile Memory (NEMory) Cells. IEEE Electron Device Letters, 2009, 30, 269-271.	3.9	7
61	Characteristics of Gate-All-Around Hetero-Gate-Dielectric Tunneling Field-Effect Transistors. Japanese Journal of Applied Physics, 2012, 51, 06FE03.	1.5	7
62	Germanium electronâ€“hole bilayer tunnel field-effect transistors with a symmetrically arranged double gate. Semiconductor Science and Technology, 2015, 30, 035021.	2.0	7
63	Miller effect suppression of tunnel fieldâ€effect transistors (TFETs) using capacitor neutralisation. Electronics Letters, 2016, 52, 659-661.	1.0	7
64	An Accurate Drain Current Model of Monolayer Transition-Metal Dichalcogenide Tunnel FETs. IEEE Transactions on Electron Devices, 2017, 64, 3502-3507.	3.0	7
65	Island-Style Monolithic Three-Dimensional CMOS-Nanoelectromechanical Logic Circuits. IEEE Electron Device Letters, 2020, 41, 1257-1260.	3.9	7
66	Linearity of Hetero-Gate-Dielectric Tunneling Field-Effect Transistors. Journal of Semiconductor Technology and Science, 2013, 13, 551-555.	0.4	7
67	A Finite Element Model for Bipolar Resistive Random Access Memory. Journal of Semiconductor Technology and Science, 2014, 14, 268-273.	0.4	7
68	EIGENVALUE ANALYSIS OF COMPASS GRADIENT EDGE OPERATORS IN FOURIER DOMAIN. Journal of Circuits, Systems and Computers, 1992, 02, 67-74.	1.5	6
69	Dual random circuit breaker network model with equivalent thermal circuit network. Applied Physics Express, 2014, 7, 024203.	2.4	6
70	Tri-State Nanoelectromechanical Memory Switches for the Implementation of a High-Impedance State. IEEE Access, 2020, 8, 202006-202012.	4.2	6
71	A low-power nanoelectromechanical (NEM) device with Al-doped HfO2-based ferroelectric capacitor. Solid-State Electronics, 2021, 175, 107956.	1.4	6
72	LTPS TFTs with an Amorphous Silicon Buffer Layer and Source/Drain Extension. Electronics (Switzerland), 2021, 10, 29.	3.1	6

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73	Reverse-order source/drain formation with double offset spacer (RODOS) for low-power and high-speed application. IEEE Nanotechnology Magazine, 2003, 2, 210-216.	2.0	5
74	Stable Extraction of Threshold Voltage Using Transconductance Change Method for CMOS Modeling, Simulation and Characterization. Japanese Journal of Applied Physics, 2004, 43, 1759-1762.	1.5	5
75	Investigation on hump effects of L-shaped tunneling filed-effect transistors. , 2012, , .		5
76	Stable extraction of linearity (V/sub IP3/) for nanoscale RF CMOS devices. IEEE Microwave and Wireless Components Letters, 2004, 14, 83-85.	3.2	4
77	Ambipolarity characterization of tunneling field-effect transistors. , 2010, , .		4
78	Design improvement of L-shaped tunneling field-effect transistors. , 2012, , .		4
79	Effects of abnormal cell-to-cell interference on p-type floating gate and control gate NAND flash memory. Japanese Journal of Applied Physics, 2014, 53, 04ED12.	1.5	4
80	Influence of Preferred Gate Metal Grain Orientation on Tunneling FETs. IEEE Transactions on Electron Devices, 2015, 62, 1353-1356.	3.0	4
81	Double bi-material cantilever structures for complex surface plasmon modulation. Optics Express, 2015, 23, 5500.	3.4	4
82	Slingshot Pull-In Operation for Low-Voltage Nanoelectromechanical Memory Switches. IEEE Transactions on Electron Devices, 2019, 66, 2040-2043.	3.0	4
83	Design guideline of tunnel field-effect transistors (TFETs) considering negative differential transconductance (NDT). Solid-State Electronics, 2020, 163, 107659.	1.4	4
84	Influence of Etch Profiles on the Leakage Current and Capacitance of 3-D DRAM Storage Capacitors. Journal of Semiconductor Technology and Science, 2019, 19, 208-213.	0.4	4
85	Pattern multiplication method and the uniformity of nanoscale multiple lines. Journal of Vacuum Science & Technology an Official Journal of the American Vacuum Society B, Microelectronics Processing and Phenomena, 2003, 21, 1491.	1.6	3
86	A Technology-Computer-Aided-Design-Based Reliability Prediction Model for DRAM Storage Capacitors. Micromachines, 2019, 10, 256.	2.9	3
87	Nanoelectromechanical-Switch-Based Ternary Content-Addressable Memory (NEMTCAM). IEEE Transactions on Electron Devices, 2021, 68, 4903-4909.	3.0	3
88	On-current Modeling of 70-nm PMOSFETs Dependent on Hot-carrier Stress Bias Conditions. Journal of Semiconductor Technology and Science, 2018, 18, 131-138.	0.4	3
89	Content-Addressable Memory System Using a Nanoelectromechanical Memory Switch. Electronics (Switzerland), 2022, 11, 481.	3.1	3
90	Stereo matching using hierarchical features for robotic applications. Advanced Robotics, 1995, 10, 1-14.	1.8	2

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91	A new method for stable numerical differentiation. Current Applied Physics, 2009, 9, 1463-1466.	2.4	2
92	Quantitative Analysis of Hump Effects of Gate-All-Around Metalâ€“Oxideâ€“Semiconductor Field-Effect Transistors. Japanese Journal of Applied Physics, 2010, 49, 04DC11.	1.5	2
93	Multibit Operation of Nanoelectromechanical Memory Cells. IEEE Electron Device Letters, 2012, 33, 309-311.	3.9	2
94	L-Shaped Tunneling Field-Effect Transistors for Complementary Logic Applications. IEICE Transactions on Electronics, 2013, E96.C, 634-638.	0.6	2
95	Disturbance characteristics of charge trap flash memory with tunneling field-effect transistor. Japanese Journal of Applied Physics, 2014, 53, 114201.	1.5	2
96	Charge trap length dependence and transconductance characteristics of a 2T SONOS cell. , 2014, , .		2
97	Scaling Down Characteristics of Vertical Channel Phase Change Random Access Memory (VPCRAM). Journal of Semiconductor Technology and Science, 2014, 14, 48-52.	0.4	2
98	Fabrication and Electrical Characterization of Graphene Formed Chemically on Nickel Nano Electro Mechanical System (NEMS) Switch. Journal of Nanoscience and Nanotechnology, 2014, 14, 9418-9424.	0.9	2
99	Effects of drain bias on the statistical variation of double-gate tunnel field-effect transistors. Japanese Journal of Applied Physics, 2017, 56, 04CD01.	1.5	2
100	Negative Capacitance Vacuum Channel Transistors for Low Operating Voltage. Micromachines, 2020, 11, 543.	2.9	2
101	Physically Consistent Method for Calculating Trap-Assisted-Tunneling Current Applied to Line Tunneling Field-Effect Transistor. IEEE Transactions on Electron Devices, 2020, 67, 2106-2112.	3.0	2
102	Modeling of Statistical Variation Effects on DRAM Sense Amplifier Offset Voltage. Micromachines, 2021, 12, 1145.	2.9	2
103	Selection Line Optimization of Nanoelectromechanical (NEM) Memory Switches for Stress Relief. Journal of Semiconductor Technology and Science, 2019, 19, 203-207.	0.4	2
104	Multi-Layer Nanoelectromechanical (NEM) Memory Switches for Multi-Path Routing. IEEE Electron Device Letters, 2022, 43, 162-165.	3.9	2
105	25-nm programmable virtual source/drain MOSFETs using a twin SONOS memory structure. Solid-State Electronics, 2006, 50, 914-919.	1.4	1
106	Breakdown voltage reduction in I-MOS devices. , 2006, , .		1
107	Characterization of surface forces for electro-mechanical memory cells. IEICE Electronics Express, 2010, 7, 827-831.	0.8	1
108	Multi-bit electromechanical memory cell for simple fabrication process. , 2010, , .		1

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109	Design guidelines of tunnelling fieldâ€effect transistors for the suppression of workâ€function variation. Electronics Letters, 2015, 51, 1819-1821.	1.0	1
110	Influence of Number Fluctuation and Position Variation of Channel Dopants and Gate Metal Grains on Tunneling Field-Effect Transistors (TFETs). Journal of Nanoscience and Nanotechnology, 2016, 16, 5255-5258.	0.9	1
111	A sub-0.5 V operating RF low noise amplifier using tunneling-FET. Japanese Journal of Applied Physics, 2017, 56, 020303.	1.5	1
112	2T-SONOS Cell Using Novel Process Integration on HV-CMOS Platform for Versatile Application. , 2019, , .		1
113	Dynamic Slingshot Operation for Low-Operation- Voltage Nanoelectromechanical (NEM) Memory Switches. IEEE Access, 2020, 8, 65683-65688.	4.2	1
114	Nanoelectromechanical-Switch-Based Binary Content-Addressable Memory (NEMBCAM). IEEE Access, 2021, 9, 70214-70220.	4.2	1
115	Analytical Model of Nano-Electromechanical (NEM) Nonvolatile Memory Cells. IEICE Transactions on Electronics, 2012, E95.C, 914-916.	0.6	1
116	Development of a Nano-Electro-Mechanical Memory Simulator. Journal of the Institute of Electronics and Information Engineers, 2012, 49, 122-127.	0.0	1
117	Modeling of Triangular Sacrificial Layer Residue Effect in Nano-Electro-Mechanical Nonvolatile Memory. IEICE Transactions on Electronics, 2013, E96.C, 714-717.	0.6	1
118	Development of sacrificial layer wet etch process of TiNi for nano-electro-mechanical device application. Journal of Semiconductor Technology and Science, 2013, 13, 410-414.	0.4	1
119	Synaptic Tunnel Field-Effect Transistors for Extremely-Low-Power Operation. IEEE Electron Device Letters, 2022, 43, 1149-1152.	3.9	1
120	A new linearity measurement algorithm for sub-micron microwave cmos. , 0, , .		0
121	Reverse-order source/drain formation with double offset spacer (RODOS) for CMOS low-power, high-speed and low-noise amplifiers. , 0, , .		0
122	Nano-scale MOSFETs with programmable virtual source/drain. , 0, , .		0
123	Highly Manufacturable and Reliable 80-nm Gate Twin Silicon-Oxide-Nitride-Oxide-Silicon Memory Transistor. Japanese Journal of Applied Physics, 2005, 44, L1214-L1217.	1.5	0
124	25nm Programmable Virtual Source/Drain MOSFETs Using a Twin SONOS Memory Structure. , 0, , .		0
125	Analysis and modeling of resistive probes. , 2006, , .		0
126	Investigation of resistive probes with high sensitivity. , 2008, , .		0

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127	Self-Aligned Asymmetric Metalâ€“Oxideâ€“Semiconductor Field Effect Transistors Fabricated on Silicon-on-Insulator. Japanese Journal of Applied Physics, 2009, 48, 091201.	1.5	0
128	Nano-electromechanical (NEM) memory cells for highly energy-efficient systems. , 2011, , .		0
129	Novel 1T DRAM Cell for Low-Voltage Operation and Long Data Retention Time. IEICE Transactions on Electronics, 2011, E94-C, 110-115.	0.6	0
130	Distribution of post-breakdown resistance of MOSTFETs. IEICE Electronics Express, 2011, 8, 1309-1314.	0.8	0
131	Investigation of stiction effects in nano-electro-mechanical (NEM) memory cells based on finite element analysis (FEA). , 2012, , .		0
132	Dependency of NAND flash memory cells on random dopant fluctuation (RDF) effects. , 2012, , .		0
133	Reduction of ambipolar characteristics of vertical channel tunneling field-effect transistor by using dielectric sidewall. Semiconductor Science and Technology, 2013, 28, 115002.	2.0	0
134	Influence of Fringe Field on Nano-Electromechanical (NEM) Memory Cells. IEEE Nanotechnology Magazine, 2014, 13, 1102-1106.	2.0	0
135	Bit-to-Bit Interference of Multibit Nanoelectromechanical Memory Cells (T Cells). IEEE Nanotechnology Magazine, 2014, 13, 659-666.	2.0	0
136	Scale Effects on Stiction-Induced Release Voltage Shift of Nano-Electromechanical (NEM) Memory Cells. Journal of Nanoscience and Nanotechnology, 2014, 14, 9589-9593.	0.9	0
137	Random Telegraph Noise Model of Tunnel Field-Effect Transistors. Journal of Nanoscience and Nanotechnology, 2016, 16, 10264-10267.	0.9	0
138	Esaki-Tunneling-Assisted Tunnel Field-Effect Transistors for Sub-0.7-V Operation. Journal of Nanoscience and Nanotechnology, 2016, 16, 10237-10240.	0.9	0
139	Influence of the Source Doping Concentration on the Subthreshold Swing (<I>S</I>) of Tunneling Field-Effect Transistors (TFETs). Journal of Nanoscience and Nanotechnology, 2016, 16, 10241-10246.	0.9	0
140	Monolithic 3D (M3D) reconfigurable logic applications using extremely-low-power electron devices. , 2017, , .		0
141	Monolithic three-dimensional tunnel FETâ€“nanoelectromechanical hybrid reconfigurable logic circuits. Japanese Journal of Applied Physics, 2017, 56, 04CD12.	1.5	0
142	Influence of line-edge roughness on multiple-gate tunnel field-effect transistors. Japanese Journal of Applied Physics, 2017, 56, 04CD06.	1.5	0
143	Monolithic 3D (M3D) Complementary Metal-Oxide-Semiconductor (CMOS)-Nanoelectromechanical (NEM) Hybrid Circuits. , 2018, , .		0
144	Compact Potential Model for Si_{1â^'x}Ge_x/Si Heterojunction Double-Gate Tunnel Field-Effect Transistors (TFETs). Journal of Nanoscience and Nanotechnology, 2018, 18, 5953-5958.	0.9	0

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145	Active Region Formation of Nanoelectromechanical (NEM) Devices for Complementary-Metal-Oxide-Semiconductor-NEM Co-Integration. Journal of Nanoscience and Nanotechnology, 2019, 19, 6123-6127.	0.9	0
146	Investigation on the Hump Behavior of Gate-Normal Nanowire Tunnel Field-Effect Transistors (NWTFETs). Applied Sciences (Switzerland), 2020, 10, 8880.	2.5	0
147	Fringe Field Effects on Transient Characteristics of Nano-Electromechanical (NEM) Nonvolatile Memory Cells. Journal of Semiconductor Technology and Science, 2014, 14, 609-614.	0.4	0
148	On-State Resistance Instability of Programmed Antifuse Cells during Read Operation. Journal of Semiconductor Technology and Science, 2014, 14, 503-507.	0.4	0
149	Pull-In Voltage Modeling of Graphene Formed Nickel Nano Electro Mechanical Systems (NEMS). Journal of Semiconductor Technology and Science, 2015, 15, 647-652.	0.4	0
150	Multi-Bit Nano-Electromechanical Nonvolatile Memory Cells (Zigzag T Cells) for the Suppression of Bit-to-Bit Interference. Journal of Nanoscience and Nanotechnology, 2016, 16, 5164-5167.	0.9	0
151	Influence of Electron and Hole Distribution on 2T SONOS Embedded NVM. Journal of Semiconductor Technology and Science, 2016, 16, 624-629.	0.4	0
152	Drain-current Modeling of Sub-70-nm PMOSFETs Dependent on Hot-carrier Stress Bias Conditions. Journal of Semiconductor Technology and Science, 2017, 17, 94-100.	0.4	0
153	Nanoelectromechanical Nonvolatile Memory Cells with Scaled Beam Dimensions. Journal of Nanoelectronics and Optoelectronics, 2017, 12, 1134-1136.	0.5	0
154	Lateral Nanoelectromechanical Relays for Reconfigurable Logic. Journal of Nanoelectronics and Optoelectronics, 2017, 12, 1402-1405.	0.5	0
155	Notched Anchor Design for Low Voltage Operation of Nanoelectromechanical (NEM) Memory Switches. Journal of Nanoscience and Nanotechnology, 2020, 20, 4198-4202.	0.9	0
156	Monolithic-3D (M3D) Complementary Metal-Oxide-Semiconductor-Nanoelectromechanical (CMOS-NEM) Hybrid Reconfigurable Logic (RL) Circuits. Journal of Nanoscience and Nanotechnology, 2020, 20, 4176-4181.	0.9	0
157	Reliability of Nanoelectromechanical Nonvolatile Memory (NEMory) Cells. IEEE Electron Device Letters, 2009, , .	3.9	0