Irith Pomeranz

List of Publications by Year
in descending order

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267	1,414	623188 14	752256 20
papers	citations	h-index	g-index

267	267	267	191
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Topping Off Test Sets Under Bounded Transparent Scan. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 341-345.	1.9	1
2	GEPDFs: Path Delay Faults Based on Two-Cycle Gate-Exhaustive Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2315-2322.	1.9	2
3	Efficient Identification of Undetectable Two-Cycle Gate-Exhaustive Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 776-783.	1.9	1
4	Static Test Compaction Using Independent Suffixes of a Transparent-Scan Sequence. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1130-1141.	1.9	0
5	Multicycle Tests With Fault Detection Test Data for Improved Logic Diagnosis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1587-1591.	1.9	2
6	Pass/Fail Data for Logic Diagnosis Under Bounded Transparent Scan. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 4862-4872.	1.9	0
7	Storage-Based Logic Built-in Self-Test With Multicycle Tests. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 3553-3557.	1.9	0
8	Wrapping Paths of Undetected Transition Faults with Two-Cycle Gate-Exhaustive Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, , 1-1.	1.9	0
9	Compaction of Compressed Bounded Transparent-Scan Test Sets. , 2022, , .		0
10	Algorithms for the Selection of Applied Tests when a Stored Test Produces Many Applied Tests. , 2022, , .		0
11	Test Sequences for Faults in the Scan Logic. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 1568-1572.	2.1	0
12	Fast Test Generation for Structurally Similar Circuits. , 2022, , .		5
13	Preponing Fault Detections for Test Compaction Under Transparent Scan. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 1543-1547.	2.1	1
14	Storage-Based Built-In Self-Test for Gate-Exhaustive Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2189-2193.	1.9	8
15	Test Compaction by Backward and Forward Extension of Multicycle Tests. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 242-246.	2.1	0
16	PRESERVE: Static Test Compaction that Preserves Individual Numbers of Tests. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 803-807.	1.9	1
17	Maximal Independent Fault Set for Gate-Exhaustive Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 598-602.	1.9	11
18	Hybrid Pass/Fail and Full Fail Data for Reduced Fail Data Volume. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1711-1720.	1.9	5

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19	Padding of <i>LFSR</i> Seeds for Reduced Input Test Data Volume. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1004-1008.	1.9	2
20	Partitioning Functional Test Sequences Into Multicycle Functional Broadside Tests. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 89-99.	2.1	1
21	Single Test Type to Replace Broadside and Skewed-Load Tests for Transition Faults. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 423-433.	2.1	1
22	Logic Diagnosis with Hybrid Fail Data. ACM Transactions on Design Automation of Electronic Systems, 2021, 26, 1-13.	1.9	1
23	Compact Set of LFSR Seeds for Diagnostic Tests. , 2021, , .		1
24	Equivalent Faults under Launch-on-Shift (LOS) Tests with Equal Primary Input Vectors. ACM Transactions on Design Automation of Electronic Systems, 2021, 26, 1-15.	1.9	0
25	Functional Constraints in the Selection of Two-Cycle Gate-Exhaustive Faults for Test Generation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1500-1504.	2.1	0
26	Zoom-In Feature for Storage-Based Logic Built-In Self-Test. , 2021, , .		4
27	Positive and Negative Extra Clocking of LFSR Seeds for Reduced Numbers of Stored Tests. , 2021, , .		0
28	Reverse Low-Power Broadside Tests. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 742-746.	1.9	0
29	Switching Activity of Faulty Circuits in Presence of Multiple Transition Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 936-945.	1.9	0
30	Multicycle Broadside and Skewed-Load Tests for Test Compaction. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 262-266.	1.9	2
31	New Targets for Diagnostic Test Generation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 3035-3043.	1.9	0
32	Broadside Tests for Transition and Stuck-At Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 1739-1743.	1.9	0
33	Globally Functional Transparent-Scan Sequences. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 3012-3022.	1.9	1
34	Selection of Primary Output Vectors to Observe Under Multicycle Tests. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 156-162.	2.1	0
35	Extra Clocking of LFSR Seeds for Improved Path Delay Fault Coverage. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 544-552.	2.1	8
36	Functional Broadside Tests Under Broadcast Scan. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 3139-3143.	1.9	1

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37	Input Test Data Volume Reduction Using Seed Complementation and Multiple LFSRs. , 2020, , .		6
38	Non-Masking Non-Robust Tests for Path Delay Faults. , 2020, , .		1
39	Improving a Test Set to Cover Test Holes by Detecting Gate-Exhaustive Faults. , 2020, , .		0
40	Broad-Brush Compaction for Sequential Test Generation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1940-1944.	2.1	1
41	LFSR-Based Test Generation for Reduced Fail Data Volume. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 5261-5266.	1.9	1
42	RETRO: Reintroducing Tests for Improved Reverse Order Fault Simulation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1930-1934.	2.1	0
43	Direct Computation of LFSR-Based Stored Tests for Broadside and Skewed-Load Tests. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 5238-5246.	1.9	1
44	Selecting Close-to-Functional Path Delay Faults for Test Generation. , 2020, , .		3
45	Diagnostic Test Generation That Addresses Diagnostic Holes. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 335-344.	1.9	0
46	Test Compaction Under Bounded Transparent-Scan. , 2019, , .		8
47	Padding of Multicycle Broadside and Skewed-Load Tests. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2587-2595.	2.1	0
48	Extended Transparent-Scan. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2096-2104.	2.1	2
49	Skewed-Load Tests for Transition and Stuck-at Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1969-1973.	1.9	9
50	Resynthesis for Avoiding Undetectable Faults Based on Design-for-Manufacturability Guidelines. , 2019, , .		5
51	Test Scores for Improving the Accuracy of Logic Diagnosis for Multiple Defects. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1720-1724.	2.1	3
52	Extracting a Close-to-Minimum Multicycle Functional Broadside Test Set From a Functional Test Sequence. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1428-1437.	2.1	0
53	TEA: A Test Generation Algorithm for Designs with Timing Exceptions. , 2019, , .		3
54	Compaction of a Functional Broadside Test Set through the Compaction of a Functional Test Sequence without Sequential Fault Simulation. , 2019, , .		0

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55	Iterative Test Generation for Gate-Exhaustive Faults to Cover the Sites of Undetectable Target Faults. , 2019, , .		5
56	Test Compaction by Test Removal Under Transparent Scan. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 496-500.	2.1	5
57	Invisible-Scan: A Design-for-Testability Approach for Functional Test Sequences. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 2357-2365.	1.9	0
58	LFSR-Based Test Generation for Path Delay Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 345-353.	1.9	6
59	Improving the Resolution of Multiple Defect Diagnosis by Removing and Selecting Tests. , 2018, , .		13
60	On Close-to-Functional Test Sequences. , 2018, , .		0
61	Covering undetected transition fault sites with optimistic unspecified transition faults under multicycle tests. , 2018, , .		3
62	Selecting Functional Test Sequences for Defect Diagnosis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2160-2164.	2.1	1
63	Partially Invariant Patterns for LFSR -Based Generation of Close-to-Functional Broadside Tests. ACM Transactions on Design Automation of Electronic Systems, 2018, 23, 1-18.	1.9	3
64	An Initialization Process to Support Online Testing Based on Output Comparison for Identical Finite-State Machines. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1494-1504.	1.9	2
65	Autonomous Multicycle Tests With Low Storage and Test Application Time Overheads. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1881-1892.	1.9	0
66	Improving the Diagnosability of Scan Chain Faults Under Transparent-Scan by Observation Points. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1278-1287.	1.9	3
67	Observation Points on State Variables for the Compaction of Multicycle Tests. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2567-2571.	2.1	4
68	Static test compaction procedure for large pools of multicycle functional broadside tests. IET Computers and Digital Techniques, 2018, 12, 233-240.	0.9	15
69	Dynamically Determined Preferred Values and a Design-for-Testability Approach for Multiplexer Select Inputs under Functional Test Sequences. ACM Transactions on Design Automation of Electronic Systems, 2018, 23, 1-16.	1.9	0
70	Sequential Test Generation Based on Preferred Primary Input Cubes. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 351-355.	1.9	8
71	Restoration-Based Merging of Functional Test Sequences. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1739-1749.	1.9	2
72	Close-to-Functional Broadside Tests With a Safety Margin. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 2139-2143.	1.9	6

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73	Selecting Replacements for Undetectable Path Delay Faults. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1988-1992.	2.1	4
74	Test Modification for Reduced Volumes of Fail Data. ACM Transactions on Design Automation of Electronic Systems, 2017, 22, 1-17.	1.9	6
75	Using piecewise-functional broadside tests for functional broadside test compaction. , 2017, , .		0
76	Reordering Tests for Efficient Fail Data Collection and Tester Time Reduction. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1497-1505.	2.1	3
77	Static Compaction by Merging of Seeds for LFSR-Based Test Generation. , 2017, , .		0
78	Functional Broadside Test Generation Using a Commercial ATPG Tool. , 2017, , .		3
79	A bridging fault model for line coverage in the presence of undetected transition faults. , 2017, , .		3
80	Clock Sequences for Increasing the Fault Coverage of Functional Test Sequences. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1231-1235.	1.9	2
81	Reconstruction of a functional test sequence for increased fault coverage. IET Computers and Digital Techniques, 2017, 11, 91-99.	0.9	0
82	Identifying Biases of a Defect Diagnosis Procedure. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1215-1225.	1.9	1
83	Test Compaction with Dynamic Updating of Faults for Coverage of Undetected Transition Fault Sites. , 2017, , .		0
84	Test reordering for improved scan chain diagnosis using an enhanced defect diagnosis procedure. , 2017, , .		2
85	POSTT: Path-oriented static test compaction for transition faults in scan circuits. , 2017, , .		2
86	Metric for the ability of functional capture cycles to ensure functional operation conditions. IET Computers and Digital Techniques, 2017, 11, 100-106.	0.9	0
87	Combined input test data volume reduction for mixed broadside and skewedâ€load test sets. IET Computers and Digital Techniques, 2016, 10, 138-145.	0.9	0
88	On the Switching Activity in Faulty Circuits During Test Application. , 2016, , .		3
89	Improving the accuracy of defect diagnosis by adding and removing tests. IET Computers and Digital Techniques, 2016, 10, 47-53.	0.9	0
90	A Compact Set of Seeds for LFSR-Based Test Generation from a Fully-Specified Compact Test Set. , 2016, , .		2

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91	LFSR-Based Generation of Multicycle Tests. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, , 1-1.	1.9	1
92	Static test compaction for circuits with multiple independent scan chains. IET Computers and Digital Techniques, 2016, 10, 12-17.	0.9	1
93	Reduction of diagnostic fail data volume and tester time using a dynamic N-cover algorithm. , 2016, , .		14
94	A convergent procedure for partially-reachable states. , 2016, , .		0
95	Balancing the Numbers of Detected Faults for Improved Test Set Quality. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 337-341.	1.9	1
96	Improving the Accuracy of Defect Diagnosis with Multiple Sets of Candidate Faults. IEEE Transactions on Computers, 2016, 65, 2332-2338.	2.4	2
97	A Test Selection Procedure for Improving the Accuracy of Defect Diagnosis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2759-2767.	2.1	9
98	Static Test Compaction for Functional Test Sequences With Restoration of Functional Switching Activity. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1755-1762.	1.9	0
99	-Based Generation of Partially-Functional Broadside Tests. IEEE Transactions on Computers, 2016, 65, 2659-2664.	2.4	5
100	Diagnostic Fail Data Minimization Using an N-Cover Algorithm. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1198-1202.	2.1	7
101	A Joint Diagnostic Test Generation Procedure with Dynamic Test Compaction. , 2016, , .		7
102	Reducing the Storage Requirements of a Set of Functional Test Sequences by Using a Background Sequence. , 2015, , .		0
103	Computing Seeds for LFSR-Based Test Generation From Nontest Cubes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, , 1-5.	2.1	1
104	Piecewise-functional broadside tests based on intersections of reachable states. , 2015, , .		1
105	Test compaction by test cube merging for four-way bridging faults. , 2015, , .		2
106	Test Vector Omission for Fault Coverage Improvement of Functional Test Sequences. IEEE Transactions on Computers, 2015, 64, 3317-3321.	2.4	0
107	Static Test Compaction for Low-Power Test Sets by Increasing the Switching Activity. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1936-1940.	2.1	2
108	Test Compaction by Sharing of Functional Test Sequences Among Logic Blocks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 3006-3014.	2.1	0

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109	A Multicycle Test Set Based on a Two-Cycle Test Set With Constant Primary Input Vectors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1124-1132.	1.9	22
110	Use of input necessary assignments for test generation based on merging of test cubes. IET Computers and Digital Techniques, 2015, 9, 106-112.	0.9	0
111	Improving the accuracy of defect diagnosis by considering reduced diagnostic information. , 2015, , .		4
112	A definition of the number of detections for faults with single tests in a compact scan-based test set. , 2015, , .		0
113	Modeling a Set of Functional Test Sequences as a Single Sequence for Test Compaction. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2629-2638.	2.1	3
114	Two-Dimensional Static Test Compaction for Functional Test Sequences. IEEE Transactions on Computers, 2015, 64, 3009-3015.	2.4	2
115	Generation of close-to-functional broadside tests with equal primary input vectors. , 2015, , .		10
116	Test vector omission with minimal sets of simulated faults. , 2015, , .		0
117	Piecewise-Functional Broadside Tests Based on Reachable States. IEEE Transactions on Computers, 2015, 64, 2415-2420.	2.4	11
118	Computation of Seeds for LFSR-Based Diagnostic Test Generation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 2004-2012.	1.9	14
119	Skewed-Load Test Cubes Based on Functional Broadside Tests for a Low-Power Test Set. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 593-597.	2.1	7
120	Test and non-test cubes for diagnostic test generation based on merging of test cubes. , 2014, , .		0
121	Unknown Output Values of Faulty Circuits and Output Response Compaction. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 323-327.	1.9	1
122	On the use of multi-cycle tests for storage of two-cycle broadside tests. , 2014, , .		7
123	Reducing the input test data volume under transparent scan. IET Computers and Digital Techniques, 2014, 8, 1-10.	0.9	2
124	Multiâ€cycle broadside tests with runs of constant primary input vectors. IET Computers and Digital Techniques, 2014, 8, 90-96.	0.9	2
125	Substituting transition faults with path delay faults as a basic delay fault model. , 2014, , .		0
126	A distance-based test cube merging procedure for compatible and incompatible test cubes. , 2014, , .		0

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127	Static Test Compaction for Scan Circuits by Using Restoration to Modify and Remove Tests. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1955-1964.	1.9	8
128	Test and non-test cubes for diagnostic test generation based on merging of test cubes. , 2014, , .		0
129	Improving the Accuracy of Defect Diagnosis by Considering Fewer Tests. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 2010-2014.	1.9	21
130	Restoration-Based Procedures With Set Covering Heuristics for Static Test Compaction of Functional Test Sequences. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 779-791.	2.1	6
131	Test Compaction by Sharing of Transparent-Scan Sequences Among Logic Blocks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 792-802.	2.1	2
132	Functional Broadside Tests for Multistep Defect Diagnosis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1429-1433.	1.9	1
133	Input Test Data Volume Reduction for Skewed-Load Tests by Additional Shifting of Scan-In States. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 638-642.	1.9	9
134	OBO: An Output-by-Output Scoring Algorithm for Fault Diagnosis. , 2014, , .		19
135	Simultaneous Generation of Functional and Low-Power Non-Functional Broadside Tests. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1245-1257.	1.9	3
136	Fault simulation with test switching for static test compaction. , 2014, , .		4
137	Selection of Functional Test Sequences With Overlaps. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1095-1099.	1.9	1
138	FDPIC: Generation of Functional Test Sequences Based on Fault-Dependent Primary Input Cubes. , 2014, , .		0
139	Low-Power Diagnostic Test Sets for Transition Faults Based on Functional Broadside Tests. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 2427-2431.	2.1	1
140	Low-Power Test Generation by Merging of Functional Broadside Test Cubes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1570-1582.	2.1	14
141	Sharing Logic for Built-In Generationof Functional Broadside Tests. IEEE Transactions on Computers, 2014, 63, 1048-1054.	2.4	0
142	Substituting transition faults with path delay faults as a basic delay fault model. , 2014, , .		0
143	Path selection based on static timing analysis considering input necessary assignments. , 2013, , .		1
144	Functional Broadside Tests With Incompletely Specified Scan-In States. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 1445-1449.	1.9	5

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145	An Adjacent Switching Activity Metric under Functional Broadside Tests. IEEE Transactions on Computers, 2013, 62, 404-410.	2.4	3
146	Signal-Transition Patterns of Functional Broadside Tests. IEEE Transactions on Computers, 2013, 62, 2544-2549.	2.4	7
147	Generation of compact multi-cycle diagnostic test sets. , 2013, , .		1
148	Classes of difficult-to-diagnose transition fault clusters. , 2013, , .		1
149	On Test Compaction of Broadside and Skewed-Load Test Cubes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1705-1714.	2.1	10
150	On Candidate Fault Sets for Fault Diagnosis and Dominance Graphs of Equivalence Classes. , 2013, , .		0
151	Generation of Functional Broadside Tests for Logic Blocks With Constrained Primary Input Sequences. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 442-452.	1.9	9
152	Built-In Generation of Functional Broadside Tests Using a Fixed Hardware Structure. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 124-132.	2.1	9
153	Reduced Power Transition Fault Test Sets for Circuits With Independent Scan Chain Modes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1354-1359.	2.1	3
154	Computing Two-Pattern Test Cubes for Transition Path Delay Faults. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 475-485.	2.1	0
155	Broadside and Skewed-Load Tests Under Primary Input Constraints. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 776-780.	2.1	0
156	Functional Broadside Templates for Low-Power Test Generation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 2321-2325.	2.1	3
157	Transition Fault Simulation Considering Broadside Tests as Partially-Functional Broadside Tests. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1359-1363.	2.1	4
158	Static test compaction for mixed broadside and skewedâ€load transition fault test sets. IET Computers and Digital Techniques, 2013, 7, 21-28.	0.9	3
159	On multiâ€cycle test cubes. IET Computers and Digital Techniques, 2013, 7, 182-189.	0.9	0
160	Non-Test Cubes for Test Generation Targeting Hard-to-Detect Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 1957-1965.	1.9	1
161	Generation of Mixed Test Sets for Transition Faults. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1895-1899.	2.1	10
162	Non-Uniform Coverage by n-Detection Test Sets. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 2138-2142.	2.1	4

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163	Generation and compaction of mixed broadside and skewed-load n-detection test sets for transition faults. , 2012, , .		1
164	Resolution of Diagnosis Based on Transition Faults. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 172-176.	2.1	1
165	Static test compaction for transition faults under the hazard-based detection conditions. , 2012, , .		0
166	On the detection of path delay faults by functional broadside tests. , 2012, , .		9
167	Built-in generation of multi-cycle broadside tests. , 2012, , .		0
168	TSV and DFT cost aware circuit partitioning for 3D-SOCs. , 2012, , .		2
169	Performance aware partitioning for 3D-SOCs. , 2012, , .		3
170	Gradual Diagnostic Test Generation and Observation Point Insertion Based on the Structural Distance Between Indistinguished Fault Pairs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1026-1035.	2.1	11
171	A Metric for Identifying Detectable Path Delay Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1734-1742.	1.9	4
172	Multi-Pattern n-Detection Stuck-At Test Sets for Delay Defect Coverage. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1156-1160.	2.1	3
173	Multicycle Tests With Constant Primary Input Vectors for Increased Fault Coverage. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1428-1438.	1.9	9
174	Concatenation of Functional Test Subsequences for Improved Fault Coverage and Reduced Test Length. IEEE Transactions on Computers, 2012, 61, 899-904.	2.4	11
175	Fast Identification of Undetectable Transition Faults under Functional Broadside Tests. IEEE Transactions on Computers, 2012, 61, 905-910.	2.4	1
176	On the Switching Activity and Static Test Compaction of Multicycle Scan-Based Tests. IEEE Transactions on Computers, 2012, 61, 1179-1188.	2.4	2
177	On the Computation of Common Test Data for Broadside and Skewed-Load Tests. IEEE Transactions on Computers, 2012, 61, 578-583.	2.4	18
178	Multipattern Scan-Based Test Sets With Small Numbers of Primary Input Sequences. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 322-326.	1.9	1
179	Static test compaction for delay fault test sets consisting of broadside and skewed-load tests. , 2011, , .		29
180	On clustering of undetectable transition faults in standard-scan circuits. , 2011, , .		1

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181	On Transition Fault Diagnosis Using Multicycle At-Speed Broadside Tests. , 2011, , .		4
182	Augmenting Functional Broadside Tests for Transition Fault Coverage with Bounded Switching Activity. , 2011, , .		12
183	Generation of Mixed Broadside and Skewed-Load Diagnostic Test Sets for Transition Faults. , 2011, , .		10
184	On Functional Broadside Tests With Functional Propagation Conditions. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1094-1098.	2.1	2
185	Built-in generation of functional broadside tests. , 2011, , .		4
186	Input Necessary Assignments for Testing of Path Delay Faults in Standard-Scan Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 333-337.	2.1	12
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