Irith Pomeranz

List of Publications by Year
in descending order

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267	1,414	623188	752256
papers	citations	14	20
		h-index	g-index

267	267	267	191
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	On static compaction of test sequences for synchronous sequential circuits. , 1996, , .		101
2	On the generation of small dictionaries for fault location. , 1992, , .		82
3	On the generation of scan-based test sets with reachable states for testing under functional operation conditions. , 2004, , .		54
4	Primary Input Vectors to Avoid in Random Test Sequences for Synchronous Sequential Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 193-197.	1.9	42
5	Transition Path Delay Faults: A New Path Delay Fault Model for Small and Large Delay Defects. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 98-107.	2.1	36
6	On Selecting Testable Paths in Scan Designs. Journal of Electronic Testing: Theory and Applications (JETTA), 2003, 19, 447-456.	0.9	32
7	Static test compaction for delay fault test sets consisting of broadside and skewed-load tests. , 2011, , .		29
8	A Functional Coverage Metric for Estimating the Gate-Level Fault Coverage of Functional Tests. IEEE International Test Conference (TC), 2006, , .	0.0	25
9	Unspecified Transition Faults: A Transition Fault Model for At-Speed Fault Simulation and Test Generation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 137-146.	1.9	22
10	A Multicycle Test Set Based on a Two-Cycle Test Set With Constant Primary Input Vectors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1124-1132.	1.9	22
11	Hazard-Based Detection Conditions for Improved Transition Fault Coverage of Scan-Based Tests. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 333-337.	2.1	21
12	Improving the Accuracy of Defect Diagnosis by Considering Fewer Tests. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 2010-2014.	1.9	21
13	ATPG Heuristics Dependant Observation Point Insertion for Enhanced Compaction and Data Volume Reduction. , 2008, , .		20
14	Generation of Multi-Cycle Broadside Tests. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 1253-1257.	1.9	20
15	OBO: An Output-by-Output Scoring Algorithm for Fault Diagnosis. , 2014, , .		19
16	Estimating the Fault Coverage of Functional Test Sequences Without Fault Simulation. , 2007, , .		18
17	On the Computation of Common Test Data for Broadside and Skewed-Load Tests. IEEE Transactions on Computers, 2012, 61, 578-583.	2.4	18
18	On Test Generation With Test Vector Improvement. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 502-506.	1.9	17

#	Article	IF	Citations
19	Static test compaction procedure for large pools of multicycle functional broadside tests. IET Computers and Digital Techniques, 2018, 12, 233-240.	0.9	15
20	On reset based functional broadside tests. , 2010, , .		14
21	Static Test Data Volume Reduction Using Complementation or Modulo-M Addition. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1108-1112.	2.1	14
22	Low-Power Test Generation by Merging of Functional Broadside Test Cubes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1570-1582.	2.1	14
23	Computation of Seeds for LFSR-Based Diagnostic Test Generation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 2004-2012.	1.9	14
24	Reduction of diagnostic fail data volume and tester time using a dynamic N-cover algorithm. , 2016, , .		14
25	Improving the Resolution of Multiple Defect Diagnosis by Removing and Selecting Tests. , 2018, , .		13
26	On Complete Functional Broadside Tests for Transition Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 583-587.	1.9	12
27	Switching Activity as a Test Compaction Heuristic for Transition Faults. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1357-1361.	2.1	12
28	Augmenting Functional Broadside Tests for Transition Fault Coverage with Bounded Switching Activity. , 2011, , .		12
29	Input Necessary Assignments for Testing of Path Delay Faults in Standard-Scan Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 333-337.	2.1	12
30	TOV: Sequential Test Generation by Ordering of Test Vectors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 454-465.	1.9	11
31	Output-Dependent Diagnostic Test Generation. , 2010, , .		11
32	Gradual Diagnostic Test Generation and Observation Point Insertion Based on the Structural Distance Between Indistinguished Fault Pairs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1026-1035.	2.1	11
33	Concatenation of Functional Test Subsequences for Improved Fault Coverage and Reduced Test Length. IEEE Transactions on Computers, 2012, 61, 899-904.	2.4	11
34	Piecewise-Functional Broadside Tests Based on Reachable States. IEEE Transactions on Computers, 2015, 64, 2415-2420.	2.4	11
35	Maximal Independent Fault Set for Gate-Exhaustive Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 598-602.	1.9	11
36	z-Diagnosis: A Framework for Diagnostic Fault Simulation and Test Generation Utilizing Subsets of Outputs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1700-1712.	1.9	10

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37	Diagnostic Test Generation Based on Subsets of Faults. Proceedings of the IEEE European Test Workshop, 2007, , .	0.0	10
38	Forming multi-cycle tests for delay faults by concatenating broadside tests. , 2010, , .		10
39	Path Selection for Transition Path Delay Faults. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 401-409.	2.1	10
40	Generation of Mixed Broadside and Skewed-Load Diagnostic Test Sets for Transition Faults. , 2011, , .		10
41	Generation of Mixed Test Sets for Transition Faults. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1895-1899.	2.1	10
42	On Test Compaction of Broadside and Skewed-Load Test Cubes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1705-1714.	2.1	10
43	Generation of close-to-functional broadside tests with equal primary input vectors. , 2015, , .		10
44	Equivalence and Dominance Relations Between Fault Pairs and Their Use in Fault Pair Collapsing for Fault Diagnosis. , 2007, , .		9
45	Hazard-Based Detection Conditions for Improved Transition Path Delay Fault Coverage. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1449-1453.	1.9	9
46	On the detection of path delay faults by functional broadside tests. , 2012, , .		9
47	Multicycle Tests With Constant Primary Input Vectors for Increased Fault Coverage. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1428-1438.	1.9	9
48	Generation of Functional Broadside Tests for Logic Blocks With Constrained Primary Input Sequences. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 442-452.	1.9	9
49	Built-In Generation of Functional Broadside Tests Using a Fixed Hardware Structure. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 124-132.	2.1	9
50	Input Test Data Volume Reduction for Skewed-Load Tests by Additional Shifting of Scan-In States. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 638-642.	1.9	9
51	A Test Selection Procedure for Improving the Accuracy of Defect Diagnosis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2759-2767.	2.1	9
52	Skewed-Load Tests for Transition and Stuck-at Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1969-1973.	1.9	9
53	Scan Shift Power of Functional Broadside Tests. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 1416-1420.	1.9	8
54	Static Test Compaction for Scan Circuits by Using Restoration to Modify and Remove Tests. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1955-1964.	1.9	8

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55	Sequential Test Generation Based on Preferred Primary Input Cubes. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 351-355.	1.9	8
56	Test Compaction Under Bounded Transparent-Scan. , 2019, , .		8
57	Extra Clocking of LFSR Seeds for Improved Path Delay Fault Coverage. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 544-552.	2.1	8
58	Storage-Based Built-In Self-Test for Gate-Exhaustive Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2189-2193.	1.9	8
59	On Clustering of Undetectable Single Stuck-At Faults and Test Quality in Full-Scan Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1135-1140.	1.9	7
60	Hyper-graph based partitioning to reduce DFT cost for pre-bond 3D-IC testing. , 2011, , .		7
61	Signal-Transition Patterns of Functional Broadside Tests. IEEE Transactions on Computers, 2013, 62, 2544-2549.	2.4	7
62	On the use of multi-cycle tests for storage of two-cycle broadside tests. , 2014, , .		7
63	Skewed-Load Test Cubes Based on Functional Broadside Tests for a Low-Power Test Set. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 593-597.	2.1	7
64	Diagnostic Fail Data Minimization Using an N-Cover Algorithm. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1198-1202.	2.1	7
65	A Joint Diagnostic Test Generation Procedure with Dynamic Test Compaction. , 2016, , .		7
66	Enhanced Broadside Testing for Improved Transition Fault Coverage. , 2007, , .		6
67	Generation of Broadside Transition-Fault Test Sets That Detect Four-Way Bridging Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1311-1319.	1.9	6
68	Improving the Transition Fault Coverage of Functional Broadside Tests by Observation Point Insertion. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 931-936.	2.1	6
69	Safe Fault Collapsing Based on Dominance Relations. , 2008, , .		6
70	Forward-Looking Reverse Order Fault Simulation for n -Detection Test Sets. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 1424-1428.	1.9	6
71	Restoration-Based Procedures With Set Covering Heuristics for Static Test Compaction of Functional Test Sequences. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 779-791.	2.1	6
72	Close-to-Functional Broadside Tests With a Safety Margin. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 2139-2143.	1.9	6

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73	Test Modification for Reduced Volumes of Fail Data. ACM Transactions on Design Automation of Electronic Systems, 2017, 22, 1-17.	1.9	6
74	LFSR-Based Test Generation for Path Delay Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 345-353.	1.9	6
75	Input Test Data Volume Reduction Using Seed Complementation and Multiple LFSRs. , 2020, , .		6
76	Fault Detection by Output Response Comparison of Identical Circuits Using Half-Frequency Compatible Sequences. IEEE International Test Conference (TC), 2006, , .	0.0	5
77	Design-for-Testability for Improved Path Delay Fault Coverage of Critical Paths. , 2008, , .		5
78	Hazard-Based Detection Conditions for Improved Transition Fault Coverage of Functional Test Sequences. , 2009, , .		5
79	Doubleâ€“Single Stuck-at Faults: A Delay Fault Model for Synchronous Sequential Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 426-432.	1.9	5
80	Gradual Diagnostic Test Generation Based on the Structural Distance between Indistinguished Fault Pairs. , 2010, , .		5
81	Functional Broadside Tests With Incompletely Specified Scan-In States. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 1445-1449.	1.9	5
82	-Based Generation of Partially-Functional Broadside Tests. IEEE Transactions on Computers, 2016, 65, 2659-2664.	2.4	5
83	Resynthesis for Avoiding Undetectable Faults Based on Design-for-Manufacturability Guidelines. , 2019, , .		5
84	Iterative Test Generation for Gate-Exhaustive Faults to Cover the Sites of Undetectable Target Faults. , 2019, , .		5
85	Test Compaction by Test Removal Under Transparent Scan. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 496-500.	2.1	5
86	Hybrid Pass/Fail and Full Fail Data for Reduced Fail Data Volume. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1711-1720.	1.9	5
87	Fast Test Generation for Structurally Similar Circuits. , 2022, , .		5
88	Diagnostic Test Generation Targeting Equivalence Classes. , 2007, , .		4
89	On the saturation of n-detection test sets with increased n. , 2007, , .		4
90	Robust Fault Models Where Undetectable Faults Imply Logic Redundancy. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1230-1234.	2.1	4

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91	On Transition Fault Diagnosis Using Multicycle At-Speed Broadside Tests. , 2011, , .		4
92	Built-in generation of functional broadside tests. , 2011, , .		4
93	Reducing the Storage Requirements of a Test Sequence by Using One or Two Background Vectors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1755-1764.	2.1	4
94	Non-Uniform Coverage by n-Detection Test Sets. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 2138-2142.	2.1	4
95	A Metric for Identifying Detectable Path Delay Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1734-1742.	1.9	4
96	Transition Fault Simulation Considering Broadside Tests as Partially-Functional Broadside Tests. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1359-1363.	2.1	4
97	Fault simulation with test switching for static test compaction. , 2014, , .		4
98	Improving the accuracy of defect diagnosis by considering reduced diagnostic information. , 2015, , .		4
99	Selecting Replacements for Undetectable Path Delay Faults. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1988-1992.	2.1	4
100	Observation Points on State Variables for the Compaction of Multicycle Tests. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2567-2571.	2.1	4
101	Zoom-In Feature for Storage-Based Logic Built-In Self-Test. , 2021, , .		4
102	Semi-Concurrent On-Line Testing of Transition Faults Through Output Response Comparison of Identical Circuits. , 2007, , .		3
103	Selection of a Fault Model for Fault Diagnosis Based on Unique Responses. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1533-1543.	2.1	3
104	Equivalence, Dominance, and Similarity Relations between Fault Pairs and a Fault Pair Collapsing Process for Fault Diagnosis. IEEE Transactions on Computers, 2010, 59, 150-158.	2.4	3
105	Subsets of Primary Input Vectors in Sequential Test Generation for Single Stuck-at Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 1579-1583.	1.9	3
106	Performance aware partitioning for 3D-SOCs. , 2012, , .		3
107	Multi-Pattern n-Detection Stuck-At Test Sets for Delay Defect Coverage. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1156-1160.	2.1	3
108	An Adjacent Switching Activity Metric under Functional Broadside Tests. IEEE Transactions on Computers, 2013, 62, 404-410.	2.4	3

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109	Reduced Power Transition Fault Test Sets for Circuits With Independent Scan Chain Modes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1354-1359.	2.1	3
110	Functional Broadside Templates for Low-Power Test Generation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 2321-2325.	2.1	3
111	Static test compaction for mixed broadside and skewedâ€load transition fault test sets. IET Computers and Digital Techniques, 2013, 7, 21-28.	0.9	3
112	Simultaneous Generation of Functional and Low-Power Non-Functional Broadside Tests. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1245-1257.	1.9	3
113	Modeling a Set of Functional Test Sequences as a Single Sequence for Test Compaction. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2629-2638.	2.1	3
114	On the Switching Activity in Faulty Circuits During Test Application. , 2016, , .		3
115	Reordering Tests for Efficient Fail Data Collection and Tester Time Reduction. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1497-1505.	2.1	3
116	Functional Broadside Test Generation Using a Commercial ATPG Tool. , 2017, , .		3
117	A bridging fault model for line coverage in the presence of undetected transition faults. , 2017, , .		3
118	Covering undetected transition fault sites with optimistic unspecified transition faults under multicycle tests. , 2018, , .		3
119	Partially Invariant Patterns for LFSR -Based Generation of Close-to-Functional Broadside Tests. ACM Transactions on Design Automation of Electronic Systems, 2018, 23, 1-18.	1.9	3
120	Improving the Diagnosability of Scan Chain Faults Under Transparent-Scan by Observation Points. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1278-1287.	1.9	3
121	Test Scores for Improving the Accuracy of Logic Diagnosis for Multiple Defects. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1720-1724.	2.1	3
122	TEA: A Test Generation Algorithm for Designs with Timing Exceptions. , 2019, , .		3
123	Selecting Close-to-Functional Path Delay Faults for Test Generation. , 2020, , .		3
124	A Delay Fault Model for At-Speed Fault Simulation and Test Generation. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	2
125	Synthesis for Broadside Testability of Transition Faults. VLSI Test Symposium (VTS), Proceedings, IEEE, 2008, , .	1.0	2
126	Expanded Definition of Functional Operation Conditions and its Effects on the Computation of Functional Broadside Tests. VLSI Test Symposium (VTS), Proceedings, IEEE, 2008, , .	1.0	2

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127	Random Test Generation With Input Cube Avoidance. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 45-54.	2.1	2
128	Selecting state variables for improved on-line testability through output response comparison of identical circuits. , 2010, , .		2
129	Functional and partially-functional skewed-load tests. , 2010, , .		2
130	On multiple bridging faults. , 2010, , .		2
131	On Functional Broadside Tests With Functional Propagation Conditions. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1094-1098.	2.1	2
132	Broadside and Functional Broadside Tests for Partial-Scan Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1104-1108.	2.1	2
133	TSV and DFT cost aware circuit partitioning for 3D-SOCs. , 2012, , .		2
134	On the Switching Activity and Static Test Compaction of Multicycle Scan-Based Tests. IEEE Transactions on Computers, 2012, 61, 1179-1188.	2.4	2
135	Reducing the input test data volume under transparent scan. IET Computers and Digital Techniques, 2014, 8, 1-10.	0.9	2
136	Multiâ€cycle broadside tests with runs of constant primary input vectors. IET Computers and Digital Techniques, 2014, 8, 90-96.	0.9	2
137	Test Compaction by Sharing of Transparent-Scan Sequences Among Logic Blocks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 792-802.	2.1	2
138	Test compaction by test cube merging for four-way bridging faults. , 2015, , .		2
139	Static Test Compaction for Low-Power Test Sets by Increasing the Switching Activity. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1936-1940.	2.1	2
140	Two-Dimensional Static Test Compaction for Functional Test Sequences. IEEE Transactions on Computers, 2015, 64, 3009-3015.	2.4	2
141	A Compact Set of Seeds for LFSR-Based Test Generation from a Fully-Specified Compact Test Set. , 2016, , .		2
142	Improving the Accuracy of Defect Diagnosis with Multiple Sets of Candidate Faults. IEEE Transactions on Computers, 2016, 65, 2332-2338.	2.4	2
143	Restoration-Based Merging of Functional Test Sequences. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1739-1749.	1.9	2
144	Clock Sequences for Increasing the Fault Coverage of Functional Test Sequences. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1231-1235.	1.9	2

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145	Test reordering for improved scan chain diagnosis using an enhanced defect diagnosis procedure. , 2017, , .		2
146	POSTT: Path-oriented static test compaction for transition faults in scan circuits. , 2017, , .		2
147	An Initialization Process to Support Online Testing Based on Output Comparison for Identical Finite-State Machines. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1494-1504.	1.9	2
148	Extended Transparent-Scan. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2096-2104.	2.1	2
149	Multicycle Broadside and Skewed-Load Tests for Test Compaction. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 262-266.	1.9	2
150	Padding of LFSR Seeds for Reduced Input Test Data Volume. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1004-1008.	1.9	2
151	GEPDFs: Path Delay Faults Based on Two-Cycle Gate-Exhaustive Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2315-2322.	1.9	2
152	Multicycle Tests With Fault Detection Test Data for Improved Logic Diagnosis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1587-1591.	1.9	2
153	Test data volume reduction by test data realignment. , 2003, , .		1
154	Scan-Based Delay Fault Tests for Diagnosis of Transition Faults. Defect and Fault Tolerance in VLSI Systems, Proceedings of the IEEE International Symposium on, 2006, , .	0.0	1
155	Invariant States and Redundant Logic in Synchronous Sequential Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1171-1175.	1.9	1
156	A-Diagnosis: A Complement to Z-Diagnosis. , 2007, , .		1
157	Autoscan-Invert: An Improved Scan Design without External Scan Inputs or Outputs. VLSI Test Symposium (VTS), Proceedings, IEEE, 2007, , .	1.0	1
158	On Test Generation by Input Cube Avoidance. , 2007, , .		1
159	Functional Broadside Tests with Different Levels of Reachability. , 2007, , .		1
160	A Bridging Fault Model Where Undetectable Faults Imply Logic Redundancy. , 2008, , .		1
161	Input Cubes with Lingering Synchronization Effects and their Use in Random Sequential Test Generation. , 2009, , .		1
162	Selection of a fault model for fault diagnosis based on unique responses. , 2009, , .		1

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163	Functional Broadside Tests Under an Expanded Definition of Functional Operation Conditions. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 121-129.	1.9	1
164	On clustering of undetectable transition faults in standard-scan circuits. , 2011, , .		1
165	Generation and compaction of mixed broadside and skewed-load n-detection test sets for transition faults. , 2012, , .		1
166	Resolution of Diagnosis Based on Transition Faults. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 172-176.	2.1	1
167	Fast Identification of Undetectable Transition Faults under Functional Broadside Tests. IEEE Transactions on Computers, 2012, 61, 905-910.	2.4	1
168	Multipattern Scan-Based Test Sets With Small Numbers of Primary Input Sequences. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 322-326.	1.9	1
169	Path selection based on static timing analysis considering input necessary assignments. , 2013, , .		1
170	Generation of compact multi-cycle diagnostic test sets. , 2013, , .		1
171	Classes of difficult-to-diagnose transition fault clusters. , 2013, , .		1
172	Non-Test Cubes for Test Generation Targeting Hard-to-Detect Faults. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 1957-1965.	1.9	1
173	Unknown Output Values of Faulty Circuits and Output Response Compaction. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 323-327.	1.9	1
174	Functional Broadside Tests for Multistep Defect Diagnosis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1429-1433.	1.9	1
175	Selection of Functional Test Sequences With Overlaps. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1095-1099.	1.9	1
176	Low-Power Diagnostic Test Sets for Transition Faults Based on Functional Broadside Tests. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 2427-2431.	2.1	1
177	Computing Seeds for LFSR-Based Test Generation From Nontest Cubes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, , 1-5.	2.1	1
178	Piecewise-functional broadside tests based on intersections of reachable states. , 2015, , .		1
179	LFSR-Based Generation of Multicycle Tests. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, , 1-1.	1.9	1
180	Static test compaction for circuits with multiple independent scan chains. IET Computers and Digital Techniques, 2016, 10, 12-17.	0.9	1

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181	Balancing the Numbers of Detected Faults for Improved Test Set Quality. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 337-341.	1.9	1
182	Identifying Biases of a Defect Diagnosis Procedure. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1215-1225.	1.9	1
183	Selecting Functional Test Sequences for Defect Diagnosis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2160-2164.	2.1	1
184	Globally Functional Transparent-Scan Sequences. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 3012-3022.	1.9	1
185	Functional Broadside Tests Under Broadcast Scan. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 3139-3143.	1.9	1
186	Non-Masking Non-Robust Tests for Path Delay Faults. , 2020, , .		1
187	Broad-Brush Compaction for Sequential Test Generation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1940-1944.	2.1	1
188	LFSR-Based Test Generation for Reduced Fail Data Volume. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 5261-5266.	1.9	1
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