Juan Duarte

List of Publications by Year
in descending order

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27	986	516710 16	713466 21
papers	citations	h-index	g-index

27	27	27	974
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	BSIM-HV: High-Voltage MOSFET Model Including Quasi-Saturation and Self-Heating Effect. IEEE Transactions on Electron Devices, 2019, 66, 4258-4263.	3.0	23
2	Designing 0.5 V 5-nm HP and 0.23 V 5-nm LP NC-FinFETs With Improved ${I}_{ mathrm{scriptscriptstyle OFF}}$ Sensitivity in Presence of Parasitic Capacitance. IEEE Transactions on Electron Devices, 2018, 65, 1211-1216.	3.0	31
3	Engineering Negative Differential Resistance in NCFETs for Analog Applications. IEEE Transactions on Electron Devices, 2018, 65, 2033-2039.	3.0	79
4	New Mobility Model for Accurate Modeling of Transconductance in FDSOI MOSFETs. IEEE Transactions on Electron Devices, 2018, 65, 463-469.	3.0	5
5	Modeling of Advanced RF Bulk FinFETs. IEEE Electron Device Letters, 2018, 39, 791-794.	3.9	17
6	Effect of Polycrystallinity and Presence of Dielectric Phases on NC-FinFET Variability. , 2018, , .		14
7	Response Speed of Negative Capacitance FinFETs. , 2018, , .		29
8	A Unified Flicker Noise Model for FDSOI MOSFETs Including Back-bias Effect. , 2018, , .		7
9	Variation Caused by Spatial Distribution of Dielectric and Ferroelectric Grains in a Negative Capacitance Field-Effect Transistor. IEEE Transactions on Electron Devices, 2018, 65, 4652-4658.	3.0	29
10	NCFET Design Considering Maximum Interface Electric Field. IEEE Electron Device Letters, 2018, 39, 1254-1257.	3.9	33
11	A Predictive Tunnel FET Compact Model With Atomistic Simulation Validation. IEEE Transactions on Electron Devices, 2017, 64, 599-605.	3.0	20
12	Compact Modeling Source-to-Drain Tunneling in Sub-10-nm GAA FinFET With Industry Standard Model. IEEE Transactions on Electron Devices, 2017, 64, 3576-3581.	3.0	13
13	Modeling of Back-Gate Effects on Gate-Induced Drain Leakage and Gate Currents in UTB SOI MOSFETs. IEEE Transactions on Electron Devices, 2017, 64, 3986-3990.	3.0	9
14	Impact of Parasitic Capacitance and Ferroelectric Parameters on Negative Capacitance FinFET Characteristics. IEEE Electron Device Letters, 2017, 38, 142-144.	3.9	71
15	Thermal resistance modeling in FDSOI transistors with industry standard model BSIM-IMG. Microelectronics Journal, 2016, 56, 171-176.	2.0	19
16	RF Modeling of FDSOI Transistors Using Industry Standard BSIM-IMG Model. IEEE Transactions on Microwave Theory and Techniques, 2016, 64, 1745-1751.	4.6	34
17	Negative Capacitance in Short-Channel FinFETs Externally Connected to an Epitaxial Ferroelectric Capacitor. IEEE Electron Device Letters, 2016, 37, 111-114.	3.9	198
18	Modeling SiGe FinFETs With Thin Fin and Current-Dependent Source/Drain Resistance. IEEE Electron Device Letters, 2015, 36, 636-638.	3.9	7

#	Article	IF	Citations
19	Modeling STI Edge Parasitic Current for Accurate Circuit Simulations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1291-1294.	2.7	11
20	BSIM-IMG: Compact model for RF-SOI MOSFETs. , 2015, , .		13
21	Capacitance Modeling in IIIâ€“V FinFETs. IEEE Transactions on Electron Devices, 2015, 62, 3892-3897.	3.0	25
22	Modeling 20-nm Germanium FinFET With the Industry Standard FinFET Model. IEEE Electron Device Letters, 2014, 35, 711-713.	3.9	20
23	BSIM6: Analog and RF Compact Model for Bulk MOSFET. IEEE Transactions on Electron Devices, 2014, 61, 234-244.	3.0	105
24	Modeling of GaN-Based Normally-Off FinFET. IEEE Electron Device Letters, 2014, 35, 612-614.	3.9	40
25	BSIM-IMG with improved surface potential calculation recipe. , 2014, , .		5
26	BSIMâ€”SPICE Models Enable FinFET and UTB IC Designs. IEEE Access, 2013, 1, 201-215.	4.2	101
27	Unified FinFET compact model: Modelling Trapezoidal Triple-Gate FinFETs. , 2013, , .		28