Suman Datta

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/499780/publications.pdf

Version: 2024-02-01

367 papers	15,738 citations	28274 55 h-index	27406 106 g-index
374 all docs	374 docs citations	374 times ranked	11265 citing authors

#	Article	IF	Citations
1	Theory of ballistic nanotransistors. IEEE Transactions on Electron Devices, 2003, 50, 1853-1864.	3.0	652
2	Two-dimensional gallium nitride realized via grapheneÂencapsulation. Nature Materials, 2016, 15, 1166-1171.	27.5	626
3	Benchmarking Nanotechnology for High-Performance and Low-Power Logic Transistor Applications. IEEE Nanotechnology Magazine, 2005, 4, 153-158.	2.0	583
4	High-<tex>$kappa$</tex>/Metalâ€“Gate Stack and Its MOSFET Characteristics. IEEE Electron Device Letters, 2004, 25, 408-410.	3.9	422
5	The future of ferroelectric field-effect transistor technology. Nature Electronics, 2020, 3, 588-597.	26.0	398
6	High performance fully-depleted tri-gate CMOS transistors. IEEE Electron Device Letters, 2003, 24, 263-265.	3.9	387
7	Atomically thin resonant tunnel diodes built from synthetic van der Waals heterostructures. Nature Communications, 2015, 6, 7311.	12.8	382
8	The era of hyper-scaling in electronics. Nature Electronics, 2018, 1, 442-450.	26.0	375
9	Integrated nanoelectronics for the future. Nature Materials, 2007, 6, 810-812.	27.5	350
10	Ferroelectric FET analog synapse for acceleration of deep neural network training. , 2017, , .		322
11	A steep-slope transistor based on abrupt electronic phase transition. Nature Communications, 2015, 6, 7812.	12.8	294
12	Critical Role of Interlayer in Hf_{0.5}Zr_{0.5}O₂ Ferroelectric FET Nonvolatile Memory Performance. IEEE Transactions on Electron Devices, 2018, 65, 2461-2469.	3.0	284
13	A Numerical Study of Scaling Issues for Schottky-Barrier Carbon Nanotube Transistors. IEEE Transactions on Electron Devices, 2004, 51, 172-177.	3.0	263
14	Ferroelectric ternary content-addressable memory for one-shot learning. Nature Electronics, 2019, 2, 521-529.	26.0	217
15	Temperature-Dependent Iâ€“ V Characteristics of a Vertical $hbox{In}_{0.53}hbox{Ga}_{0.47}hbox{As}$ Tunnel FET. IEEE Electron Device Letters, 2010, 31, 564-566.	3.9	203
16	On the performance limits for Si MOSFETs: a theoretical study. IEEE Transactions on Electron Devices, 2000, 47, 232-240.	3.0	197
17	Effective Capacitance and Drive Current for Tunnel FET (TFET) CV/I Estimation. IEEE Transactions on Electron Devices, 2009, 56, 2092-2098.	3.0	197
18	On Enhanced Miller Capacitance Effect in Interband Tunnel Transistors. IEEE Electron Device Letters, 2009, 30, 1102-1104.	3.9	188

#	Article	IF	Citations
19	Transport Effects on Signal Propagation in Quantum Wires. IEEE Transactions on Electron Devices, 2005, 52, 1734-1742.	3.0	167
20	Tunnel FET technology: A reliability perspective. Microelectronics Reliability, 2014, 54, 861-874.	1.7	155
21	Synchronized charge oscillations in correlated electron systems. Scientific Reports, 2014, 4, .	3.3	155
22	Scaling Length Theory of Double-Gate Interband Tunnel Field-Effect Transistors. IEEE Transactions on Electron Devices, 2012, 59, 902-908.	3.0	153
23	A simple quantum mechanical treatment of scattering in nanoscale transistors. Journal of Applied Physics, 2003, 93, 5613-5625.	2.5	152
24	Fermi level depinning and contact resistivity reduction using a reduced titania interlayer in n-silicon metal-insulator-semiconductor ohmic contacts. Applied Physics Letters, 2014, 104, .	3.3	145
25	Tri-Gate fully-depleted CMOS transistors: fabrication, design and layout. , 0, , .		136
26	Atomically Thin Heterostructures Based on Single-Layer Tungsten Diselenide and Graphene. Nano Letters, 2014, 14, 6936-6941.	9.1	132
27	Electrically Driven Reversible Insulatorâ€“Metal Phase Transition in 1T-TaS₂. Nano Letters, 2015, 15, 1861-1866.	9.1	131
28	Enhancing the magnetoelectric response of Metglas/polyvinylidene fluoride laminates by exploiting the flux concentration effect. Applied Physics Letters, 2009, 95, .	3.3	126
29	A Circuit Compatible Accurate Compact Model for Ferroelectric-FETs. , 2018, , .		120
30	Probing electronic excitations in molecular conduction. Physical Review B, 2006, 73, .	3.2	114
31	Variation-tolerant ultra low-power heterojunction tunnel FET SRAM design. , 2011, , .		114
32	A ferroelectric field effect transistor based synaptic weight cell. Journal Physics D: Applied Physics, 2018, 51, 434001.	2.8	113
33	Ultrathin ferroic HfO2â€“ZrO2 superlattice gate stack for advanced transistors. Nature, 2022, 604, 65-71.	27.8	108
34	Physics-Based Circuit-Compatible SPICE Model for Ferroelectric Transistors. IEEE Electron Device Letters, 2016, , 1-1.	3.9	106
35	Roadmap on emerging hardware and technology for machine learning. Nanotechnology, 2021, 32, 012002.	2.6	104
36	Sub-kT/q Switching in Strong Inversion in PbZr_{0.52}Ti_{0.48}O₃ Gated Negative Capacitance FETs. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2015, 1, 43-48.	1.5	101

#	Article	IF	Citations
37	Joule Heating-Induced Metalâ€“Insulator Transition in Epitaxial VO₂/TiO₂ Devices. ACS Applied Materials & Interfaces, 2016, 8, 12908-12914.	8.0	101
38	Vertex coloring of graphs via phase dynamics of coupled oscillatory networks. Scientific Reports, 2017, 7, 911.	3.3	93
39	Nonvolatile memory design based on ferroelectric FETs. , 2016, , .		91
40	Transport properties of ultra-thin VO2 films on (001) TiO2 grown by reactive molecular-beam epitaxy. Applied Physics Letters, 2015, 107, .	3.3	88
41	SoC Logic Compatible Multi-Bit FeMFET Weight Cell for Neuromorphic Applications. , 2018, , .		88
42	Barrier-Engineered Arsenideâ€“Antimonide Heterojunction Tunnel FETs With Enhanced Drive Current. IEEE Electron Device Letters, 2012, 33, 1568-1570.	3.9	86
43	Device-Circuit Analysis of Ferroelectric FETs for Low-Power Logic. IEEE Transactions on Electron Devices, 2017, 64, 3092-3100.	3.0	86
44	â€œNegative capacitanceâ€•in resistor-ferroelectric and ferroelectric-dielectric networks: Apparent or intrinsic?. Journal of Applied Physics, 2018, 123, .	2.5	82
45	Current-voltage characteristics of molecular conductors: two versus three terminal. IEEE Nanotechnology Magazine, 2002, 1, 145-153.	2.0	79
46	Opportunities in vanadium-based strongly correlated electron systems. MRS Communications, 2017, 7, 27-52.	1.8	77
47	Indiumâ€“Tin-Oxide Transistors with One Nanometer Thick Channel and Ferroelectric Gating. ACS Nano, 2020, 14, 11542-11547.	14.6	75
48	Time-Resolved Measurement of Negative Capacitance. IEEE Electron Device Letters, 2018, 39, 272-275.	3.9	74
49	An Ultra-Dense 2FeFET TCAM Design Based on a Multi-Domain FeFET Model. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1577-1581.	3.0	74
50	Back-End-of-Line Compatible Transistors for Monolithic 3-D Integration. IEEE Micro, 2019, 39, 8-15.	1.8	73
51	Enabling Energy-Efficient Nonvolatile Computing With Negative Capacitance FET. IEEE Transactions on Electron Devices, 2017, 64, 3452-3458.	3.0	72
52	Write Disturb in Ferroelectric FETs and Its Implication for 1T-FeFET AND Memory Arrays. IEEE Electron Device Letters, 2018, 39, 1656-1659.	3.9	72
53	Exploiting Hybrid Precision for Training and Inference: A 2T-1FeFET Based Analog Synaptic Weight Cell. , 2018, , .		71
54	Tunnel FET RF Rectifier Design for Energy Harvesting Applications. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2014, 4, 400-411.	3.6	70

#	Article	IF	Citations
55	Quantum mechanical analysis of channel access geometry and series resistance in nanoscale transistors. Journal of Applied Physics, 2004, 95, 292-305.	2.5	69
56	Electrostatics of nanowire transistors. IEEE Nanotechnology Magazine, 2003, 2, 329-334.	2.0	68
57	Modeling and Simulation of Vanadium Dioxide Relaxation Oscillators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 2207-2215.	5.4	65
58	Impact of total and partial dipole switching on the switching slope of gate-last negative capacitance FETs with ferroelectric hafnium zirconium oxide gate stack. , 2017, , .		65
59	Small-Signal Response of Inversion Layers in High-Mobility $hbox{In}_{0.53}hbox{Ga}_{0.47}hbox{As}$ MOSFETs Made With Thin High- $kappa$ Dielectrics. IEEE Transactions on Electron Devices, 2010, 57, 742-748.	3.0	64
60	A unified model for insulator selection to form ultra-low resistivity metal-insulator-semiconductor contacts to n-Si, n-Ge, and n-InGaAs. Applied Physics Letters, 2012, 101, 042108.	3.3	64
61	A novel Si-Tunnel FET based SRAM design for ultra low-power 0.3V VDD applications. , 2010, , .		62
62	Phase field modeling of domain dynamics and polarization accumulation in ferroelectric HZO. Applied Physics Letters, 2019, 114, .	3.3	60
63	Molecules on silicon: Self-consistent first-principles theory and calibration to experiments. Physical Review B, 2005, 72, .	3.2	59
64	Pairwise coupled hybrid vanadium dioxide-MOSFET (HVFET) oscillators for non-boolean associative computing. , 2014, , .		59
65	Experimental demonstration of 100nm channel length In<inf>0.53</inf>Ga<inf>0.47</inf>As-based vertical inter-band tunnel field effect transistors (TFETs) for ultra low-power logic and SRAM applications. , 2009, , .		58
66	Supervised Learning in All FeFET-Based Spiking Neural Network: Opportunities and Challenges. Frontiers in Neuroscience, 2020, 14, 634.	2.8	58
67	Analysis of DIBL Effect and Negative Resistance Performance for NCFET Based on a Compact SPICE Model. IEEE Transactions on Electron Devices, 2018, 65, 5525-5529.	3.0	57
68	Computing With Networks of Oscillatory Dynamical Systems. Proceedings of the IEEE, 2019, 107, 73-89.	21.3	57
69	An Ising Hamiltonian solver based on coupled stochastic phase-transition nano-oscillators. Nature Electronics, 2021, 4, 502-512.	26.0	57
70	Monolithic 3D Integration of High Endurance Multi-Bit Ferroelectric FET for Accelerating Compute-In-Memory. , 2020, , .		56
71	Quantitative Mapping of Phase Coexistence in Mott-Peierls Insulator during Electronic and Thermally Driven Phase Transition. ACS Nano, 2015, 9, 2009-2017.	14.6	55
72	Experimental Demonstration of Ferroelectric Spiking Neurons for Unsupervised Clustering. , 2018, , .		55

#	Article	IF	Citations
73	Electrical Noise in Heterojunction Interband Tunnel FETs. IEEE Transactions on Electron Devices, 2014, 61, 552-560.	3.0	54
74	Programmable coupled oscillators for synchronized locomotion. Nature Communications, 2019, 10, 3299.	12.8	52
75	Synchronization of pairwise-coupled, identical, relaxation oscillators based on metal-insulator phase transition devices: A model study. Journal of Applied Physics, 2015, 117, .	2.5	51
76	Design and Analysis of an Ultra-Dense, Low-Leakage, and Fast FeFET-Based Random Access Memory Array. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2019, 5, 103-112.	1.5	50
77	Demonstration of improved heteroepitaxy, scaled gate stack and reduced interface states enabling heterojunction tunnel FETs with high drive current and high on-off ratio. , 2012, , .		49
78	Advancing Nonvolatile Computing With Nonvolatile NCFET Latches and Flip-Flops. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2907-2919.	5.4	49
79	0.5 V Supply Voltage Operation of In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}Tunnel FET. IEEE Electron Device Letters, 2015, 36, 20-22.	3.9	48
80	Exploiting ferroelectric FETs for low-power non-volatile logic-in-memory circuits. , 2016, , .		48
81	Design of Nonvolatile SRAM with Ferroelectric FETs for Energy-Efficient Backup and Restore. IEEE Transactions on Electron Devices, 2017, 64, 3037-3040.	3.0	48
82	Computing with ferroelectric FETs: Devices, models, systems, and applications. , 2018, , .		48
83	Fundamental Understanding and Control of Device-to-Device Variation in Deeply Scaled Ferroelectric FETs. , 2019, , .		48
84	First principles calculations of intrinsic mobilities in tin-based oxide semiconductors SnO, SnO2, and Ta2SnO6. Journal of Applied Physics, 2019, 126, .	2.5	47
85	Comparative Study of Si, Ge and InAs based Steep SubThreshold Slope Tunnel Transistors for 0.25V Supply Voltage Logic Applications. , 2008, , .		46
86	Steep switching tunnel FET: A promise to extend the energy efficient roadmap for post-CMOS digital and analog/RF applications. , 2013, , .		46
87	FerroElectronics for Edge Intelligence. IEEE Micro, 2020, 40, 33-48.	1.8	46
88	Exploiting Heterogeneity for Energy Efficiency in Chip Multiprocessors. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2011, 1, 109-119.	3.6	45
89	Demonstration of MOSFET-like on-current performance in arsenide/antimonide tunnel FETs with staggered hetero-junctions for 300mV logic applications. , 2011, , .		45
90	Soft-Error Performance Evaluation on Emerging Low Power Devices. IEEE Transactions on Device and Materials Reliability, 2014, 14, 732-741.	2.0	45

#	Article	IF	Citations
91	Ferroelectric transistor model based on self-consistent solution of 2D Poisson's, non-equilibrium Green's function and multi-domain Landau Khalatnikov equations. , 2017, , .		45
92	Insight into the output characteristics of III-V tunneling field effect transistors. Applied Physics Letters, 2013, 102, 092105.	3.3	44
93	Steep-Slope Devices: From Dark to Dim Silicon. IEEE Micro, 2013, 33, 50-59.	1.8	44
94	Novel insb-based quantum well transistors for ultra-high speed, low power logic applications. , 0, , .		43
95	Imprinting of Local Metallic States into VO₂ with Ultraviolet Light. Advanced Functional Materials, 2016, 26, 6612-6618.	14.9	43
96	Assessment of silicon MOS and carbon nanotube FET performance limits using a general theory of ballistic transistors. , 0, , .		41
97	Opportunities and Challenges of Tunnel FETs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 2128-2138.	5.4	40
98	Utilization of Negative-Capacitance FETs to Boost Analog Circuit Performances. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2855-2860.	3.1	40
99	Intrinsic electronic switching time in ultrathin epitaxial vanadium dioxide thin film. Applied Physics Letters, 2013, 102, .	3.3	39
100	Neuro-Mimetic Dynamics of a Ferroelectric FET-Based Spiking Neuron. IEEE Electron Device Letters, 2019, 40, 1213-1216.	3.9	39
101	Impact of Transistor Architecture (Bulk Planar, Trigate on Bulk, Ultrathin-Body Planar SOI) and Material (Silicon or IIIâ€“V Semiconductor) on Variation for Logic and SRAM Applications. IEEE Transactions on Electron Devices, 2013, 60, 3298-3304.	3.0	38
102	Influence of Body Effect on Sample-and-Hold Circuit Design Using Negative Capacitance FET. IEEE Transactions on Electron Devices, 2018, 65, 3909-3914.	3.0	38
103	Nanoscale Transistorsâ€”Just Around the Gate?. Science, 2013, 341, 140-141.	12.6	37
104	Revisiting the Theory of Ferroelectric Negative Capacitance. IEEE Transactions on Electron Devices, 2016, 63, 2043-2049.	3.0	37
105	The non-equilibrium Green's function (NEGF) formalism: An elementary introduction. , 0, , .		36
106	Electron Transport in Multigate In_xGa_{1â€“x} As Nanowire FETs: From Diffusive to Ballistic Regimes at Room Temperature. Nano Letters, 2014, 14, 626-633.	9.1	36
107	Ferroelectric Transistor based Non-Volatile Flip-Flop. , 2016, , .		35
108	Device Circuit Co Design of FEFET Based Logic for Low Voltage Processors. , 2016, , .		35

#	Article	IF	Citations
109	IIIâ€“V Tunnel FET Model With Closed-Form Analytical Solution. IEEE Transactions on Electron Devices, 2016, 63, 2163-2168.	3.0	35
110	Stochastic Insulator-to-Metal Phase Transition-Based True Random Number Generator. IEEE Electron Device Letters, 2018, 39, 139-142.	3.9	35
111	Rf-powered systems using steep-slope devices. , 2014, , .		34
112	Application of Silicon-Germanium Source Tunnel-FET to Enable Ultralow Power Cellular Neural Network-Based Associative Memory. IEEE Transactions on Electron Devices, 2014, 61, 3707-3715.	3.0	34
113	Modeling and in Situ Probing of Surface Reactions in Atomic Layer Deposition. ACS Applied Materials & Interfaces, 2017, 9, 15848-15856.	8.0	33
114	Logic Compatible High-Performance Ferroelectric Transistor Memory. IEEE Electron Device Letters, 2022, 43, 382-385.	3.9	33
115	Steep Switching Hybrid Phase Transition FETs (Hyper-FET) for Low Power Applications: A Device-Circuit Co-design Perspectiveâ€“Part I. IEEE Transactions on Electron Devices, 2017, 64, 1350-1357.	3.0	32
116	Double-Gate W-Doped Amorphous Indium Oxide Transistors for Monolithic 3D Capacitorless Gain Cell eDRAM. , 2020, , .		32
117	Band offsets determination and interfacial chemical properties of the Al2O3/GaSb system. Applied Physics Letters, 2010, 97, 162109.	3.3	31
118	Defect assistant band alignment transition from staggered to broken gap in mixed As/Sb tunnel field effect transistor heterostructure. Journal of Applied Physics, 2012, 112, .	2.5	31
119	Nanoscale structural evolution of electrically driven insulator to metal transition in vanadium dioxide. Applied Physics Letters, 2013, 103, .	3.3	31
120	Field Effect and Strongly Localized Carriers in the Metal-Insulator Transition MaterialVO2. Physical Review Letters, 2015, 115, 196401.	7.8	31
121	Two-dimensional tantalum disulfide: controlling structure and properties via synthesis. 2D Materials, 2018, 5, 025001.	4.4	31
122	In-Memory Computing Primitive for Sensor Data Fusion in 28 nm HKMG FeFET Technology. , 2018, , .		31
123	Time-Delay Encoded Image Recognition in a Network of Resistively Coupled VOâ„‚ on Si Oscillators. IEEE Electron Device Letters, 2020, 41, 629-632.	3.9	31
124	Stochastic IMT (Insulator-Metal-Transition) Neurons: An Interplay of Thermal and Threshold Noise at Bifurcation. Frontiers in Neuroscience, 2018, 12, 210.	2.8	30
125	Neuro Inspired Computing with Coupled Relaxation Oscillators. , 2014, , .		29
126	Ultra low power coupled oscillator arrays for computer vision applications. , 2016, , .		29

#	Article	IF	Citations
127	Experimental Demonstration of Phase Transition Nano-Oscillator Based Ising Machine. , 2019, , .		29
128	Drain-Erase Scheme in Ferroelectric Field Effect Transistorâ€"Part II: 3-D-NAND Architecture for In-Memory Computing. IEEE Transactions on Electron Devices, 2020, 67, 962-967.	3.0	29
129	Low Thermal Budget (<250 Â°C) Dual-Gate Amorphous Indium Tungsten Oxide (IWO) Thin-Film Transistor for Monolithic 3-D Integration. IEEE Transactions on Electron Devices, 2020, 67, 5336-5342.	3.0	29
130	Ultra Low Power Circuit Design Using Tunnel FETs. , 2012, , .		28
131	Enabling New Computation Paradigms with HyperFET - An Emerging Device. IEEE Transactions on Multi-Scale Computing Systems, 2016, 2, 30-48.	2.4	28
132	Subnanosecond Fluctuations in Low-Barrier Nanomagnets. Physical Review Applied, 2019, 12, .	3.8	28
133	Role of InAs and GaAs terminated heterointerfaces at source/channel on the mixed As-Sb staggered gap tunnel field effect transistor structures grown by molecular beam epitaxy. Journal of Applied Physics, 2012, 112, 024306.	2.5	27
134	Tunnel transistors for energy efficient computing. , 2013, , .		27
135	Exploiting Synchronization Properties of Correlated Electron Devices in a Non-Boolean Computing Fabric for Template Matching. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2014, 4, 450-459.	3.6	27
136	A Steep-Slope Tunnel FET Based SAR Analog-to-Digital Converter. IEEE Transactions on Electron Devices, 2014, 61, 3661-3667.	3.0	27
137	Reliability Studies on High-Temperature Operation of Mixed As/Sb Staggered Gap Tunnel FET Material and Devices. IEEE Transactions on Device and Materials Reliability, 2014, 14, 245-254.	2.0	27
138	Fabrication, Characterization, and Analysis of Ge/GeSn Heterojunction p-Type Tunnel Transistors. IEEE Transactions on Electron Devices, 2017, 64, 4354-4362.	3.0	27
139	A Novel Ferroelectric Superlattice Based Multi-Level Cell Non-Volatile Memory. , 2019, , .		27
140	Technology assessment of Si and III-V FinFETs and III-V tunnel FETs from soft error rate perspective. , 2012, , .		26
141	Tunnel FET-based ultra-low power, high-sensitivity UHF RFID rectifier. , 2013, , .		26
142	Ag/HfO<inf>2</inf> based threshold switch with extreme non-linearity for unipolar cross-point memory and steep-slope phase-FETs. , 2016, , .		26
143	A Multitask Grocery Assist System for the Visually Impaired: Smart glasses, gloves, and shopping carts provide auditory and tactile feedback. IEEE Consumer Electronics Magazine, 2017, 6, 73-81.	2.3	26
144	Design of 2T/Cell and 3T/Cell Nonvolatile Memories with Emerging Ferroelectric FETs. IEEE Design and Test, 2019, 36, 39-45.	1.2	26

#	Article	IF	Citations
145	Hf_{0.5}Zr_{0.5}O₂-Based Ferroelectric Gate HEMTs With Large Threshold Voltage Tuning Range. IEEE Electron Device Letters, 2020, 41, 337-340.	3.9	26
146	Mismatch of Ferroelectric Film on Negative Capacitance FETs Performance. IEEE Transactions on Electron Devices, 2020, 67, 1297-1304.	3.0	26
147	Drainâ€“Erase Scheme in Ferroelectric Field-Effect Transistorâ€”Part I: Device Characterization. IEEE Transactions on Electron Devices, 2020, 67, 955-961.	3.0	26
148	Neural sampling machine with stochastic synapse allows brain-like learning and inference. Nature Communications, 2022, 13, 2571.	12.8	26
149	Reconfigurable BDD based quantum circuits. , 2008, , .		25
150	Impact of Variation in Nanoscale Silicon and Non-Silicon FinFETs and Tunnel FETs on Device and SRAM Performance. IEEE Transactions on Electron Devices, 2015, 62, 1691-1697.	3.0	25
151	Automated mapping for reconfigurable single-electron transistor arrays. , 2011, , .		24
152	26.5 Terahertz electrically triggered RF switch on epitaxial VO2-on-Sapphire (VOS) wafer. , 2015, , .		24
153	Comparative Area and Parasitics Analysis in FinFET and Heterojunction Vertical TFET Standard Cells. ACM Journal on Emerging Technologies in Computing Systems, 2016, 12, 1-23.	2.3	24
154	Steep Switching Hybrid Phase Transition FETs (Hyper-FET) for Low Power Applications: A Device-Circuit Co-design Perspectiveâ€”Part II. IEEE Transactions on Electron Devices, 2017, 64, 1358-1365.	3.0	24
155	Silicon compatible Sn-based resistive switching memory. Nanoscale, 2018, 10, 9441-9449.	5.6	24
156	Performance Enhancement of Ag/HfO₂ Metal Ion Threshold Switch Cross-Point Selectors. IEEE Electron Device Letters, 2019, 40, 1602-1605.	3.9	24
157	First Principles Design of High Hole Mobility p-Type Snâ€“Oâ€“X Ternary Oxides: Valence Orbital Engineering of Sn²⁺ in Sn²⁺â€“Oâ€“X by Selection of Appropriate Elements X. Chemistry of Materials, 2021, 33, 212-225.	6.7	24
158	Full band atomistic modeling of homo-junction InGaAs band-to-band tunneling diodes including band gap narrowing. Applied Physics Letters, 2012, 100, 063504.	3.3	23
159	Fully transparent field-effect transistor with high drain current and on-off ratio. APL Materials, 2020, 8, .	5.1	23
160	Flicker noise characterization and analytical modeling of homo and hetero-junction III–V tunnel FETs. , 2012, , .		22
161	Tunnel FET-based ultra-low power, low-noise amplifier design for bio-signal acquisition. , 2014, , .		22
162	Fundamental mechanism behind volatile and non-volatile switching in metallic conducting bridge RAM. , 2017, , .		22

#	Article	IF	Citations
163	BEOL-Compatible Superlattice FEFET Analog Synapse With Improved Linearity and Symmetry of Weight Update. IEEE Transactions on Electron Devices, 2022, 69, 2094-2100.	3.0	22
164	Ultra low-resistance palladium silicide Ohmic contacts to lightly doped n-InGaAs. Journal of Applied Physics, 2012, 112, 054510.	2.5	21
165	Demonstration of p-type In<inf>0.7</inf>Ga<inf>0.3</inf>As/GaAs<inf>0.35</inf>Sb<inf>0.65</inf> and n-type GaAs<inf>0.4</inf>Sb<inf>0.6</inf>/In<inf>0.65</inf>Ga<inf>0.35</inf>As complimentary Hetero-junction Vertical Tunnel FETs for ultra-low power logic. , 2015, , .		21
166	Lowering Area Overheads for FeFET-Based Energy-Efficient Nonvolatile Flip-Flops. IEEE Transactions on Electron Devices, 2018, 65, 2670-2674.	3.0	21
167	Power and Area Efficient FPGA Building Blocks Based on Ferroelectric FETs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 1780-1793.	5.4	21
168	Conductance in Coulomb blockaded moleculesâ€”fingerprints of wave-particle duality?. Molecular Simulation, 2006, 32, 751-758.	2.0	20
169	Band offset determination of mixed As/Sb type-II staggered gap heterostructure for n-channel tunnel field effect transistor application. Journal of Applied Physics, 2013, 113, 024319.	2.5	20
170	High quality HfO2/p-GaSb(001) metal-oxide-semiconductor capacitors with 0.8â€‰nm equivalent oxide thickness. Applied Physics Letters, 2014, 105, .	3.3	20
171	Dynamics of electrically driven sub-nanosecond switching in vanadium dioxide. , 2016, , .		20
172	Analysis of Functional Oxide based Selectors for Cross-Point Memories. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 2222-2235.	5.4	20
173	Equivalent Oxide Thickness (EOT) Scaling With Hafnium Zirconium Oxide High-Î¤ Dielectric Near Morphotropic Phase Boundary. , 2019, , .		20
174	BEOL Compatible Indium-Tin-Oxide Transistors: Switching of Ultrahigh-Density 2-D Electron Gas Over 0.8 Ã— 10¹⁴/cm² at Oxide/Oxide Interface by the Change of Ferroelectric Polarization. IEEE Transactions on Electron Devices, 2021, 68, 3195-3199.	3.0	20
175	Exploration of vertical MOSFET and tunnel FET device architecture for Sub 10nm node applications. , 2012, , .		19
176	Demonstration of In<inf>0.9</inf>Ga<inf>0.1</inf>As/GaAs<inf>0.18</inf>Sb<inf>0.82</inf> near broken-gap tunnel FET with I<inf>ON</inf>=740μA/μm, G<inf>M</inf>=70μS/μm and gigahertz switching performance at V<inf>Ds</inf>=0.5V. , 2013, , .		19
177	An enumerative method for runlength-limited codes: permutation codes. IEEE Transactions on Information Theory, 1999, 45, 2199-2204.	2.4	18
178	Structural properties and band offset determination of p-channel mixed As/Sb type-II staggered gap tunnel field-effect transistor structure. Applied Physics Letters, 2012, 101, 112106.	3.3	18
179	A Synthesis Algorithm for Reconfigurable Single-Electron Transistor Arrays. ACM Journal on Emerging Technologies in Computing Systems, 2013, 9, 1-20.	2.3	18
180	Design, fabrication, and analysis of p-channel arsenide/antimonide hetero-junction tunnel transistors. Journal of Applied Physics, 2014, 115, .	2.5	18

#	Article	IF	Citations
181	Phase-Transition-FET exhibiting steep switching slope of 8mV/decade and 36% enhanced ON current. , 2016, , .		18
182	Computing with dynamical systems based on insulator-metal-transition oscillators. Nanophotonics, 2017, 6, 601-611.	6.0	18
183	A Threshold Switch Augmented Hybrid-FeFET (H-FeFET) with Enhanced Read Distinguishability and Reduced Programming Voltage for Non-Volatile Memory Applications. , 2018, , .		18
184	Computing with Coupled Oscillators: Theory, Devices, and Applications. , 2018, , .		18
185	A Swarm Optimization Solver Based on Ferroelectric Spiking Neural Networks. Frontiers in Neuroscience, 2019, 13, 855.	2.8	18
186	Investigating Ferroelectric Minor Loop Dynamics and History Effectâ€"Part I: Device Characterization. IEEE Transactions on Electron Devices, 2020, 67, 3592-3597.	3.0	18
187	BEOL Compatible Superlattice FerroFET-based High Precision Analog Weight Cell with Superior Linearity and Symmetry. , 2021, , .		18
188	Molecular Conduction: Paradigms and Possibilities. Journal of Computational Electronics, 2002, 1, 515-525.	2.5	17
189	Energy-Delay Performance of Nanoscale Transistors Exhibiting Single Electron Behavior and Associated Logic Circuits. Journal of Low Power Electronics, 2010, 6, 415-428.	0.6	17
190	Improving energy efficiency of multi-threaded applications using heterogeneous CMOS-TFET multicores. , 2011, , .		16
191	Impact of Sidewall Passivation and Channel Composition on In_{<italic>x</italic>}Ga_{1-<italic>x</italic>}As FinFET Performance. IEEE Electron Device Letters, 2015, 36, 117-119.	3.9	15
192	An Empirically Validated Virtual Source FET Model for Deeply Scaled Cool CMOS. , 2019, , .		15
193	CryoMem: A 4K-300K 1.3GHz eDRAM Macro with Hybrid 2T-Gain-Cell in a 28nm Logic Process for Cryogenic Applications. , 2021, , .		15
194	Investigating Ferroelectric Minor Loop Dynamics and History Effectâ€"Part II: Physical Modeling and Impact on Neural Network Training. IEEE Transactions on Electron Devices, 2020, 67, 3598-3604.	3.0	15
195	Heterojunction Intra-Band Tunnel FETs for Low-Voltage SRAMs. IEEE Transactions on Electron Devices, 2012, 59, 3533-3542.	3.0	14
196	Layout-Dependent Strain Optimization for p-Channel Trigate Transistors. IEEE Transactions on Electron Devices, 2012, 59, 72-78.	3.0	14
197	Heterogeneous integration of hexagonal boron nitride on bilayer quasiâ€freeâ€standing epitaxial graphene and its impact on electrical transport properties. Physica Status Solidi (A) Applications and Materials Science, 2013, 210, 1062-1070.	1.8	14
198	A High-Efficiency Switched-Capacitance HTFET Charge Pump for Low-Input-Voltage Applications. , 2015, , .		14

#	Article	IF	Citations
199	Phase transition oxide neuron for spiking neural networks. , 2016, , .		14
200	Electrically triggered insulator-to-metal phase transition in two-dimensional (2D) heterostructures. Applied Physics Letters, 2018, 113, 142101.	3.3	14
201	Ferroelectrics: From Memory to Computing. , 2020, , .		14
202	Experimental Demonstration of Gate-Level Logic Camouflaging and Run-Time Reconfigurability Using Ferroelectric FET for Hardware Security. IEEE Transactions on Electron Devices, 2021, 68, 516-522.	3.0	14
203	Impact of Single Trap Random Telegraph Noise on Heterojunction TFET SRAM Stability. IEEE Electron Device Letters, 2014, 35, 393-395.	3.9	13
204	Indium arsenide (InAs) single and dual quantum-well heterostructure FinFETs. , 2015, , .		13
205	Insinhts on the DC Characterization of Ferroelectric Field-Effect-Transistors. , 2018, , .		13
206	Biologically Plausible Ferroelectric Quasi-Leaky Integrate and Fire Neuron. , 2019, , .		13
207	The Impact of Ferroelectric FETs on Digital and Analog Circuits and Architectures. IEEE Design and Test, 2020, 37, 79-99.	1.2	13
208	Magnetoelectric Sensors With Directly Integrated Charge Sensitive Readout Circuitâ€"Improved Field Sensitivity and Signal-to-Noise Ratio. IEEE Sensors Journal, 2011, 11, 2260-2265.	4.7	12
209	On Reconfigurable Single-Electron Transistor Arrays Synthesis Using Reordering Techniques. , 2013, , .		12
210	Enabling Power-Efficient Designs with III-V Tunnel FETs. , 2014, , .		12
211	Nanoporous Dielectric Resistive Memories Using Sequential Infiltration Synthesis. ACS Nano, 2021, 15, 4155-4164.	14.6	12
212	Scaled Gate Stacks for Sub-20-nm CMOS Logic Applications Through Integration of Thermal IL and ALD HfOx. IEEE Electron Device Letters, 2013, 34, 3-5.	3.9	11
213	Impact of contact and local interconnect scaling on logic performance. , 2014, , .		11
214	Impact of Varying Indium(x) Concentration and Quantum Confinement on PBTI Reliability in InxGa1-xAs FinFET. IEEE Electron Device Letters, 2015, 36, 120-122.	3.9	11
215	COAST: Correlated material assisted STT MRAMs for optimized read operation. , 2015, , .		11
216	ON-state evolution in lateral and vertical VO₂threshold switching devices. Nanotechnology, 2017, 28, 405201.	2.6	11

#	Article	IF	Citations
217	Hysteresis-free negative capacitance in the multi-domain scenario for logic applications. , 2019, , .		11
218	Optimal block codes for M-ary runlength-constrained channels. IEEE Transactions on Information Theory, 2001, 47, 2069-2078.	2.4	10
219	Structural, morphological, and defect properties of metamorphic In0.7Ga0.3As/GaAs0.35Sb0.65 p-type tunnel field effect transistor structure grown by molecular beam epitaxy. Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics, 2013, 31, 041203.	1.2	10
220	A Reconfigurable Low-Power BDD Logic Architecture Using Ferroelectric Single-Electron Transistors. IEEE Transactions on Electron Devices, 2015, 62, 1052-1057.	3.0	10
221	<italic>In Situ</italic> Process Control of Trilayer Gate-Stacks on p-Germanium With 0.85-nm EOT. IEEE Electron Device Letters, 2015, 36, 881-883.	3.9	10
222	Performance benchmarking of p-type In<inf>0.65</inf>Ga<inf>0.35</inf>As/GaAs<inf>0.4</inf>Sb<inf>0.6</inf> and Ge/Ge<inf>0.93</inf>Sn<inf>0.07</inf> hetero-junction tunnel FETs. , 2016, , .		10
223	Correlated Material Enhanced SRAMs With Robust Low Power Operation. IEEE Transactions on Electron Devices, 2016, 63, 4744-4752.	3.0	10
224	Low power current sense amplifier based on phase transition material. , 2017, , .		10
225	Ultra-low power probabilistic IMT neurons for stochastic sampling machines. , 2017, , .		10
226	PPAC scaling enablement for 5nm mobile SoC technology. , 2017, , .		10
227	Characterization and Modeling of 22 nm FDSOI Cryogenic RF CMOS. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2021, 7, 184-192.	1.5	10
228	Multidimensional nanoscale device modeling: the finite element method applied to the non-equilibrium Green's function formalism. , 0, , .		9
229	Magnetoelectric Flexural Gate Transistor With Nanotesla Sensitivity. Journal of Microelectromechanical Systems, 2013, 22, 71-79.	2.5	9
230	Analysis and benchmarking of graphene based RF low noise amplifiers. , 2013, , .		9
231	Gate/Source overlapped heterojunction tunnel FET for non-Boolean associative processing with plasticity. , 2015, , .		9
232	Analysis of local interconnect resistance at scaled process nodes. , 2015, , .		9
233	Tunnel junction abruptness, source random dopant fluctuation and PBTI induced variability analysis of GaAs0.4Sb0.6/In0.65Ga0.35As heterojunction tunnel FETs. , 2015, , .		9
234	Growth and characterization of metamorphic InAs/GaSb tunnel heterojunction on GaAs by molecular beam epitaxy. Journal of Applied Physics, 2016, 119, .	2.5	9

#	Article	IF	Citations
235	Understanding the Continuous-Time Dynamics of Phase-Transition Nano-Oscillator-Based Ising Hamiltonian Solver. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2020, 6, 155-163.	1.5	9
236	Flicker-Noise Improvement in 100-nm $L_{g} hbox{Si}_{0.50}hbox{Ge}_{0.50}$ Strained Quantum-Well Transistors Using Ultrathin Si Cap Layer. IEEE Electron Device Letters, 2010, 31, 47-49.	3.9	8
237	Low-Temperature Atomic-Layer-Deposited High-Î° Dielectric for p-Channel In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}Heterojunction Tunneling Field-Effect Transistor. Applied Physics Express, 2013, 6, 101201.	2.4	8
238	Design of energyâ€efficient circuits and systems using tunnel field effect transistors. IET Circuits, Devices and Systems, 2013, 7, 294-303.	1.4	8
239	Punch-Through Stop Doping Profile Control via Interstitial Trapping by Oxygen-Insertion Silicon Channel. IEEE Journal of the Electron Devices Society, 2018, 6, 481-486.	2.1	8
240	Ten nanometre CMOS logic technology. Nature Electronics, 2018, 1, 500-501.	26.0	8
241	Stabilizing the commensurate charge-density wave in 1T-tantalum disulfide at higher temperatures via potassium intercalation. Nanoscale, 2019, 11, 6016-6022.	5.6	8
242	A Hybrid FeMFET-CMOS Analog Synapse Circuit for Neural Network Training and Inference. , 2020, , .		8
243	Interlayer Engineering of Band Gap and Hole Mobility in p-Type Oxide SnO. ACS Applied Materials & Interfaces, 2022, 14, 25670-25679.	8.0	8
244	Device circuit co-design using classical and non-classical III–V Multi-Gate Quantum-Well FETs (MuQFETs). , 2011, , .		7
245	Multi-technique study of defect generation in high-k gate stacks. , 2012, , .		7
246	A programmable ferroelectric single electron transistor. Applied Physics Letters, 2013, 102, 053505.	3.3	7
247	Read optimized MRAM with separate read-write paths based on concerted operation of magnetic tunnel junction with correlated material. , 2015, , .		7
248	Single-Ended and Differential MRAMs Based on Spin Hall Effect: A Layout-Aware Design Perspective. , 2015, , .		7
249	A random number generator based on insulator-to-metal electronic phase transitions. , 2017, , .		7
250	Emerging Steep-Slope Devices and Circuits: Opportunities and Challenges. , 2019, , 195-230.		7
251	Cryogenic Performance for Compute-in-Memory Based Deep Neural Network Accelerator. , 2021, , .		7
252	Band-gap engineered hot carrier tunnel transistors. , 2009, , .		6

#	Article	IF	Citations
253	Video analytics using beyond CMOS devices. , 2014, , .		6
254	Exploration of Low-Power High-SFDR Current-Steering D/A Converter Design Using Steep-Slope Heterojunction Tunnel FETs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, , 1-11.	3.1	6
255	Computing with dynamical systems in the post-CMOS era. , 2016, , .		6
256	Pulsed I-V on TFETs: Modeling and Measurements. IEEE Transactions on Electron Devices, 2017, 64, 1489-1497.	3.0	6
257	Punch-through stop doping profile control via interstitial trapping by oxygen-insertion silicon channel. , 2017, , .		6
258	Physics and technology of electronic insulator-to-metal transition (E-IMT) for record high on/off ratio and low voltage in device applications. , 2017, , .		6
259	A FerroFET-Based In-Memory Processor for Solving Distributed and Iterative Optimizations via Least-Squares Method. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2019, 5, 132-141.	1.5	6
260	SRAMs and DRAMs With Separate Readâ€“Write Ports Augmented by Phase Transition Materials. IEEE Transactions on Electron Devices, 2019, 66, 929-937.	3.0	6
261	Ferroelectric Polarization Switching Behavior of Hf 0.5 Zr 0.5 O 2 Gate Dielectrics on Gallium Nitride Highâ€Electronâ€Mobilityâ€Transistor Heterostructures. Physica Status Solidi (A) Applications and Materials Science, 2020, 217, 1900717.	1.8	6
262	Harnessing ferroelectrics for non-volatile memories and logic. , 2017, , .		6
263	Benchmarking Monolithic 3D Integration for Compute-in-Memory Accelerators: Overcoming ADC Bottlenecks and Maintaining Scalability to 7nm or Beyond. , 2020, , .		6
264	Large Injection Velocities in Highly Scaled, Fully Depleted Silicon on Insulator Transistors. IEEE Electron Device Letters, 2022, 43, 184-187.	3.9	6
265	Power Performance Analysis of Digital Standard Cells for 28 nm Bulk CMOS at Cryogenic Temperature Using BSIM Models. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2021, 7, 193-200.	1.5	6
266	Multi-Gate Modulation Doped In_{0.7}Ga_{0.3} As Quantum Well FET for Ultra Low Power Digital Logic. ECS Transactions, 2011, 35, 311-317.	0.5	5
267	Investigation of In<inf>x</inf>Ga<inf>1−x</inf>As FinFET architecture with varying indium (x) concentration and quantum confinement. , 2014, , .		5
268	Synthesis for Width Minimization in the Single-Electron Transistor Array. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2862-2875.	3.1	5
269	A FeFET Based Processing-In-Memory Architecture for Solving Distributed Least-Square Optimizations. , 2018, , .		5
270	A Probabilistic Approach to Quantum Inspired Algorithms. , 2019, , .		5

#	Article	IF	Citations
271	Cryogenic Response of HKMG MOSFETs for Quantum Computing Systems. , 2019, , .		5
272	Optimizing the energy balance to achieve autonomous self-powering for vigilant health and IoT applications. Journal of Physics: Conference Series, 2019, 1407, 012001.	0.4	5
273	Hot Carrier Degradation in Cryo-CMOS. , 2020, , .		5
274	Stochastic Resonance in Insulator-Metal-Transition Systems. Scientific Reports, 2020, 10, 5549.	3.3	5
275	Scaled Back End of Line Interconnects at Cryogenic Temperatures. IEEE Electron Device Letters, 2021, 42, 1674-1677.	3.9	5
276	Efficiency of Ferroelectric Field-Effect Transistors: An Experimental Study. IEEE Transactions on Electron Devices, 2022, 69, 1568-1574.	3.0	5
277	A Compute-in-Memory Hardware Accelerator Design With Back-End-of-Line (BEOL) Transistor Based Reconfigurable Interconnect. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2022, 12, 445-457.	3.6	5
278	Tap weight enhancement for broad-band filters. IEEE Transactions on Sonics and Ultrasonics, 1978, 25, 51-54.	0.9	4
279	Magnetoresistance of lateral semiconductor spin valves. Journal of Applied Physics, 2010, 108, 123913.	2.5	4
280	Correlated Flicker Noise and Hole Mobility Characteristics of $(hbox{110})/langlehbox{110}angle$ Uniaxially Strained SiGe FINFETs. IEEE Electron Device Letters, 2012, 33, 1237-1239.	3.9	4
281	Implication of hysteretic selector device on the biasing scheme of a cross-point memory array. , 2015, , .		4
282	A defect-aware approach for mapping reconfigurable Single-Electron Transistor arrays. , 2015, , .		4
283	Experimental Investigation of N-Channel Oxygen-Inserted (OI) Silicon Channel MOSFETs with High-K/Metal Gate Stack. , 2018, , .		4
284	Cardiac Muscle Cellâ€Based Coupled Oscillator Network for Collective Computing. Advanced Intelligent Systems, 2021, 3, 2000253.	6.1	4
285	Electrostatics of nanowire transistors. , 0, , .		3
286	Enhancement mode strained (1.3%) germanium quantum well FinFET (W_{Fin}=20nm) with high mobility (Î¼_{Hole}=700 cm²/Vs), low EOT (â^¼0.7nm) on bulk silicon substrate. , 2014, , .		3
287	Single Event Measurement and Analysis of Antimony Based n-Channel Quantum-Well MOSFET With High-<formula formulatype="inline"><tex Notation="TeX">$kappa$</tex> </formula> Dielectric. IEEE Transactions on Nuclear Science, 2015, 62, 2807-2814.	2.0	3
288	Comparing Energy, Area, Delay Tradeoffs in Going Vertical with CMOS and Asymmetric HTFETs. , 2015, , .		3

#	Article	IF	Citations
289	Area-Aware Decomposition for Single-Electron Transistor Arrays. ACM Transactions on Design Automation of Electronic Systems, 2016, 21, 1-20.	2.6	3
290	Polarization charge and coercive field dependent performance of negative capacitance FETs. , 2016, , .		3
291	Diagnosis and Synthesis for Defective Reconfigurable Single-Electron Transistor Arrays. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, , 1-14.	3.1	3
292	A steep slope Phase-FET based on 2D MoS<inf>2</inf> and the electronic phase transition in VO<inf>2</inf>. , 2017, , .		3
293	Soft error evaluation for InGaAs and Ge complementary FinFETs. , 2017, , .		3
294	Steep Slope Ferroelectric Field Effect Transistor. , 2019, , .		3
295	Spoken vowel classification using synchronization of phase transition nano-oscillators. , 2019, , .		3
296	Rebooting Our Computing Models. , 2019, , .		3
297	CryoMem: A 4â€“300-K 1.3-GHz Hybrid 2T-Gain-Cell-Based eDRAM Macro in 28-nm Logic Process for Cryogenic Applications. IEEE Solid-State Circuits Letters, 2021, 4, 194-197.	2.0	3
298	First-principles mobility prediction for amorphous semiconductors. Physical Review B, 2022, 105, .	3.2	3
299	Modeling Challenges in Molecular Electronics on Silicon. Journal of Computational Electronics, 2005, 4, 83-86.	2.5	2
300	Compound Semiconductor as CMOS Channel Material: DÃ©jÃ vu or New Paradigm?. , 2008, , .		2
301	Direct integration of magnetoelectric sensors with microelectronics. , 2010, , .		2
302	Analyzing Energy-Delay Behavior in Room Temperature Single Electron Transistors. , 2010, , .		2
303	Experimental determination of dominant scattering mechanisms in scaled InAsSb quantum well. , 2011, , .		2
304	Width minimization in the Single-Electron Transistor array synthesis. , 2014, , .		2
305	A Low-Voltage Low-Power LC Oscillator Using the Diode-Connected SymFET. , 2014, , .		2
306	Challenges of fulfilling the promise of tunnel FETs. , 2015, , .		2

#	Article	IF	Citations
307	On the potential of correlated materials in the design of spin-based cross-point memories (Invited). , 2016, , .		2
308	Dynamic Diagnosis for Defective Reconfigurable Single-Electron Transistor Arrays. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1477-1489.	3.1	2
309	Negative capacitance transients in metal-ferroelectric Hf<inf>0.5</inf>Zr<inf>0.5</inf>O<inf>2</inf>-Insulator-Semiconductor (MFIS) capacitors. , 2017, , .		2
310	Investigation of electrically gate-all-around hexagonal nanowire FET (HexFET) architecture for 5 nm node logic and SRAM applications. , 2017, , .		2
311	Computational paradigms using oscillatory networks based on state-transition devices. , 2017, , .		2
312	Energy-Efficient Edge Inference on Multi-Channel Streaming Data in 28nm HKMG FeFET Technology. , 2019, , .		2
313	Microscopic Crystal Phase Inspired Modeling of Zr Concentration Effects in Hf_{1-x}Zr_xO₂Thin Films. , 2019, , .		2
314	Polarization Recovery Behavior of Hf0.5Zr0.5O2 on Gallium Nitride HEMT Heterostructures. , 2019, , .		2
315	Width minimization in the Single-Electron Transistor array synthesis. , 2014, , .		2
316	Microwave Performance of Ferroelectric-Gated GaN HEMTs. , 2020, , .		2
317	An All Electrical Spin Detector. , 2006, , .		1
318	Indium gallium arsenide on silicon interband tunnel diodes for NDR-based memory and steep subthreshold slope transistor applications. , 2009, , .		1
319	Giant magnetoelectric effect in nanofabricated Pb(Zr<inf>0.52</inf>Ti<inf>0.48</inf>)O<inf>3</inf>-Fe<inf>85</inf>B<inf>5</inf>Si<inf>10</inf> cantilevers and resonant gate transistors. , 2011, , .		1
320	Ultra-sensitive magnetoelectric sensor with high saturation field. , 2012, , .		1
321	A compact model for compound semiconductor tunneling field-effect-transistors. , 2014, , .		1
322	Performance enhancement of InAsSb QW-MOSFETs with in-situ H2 plasma cleaning for gate stack formation. , 2015, , .		1
323	Modelling hysteresis in vanadium dioxide oscillators. Electronics Letters, 2015, 51, 819-820.	1.0	1
324	Heterojunction resonant tunneling diode at the atomic limit. , 2015, , .		1

#	Article	IF	Citations
325	Band structure engineered Germanium-Tin (GeSn) p-channel tunnel transistors. , 2016, , .		1
326	Transistor innovation in the 21st century â€" A lesson in serendipity. , 2016, , .		1
327	Electrically driven reversible insulator-metal phase transition in Ca<inf>2</inf>RuO<inf>4</inf>. , 2016, , .		1
328	Opportunties and challenges of tunnel FETs. , 2016, , .		1
329	Single-Event Measurement and Analysis of Antimony-Based p-Channel Quantum-Well MOSFETs With High- $kappa $ Dielectric. IEEE Transactions on Nuclear Science, 2017, 64, 434-440.	2.0	1
330	Connecting spectral techniques for graph coloring and eigen properties of coupled dynamics: A pathway for solving combinatorial optimizations (Invited paper). , 2017, , .		1
331	Heterogeneous integration of InAs/GaSb tunnel diode structure on silicon using 200 nm GaAsSb dislocation filtering buffer. AIP Advances, 2018, 8, .	1.3	1
332	Investigation of the abrupt phase transition in 1T-TaS<inf>2</inf>/MoS<inf>2</inf> heterostructures. , 2018, , .		1
333	Spoken vowel classification using synchronization of phase transition nano-oscillators. , 2019, , .		1
334	Significance of Multi and Few Domain Ferroelectric Switching Dynamics for Steep-Slope Non-Hysteretic Ferroelectric Field Effect Transistor. , 2019, , .		1
335	First-principles investigation of amorphous n-type In₂ O₃ for BEOL transistor. , 2021, , .		1
336	Intermixing reduction in ultra-thin titanium nitride/hafnium oxide film stacks grown on oxygen-inserted silicon and associated reduction of the interface charge dipole. Journal of Applied Physics, 2021, 130, 185303.	2.5	1
337	Asymptotically efficient, binary-compatible block codes for M-ary runlength-limited constraints. , 0, , .		0
338	Surface Potentials of Conjugated Molecules on Metal Surfaces: Measurements Using Electrostatic Force Microscopy and Calculations using a Preliminary Physically-Based Model.. Materials Research Society Symposia Proceedings, 2000, 636, 9381.	0.1	0
339	Optimal block codes for M-ary runlength-limited channels. , 0, , .		0
340	Coherent transport in SWCNTs with spin-orbit coupling. , 0, , .		0
341	Molecular elements on silicon substrates: modeling issues and device prospects. , 0, , .		0
342	Nanodevices: a bottom-up view. , 2005, , .		0

#	Article	IF	Citations
343	Are Short Molecules Quantum Dot Arrays?. , 0, , .		0
344	Are Short Molecules Quantum Dot Arrays?. , 2006, , .		0
345	An All Electrical Spin Detector. , 0, , .		0
346	Indium Antimonide based Quantum Well FETs for Ultra-High Speed Electronics. , 2006, , .		0
347	Fabrication of axially-doped silicon nanowire tunnel FETs and characterization of tunneling current. , 2010, , .		0
348	Non-silicon logic elements on silicon for extreme voltage scaling. , 2010, , .		0
349	Experimental demonstration of “Cold” low contact resistivity ohmic contacts on moderately doped n-Ge with in-situ atomic hydrogen clean. , 2012, , .		0
350	Benchmarking of Novel Contact Architectures on Silicon and Germanium. , 2012, , .		0
351	Complete band alignment determination of InAs-GaSb broken-gap tunneling field-effect transistor hetero-junction. , 2013, , .		0
352	Electron trapping dominance in strained germanium quantum well planar and FinFET devices with NBTI. , 2015, , .		0
353	Self-powered wearable sensor platforms for wellness. , 2015, , .		0
354	Computing with coupled dynamical systems. , 2016, , .		0
355	Orbitronics â€" Harnessing metal insulator phase transition in 1T-MoSe<inf>2</inf>. , 2016, , .		0
356	In quest of the next switch. , 2016, , .		0
357	In Quest of the Next Information Processing Substrate. , 2017, , .		0
358	Corrugated channel In<inf>0.8</inf>Ga<inf>0.2</inf>As quantum well transistors for low power logic applications. , 2017, , .		0
359	Ultra-low power probabilistic IMT neurons for stochastic sampling machines. , 2017, , .		0
360	A computationally efficient compact model for leakage in cross-point array. , 2017, , .		0

#	Article	IF	Citations
361	Photoconductance Decay Characterization of 3D Multi-Fin Silicon on SOI Substrates. IEEE Electron Device Letters, 2017, 38, 1513-1515.	3.9	0
362	Dynamics of Coupled Systems and their Computing Properties Invited Paper : Invited Paper. , 2018, , .		0
363	Investigation of Threshold Switch OFF -State Resistance on Performance Enhancement in 2D Mos2 Phase-FETs. , 2018, , .		0
364	Technology Innovations in Selective ALD for Next-Generation Contacts and Vias. , 2018, , .		0
365	Cockcroft-Walton Multiplier based on Unipolar $mathbf{Ag/HfO_{2}/Pt}$ Threshold Switch. , 2018, , .		0
366	Sensing in Ferroelectric Memories and Flip-Flops. , 2019, , 47-80.		0
367	Cardiac Muscle Cellâ€Based Coupled Oscillator Network for Collective Computing. Advanced Intelligent Systems, 2021, 3, 2170043.	6.1	0