Michael Waltl

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/498967/publications.pdf

Version: 2024-02-01

104 papers	2,097 citations	361413 20 h-index	302126 39 g-index
104 all docs	104 docs citations	104 times ranked	1959 citing authors

#	Article	IF	Citations
1	The role of charge trapping in MoS ₂ /SiO ₂ and MoS ₂ /hBN field-effect transistors. 2D Materials, 2016, 3, 035004.	4.4	174
2	The performance limits of hexagonal boron nitride as an insulator for scaled CMOS devices based on two-dimensional materials. Nature Electronics, 2021, 4, 98-108.	26.0	161
3	Long-Term Stability and Reliability of Black Phosphorus Field-Effect Transistors. ACS Nano, 2016, 10, 9543-9549.	14.6	158
4	Ultrathin calcium fluoride insulators for two-dimensional field-effect transistors. Nature Electronics, 2019, 2, 230-235.	26.0	156
5	Comphy â€" A compact-physics framework for unified modeling of BTI. Microelectronics Reliability, 2018, 85, 49-65.	1.7	137
6	Improved Hysteresis and Reliability of MoS₂Transistors With High-Quality CVD Growth and Al₂O₃Encapsulation. IEEE Electron Device Letters, 2017, 38, 1763-1766.	3.9	81
7	A unified perspective of RTN and BTI. , 2014, , .		71
8	On the microscopic structure of hole traps in pMOSFETs. , 2014, , .		57
9	Highly-stable black phosphorus field-effect transistors with low density of oxide traps. Npj 2D Materials and Applications, 2017, 1, .	7.9	57
10	NBTI in Nanoscale MOSFETsâ€"The Ultimate Modeling Benchmark. IEEE Transactions on Electron Devices, 2014, 61, 3586-3593.	3.0	49
11	Energetic mapping of oxide traps in MoS ₂ field-effect transistors. 2D Materials, 2017, 4, 025108.	4.4	49
12	A brief overview of gate oxide defect properties and their relation to MOSFET instabilities and device and circuit time-dependent variability. Microelectronics Reliability, 2018, 81, 186-194.	1.7	49
13	Characterization of Single Defects in Ultrascaled MoS_{2} Field-Effect Transistors. ACS Nano, 2018, 12, 5368-5375.	14.6	48
14	A Physical Model for the Hysteresis in MoS₂ Transistors. IEEE Journal of the Electron Devices Society, 2018, 6, 972-978.	2.1	43
15	Advanced characterization of oxide traps: The dynamic time-dependent defect spectroscopy. , 2013, , .		38
16	Reliability and Variability of Advanced CMOS Devices at Cryogenic Temperatures. , 2020, , .		31
17	Improving stability in two-dimensional transistors with amorphous gate oxides by Fermi-level tuning. Nature Electronics, 2022, 5, 356-366.	26.0	31
18	Hydrogen-related volatile defects as the possible cause for the recoverable component of NBTI. , 2013, , .		30

#	ARTICLE	IF	CITATIONS
19	Reliability of scalable MoS₂ FETs with 2â€‰nm crystalline CaF₂ insulators. 2D Materials, 2019, 6, 045004.	4.4	29
20	On the volatility of oxide defects: Activation, deactivation, and transformation. , 2015, , .		25
21	Complete extraction of defect bands responsible for instabilities in n and pFinFETs. , 2016, , .		24
22	Perspective of 2D Integrated Electronic Circuits: Scientific Pipe Dream or Disruptive Technology?. Advanced Materials, 2022, 34, e2201082.	21.0	24
23	Gate-sided hydrogen release as the origin of "permanent" NBTI degradation: From single defects to lifetimes. , 2015, , .		23
24	Impact of Mixed Negative Bias Temperature Instability and Hot Carrier Stress on MOSFET Characteristicsâ€"Part II: Theory. IEEE Transactions on Electron Devices, 2019, 66, 241-248.	3.0	23
25	Toward Automated Defect Extraction From Bias Temperature Instability Measurements. IEEE Transactions on Electron Devices, 2021, 68, 4057-4063.	3.0	23
26	Reduction of the BTI time-dependent variability in nanoscaled MOSFETs by body bias. , 2013, , .		22
27	Superior NBTI in High- k SiGe Transistorsâ€“Part I: Experimental. IEEE Transactions on Electron Devices, 2017, 64, 2092-2098.	3.0	22
28	Impact of Mixed Negative Bias Temperature Instability and Hot Carrier Stress on MOSFET Characteristicsâ€"Part I: Experimental. IEEE Transactions on Electron Devices, 2019, 66, 232-240.	3.0	22
29	Physical Modeling of Charge Trapping in 4H-SiC DMOSFET Technologies. IEEE Transactions on Electron Devices, 2021, 68, 4016-4021.	3.0	22
30	Mixed Hot-Carrier/Bias Temperature Instability Degradation Regimes in Full {<i>V</i> _G, <i>V</i> _D} Bias Space: Implications and Peculiarities. IEEE Transactions on Electron Devices, 2020, 67, 3315-3322.	3.0	20
31	Efficient physical defect model applied to PBTI in high-Îº stacks. , 2017, , .		19
32	The â€œpermanentâ€•component of NBTI revisited: Saturation, degradation-reversal, and annealing. , 2016, , .		17
33	The defect-centric perspective of device and circuit reliabilityâ€"From gate oxide defects to circuits. Solid-State Electronics, 2016, 125, 52-62.	1.4	17
34	Physical Modeling of Bias Temperature Instabilities in SiC MOSFETs. , 2019, , .		17
35	Ultra-Low Noise Defect Probing Instrument for Defect Spectroscopy of MOS Transistors. IEEE Transactions on Device and Materials Reliability, 2020, 20, 242-250.	2.0	15
36	Advanced modeling of charge trapping: RTN, 1/f noise, SILC, and BTI. , 2014, , .		14

#	ARTICLE	IF	CITATIONS
37	A single-trap study of PBTI in SiON nMOS transistors: Similarities and differences to the NBTI/pMOS case. , 2014, , .		13
38	Superior NBTI in High-k SiGe Transistorsâ€"Part II: Theory. IEEE Transactions on Electron Devices, 2017, 64, 2099-2105.	3.0	13
39	Separation of electron and hole trapping components of PBTI in SiON nMOS transistors. Microelectronics Reliability, 2020, 114, 113746.	1.7	13
40	Microscopic oxide defects causing BTI, RTN, and SILC on high-k FinFETs. , 2015, , .		12
41	Characterization and physical modeling of the temporal evolution of near-interfacial states resulting from NBTI/PBTI stress in nMOS/pMOS transistors. , 2018, , .		11
42	Reliability of Miniaturized Transistors from the Perspective of Single-Defects. Micromachines, 2020, 11, 736.	2.9	11
43	Characterization of Interface Defects With Distributed Activation Energies in GaN-Based MIS-HEMTs. IEEE Transactions on Electron Devices, 2017, 64, 1045-1052.	3.0	10
44	Firstâ€"Principles Parameterâ€"Free Modeling of nâ€" and pâ€"FET Hotâ€"Carrier Degradation. , 2019, , .		10
45	Soft error hardening enhancement analysis of NBTI tolerant Schmitt trigger circuit. Microelectronics Reliability, 2020, 107, 113617.	1.7	10
46	Advanced data analysis algorithms for the time-dependent defect spectroscopy of NBTI. , 2012, , .		9
47	Implications of gate-sided hydrogen release for post-stress degradation build-up after BTI stress. , 2017, , .		9
48	Evaluation of Advanced MOSFET Threshold Voltage Drift Measurement Techniques. IEEE Transactions on Device and Materials Reliability, 2019, 19, 358-362.	2.0	9
49	Single- Versus Multi-Step Trap Assisted Tunneling Currentsâ€"Part II: The Role of Polarons. IEEE Transactions on Electron Devices, 2022, 69, 4486-4493.	3.0	9
50	The impact of mixed negative bias temperature instability and hot carrier stress on single oxide defects. , 2017, , .		8
51	The Mysterious Bipolar Bias Temperature Stress from the Perspective of Gate-Sided Hydrogen Release. , 2020, , .		8
52	Semi-Automated Extraction of the Distribution of Single Defects for nMOS Transistors. Micromachines, 2020, 11, 446.	2.9	8
53	Single- Versus Multi-Step Trap Assisted Tunneling Currentsâ€"Part I: Theory. IEEE Transactions on Electron Devices, 2022, 69, 4479-4485.	3.0	8
54	Characterization and modeling of single defects in GaN/AlGaN fin-MIS-HEMTs. , 2017, , .		7

#	ARTICLE	IF	CITATIONS
55	Nanoscale evidence for the superior reliability of SiGe high-k pMOSFETs. , 2016, , .		6
56	Bias-temperature instability on the back gate of single-layer double-gated graphene field-effect transistors. Japanese Journal of Applied Physics, 2016, 55, 04EP03.	1.5	6
57	Electrostatic Coupling and Identification of Single-Defects in GaN/AlGaN Fin-MIS-HEMTs. Solid-State Electronics, 2019, 156, 41-47.	1.4	6
58	Bias Temperature Instability Aware and Soft Error Tolerant Radiation Hardened 10T SRAM Cell. Electronics (Switzerland), 2020, 9, 256.	3.1	6
59	Efficient Modeling of Charge Trapping at Cryogenic Temperaturesâ€”Part I: Theory. IEEE Transactions on Electron Devices, 2021, 68, 6365-6371.	3.0	6
60	Evidence of Tunneling Driven Random Telegraph Noise in Cryo-CMOS. , 2021, , .		6
61	(Invited) Impact of Gate Dielectrics on the Threshold Voltage in MoS₂Transistors. ECS Transactions, 2017, 80, 203-217.	0.5	5
62	Quantum Chemistry Treatment of Silicon-Hydrogen Bond Rupture by Nonequilibrium Carriers in Semiconductor Devices. Physical Review Applied, 2021, 16, .	3.8	5
63	Advanced Electrical Characterization of Single Oxide Defects Utilizing Noise Signals. , 2020, , 229-257.		5
64	Quantum Mechanical Charge Trap Modeling to Explain BTI at Cryogenic Temperatures. , 2020, , .		4
65	Defect Spectroscopy in SiC Devices. , 2020, , .		4
66	On the Distribution of Single Defect Threshold Voltage Shifts in SiON Transistors. IEEE Transactions on Device and Materials Reliability, 2021, 21, 199-206.	2.0	4
67	Error-Tolerant Reconfigurable VDD 10T SRAM Architecture for IoT Applications. Electronics (Switzerland), 2021, 10, 1718.	3.1	4
68	High-performance radiation hardened NMOS only Schmitt Trigger based latch designs. Analog Integrated Circuits and Signal Processing, 2021, 109, 657-671.	1.4	4
69	Atomistic Modeling of Oxide Defects. , 2020, , 609-648.		4
70	Characterization and modeling of charge trapping: From single defects to devices. , 2014, , .		3
71	Physical modeling of the hysteresis in M0S2 transistors. , 2017, , .		3
72	Annealing and Encapsulation of CVD-MoS2 FETs with 10¹⁰On/Off Current Ratio. , 2018, , .		3

#	ARTICLE	IF	CITATIONS
73	Minimum Energy Paths for Non-Adiabatic Charge Transitions in Oxide Defects. , 2019, , .		3
74	Efficient Modeling of Charge Trapping at Cryogenic Temperaturesâ€"Part II: Experimental. IEEE Transactions on Electron Devices, 2021, 68, 6372-6378.	3.0	3
75	Modeling the Hysteresis of Current-Voltage Characteristics in 4H-SiC Transistors. , 2020, , .		3
76	Reliability of single-layer MoS<inf>2</inf> field-effect transistors with SiO<inf>2</inf> and hBN gate insulators. , 2016, , .		2
77	Reliability of next-generation field-effect transistors with transition metal dichalcogenides. , 2018, , .		2
78	Statistical Characterization of BTI and RTN using Integrated pMOS Arrays. , 2019, , .		2
79	Extraction of Statistical Gate Oxide Parameters From Large MOSFET Arrays. IEEE Transactions on Device and Materials Reliability, 2020, 20, 251-257.	2.0	2
80	Design of Fault-Tolerant and Thermally Stable XOR Gate in Quantum dot Cellular Automata. , 2021, , .		2
81	Impact of Bias Temperature Instabilities on the Performance of Logic Inverter Circuits Using Different SiC Transistor Technologies. Crystals, 2021, 11, 1150.	2.2	2
82	Temperature Dependent Mismatch and Variability in a Cryo-CMOS Array with 30k Transistors. , 2022, , .		2
83	Efficient Evaluation of the Time-Dependent Threshold Voltage Distribution Due to NBTI Stress Using Transistor Arrays. , 2022, , .		2
84	Hot-carrier degradation in single-layer double-gated graphene field-effect transistors. , 2015, , .		1
85	Impact of hot carrier stress on the defect density and mobility in double-gated graphene field-effect transistors. , 2015, , .		1
86	Interplay between hot carrier and bias stress components in single-layer double-gated graphene field-effect transistors. , 2015, , .		1
87	Characterization and Modeling of Single Charge Trapping in MOS Transistors. , 2019, , .		1
88	Low Cost and High Performance Radiation Hardened Latch Design for Reliable Circuits. , 2019, , .		1
89	CV Stretch-Out Correction after Bias Temperature Stress: Work-Function Dependence of Donor-/Acceptor-Like Traps, Fixed Charges, and Fast States. , 2021, , .		1
90	Utilizing NBTI for Operation Detection of Integrated Circuits. Communications in Computer and Information Science, 2019, , 190-201.	0.5	1

#	ARTICLE	IF	CITATIONS
91	Impact of single-defects on the variability of CMOS inverter circuits. Microelectronics Reliability, 2021, 126, 114275.	1.7	1
92	Reliability of black phosphorus field-effect transistors with respect to bias-temperature and hot-carrier stress. , 2017, , .		1
93	Machine Learning Prediction of Defect Formation Energies in a-SiO2. , 2020, , .		1
94	TCAD Modeling of Temperature Activation of the Hysteresis Characteristics of Lateral 4H-SiC MOSFETs. IEEE Transactions on Electron Devices, 2022, 69, 3290-3295.	3.0	1
95	The Importance of Secondary Generated Carriers in Modeling of Full Bias Space. , 2022, , .		1
96	Evidence for defect pairs in SiON pMOSFETs. , 2014, , .		0
97	A systematic study of charge trapping in single-layer double-gated GFETs. , 2016, , .		0
98	Accurate mapping of oxide traps in highly-stable black phosphorus FETs. , 2017, , .		0
99	IIRW 2019 Discussion Group II: Reliability for Aerospace Applications. , 2019, , .		0
100	Impact of negative bias temperature instability on single event transients in scaled logic circuits. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2021, 34, e2854.	1.9	0
101	Back Gate Bias-Temperature Instability in Single-Layer Double-Gated Graphene Field-Effect Transistors. , 2015, , .		0
102	Distribution of Step Heights of Electron and Hole Traps in SiON nMOS Transistors. , 2020, , .		0
103	Editorial for the Special Issue on Robust Microelectronic Devices. Crystals, 2022, 12, 16.	2.2	0
104	Performance Analysis of 4H-SiC Pseudo-D CMOS Inverter Circuits Employing Physical Charge Trapping Models. Materials Science Forum, 0, 1062, 688-695.	0.3	0