Jacob A Abraham

List of Publications by Year
in descending order

124 papers	2,103 citations	840776 11 h-index	330143 37 g-index
124 all docs	124 docs citations	124 times ranked	994 citing authors

#	Article	IF	Citations
1	Algorithm-Based Fault Tolerance for Matrix Operations. IEEE Transactions on Computers, 1984, C-33, 518-528.	3.4	982
2	Quantitative evaluation of soft error injection techniques for robust system design. , 2013, , .		172
3	Beneficial neurocognitive effects of transcranial laser in older adults. Lasers in Medical Science, 2017, 32, 1153-1162.	2.1	96
4	ACCE: Automatic correction of control-flow errors. , 2007, , .		53
5	A 5-GS/s 10-b 76-mW Time-Interleaved SAR ADC in 28 nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 1673-1683.	5.4	53
6	CEDA: Control-Flow Error Detection Using Assertions. IEEE Transactions on Computers, 2011, 60, 1233-1245.	3.4	52
7	CLEAR. , 2016, , .		45
8	Fault simulation of linear analog circuits. Journal of Electronic Testing: Theory and Applications (JETTA), 1993, 4, 345-360.	1.2	39
9	Automatic Generation of Instructions to Robustly Test Delay Defects in Processors. Proceedings of the IEEE European Test Workshop, 2007, , .	0.0	32
10	An RTL Abstraction Technique for Processor Microarchitecture Validation and Test Generation. Journal of Electronic Testing: Theory and Applications (JETTA), 2000, 16, 67-81.	1.2	25
11	Testability-Driven Statistical Path Selection. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1275-1287.	2.7	23
12	Hierarchical fault modeling for linear analog circuits. Analog Integrated Circuits and Signal Processing, 1996, 10, 89-99.	1.4	21
13	Low Cost RF Receiver Parameter Measurement with On-Chip Amplitude Detectors. VLSI Test Symposium (VTS), Proceedings, IEEE, 2008, , .	1.0	20
14	Built-In Test of RF Mixers Using RF Amplitude Detectors. , 2007, , .		18
15	Jitter Decomposition in High-Speed Communication Systems. , 2008, , .		16
16	A unified approach for fault simulation of linear mixed-signal circuits. Journal of Electronic Testing: Theory and Applications (JETTA), 1996, 9, 29-41.	1.2	14
17	Tolerating Soft Errors in Processor Cores Using CLEAR (Cross-Layer Exploration for Architecting) Tj ETQq1 1 0.784314 rgBT /Overlock 1 1839-1852.	2.7	14
18	Safety Design of a Convolutional Neural Network Accelerator with Error Localization and Correction. , 2019, , .		14

#	Article	IF	Citations
19	Title is missing!. Journal of Electronic Testing: Theory and Applications (JETTA), 2003, 19, 149-160.	1.2	13
20	Budget-Dependent Control-Flow Error Detection. , 2008, , .		13
21	Improved verification of hardware designs through antecedent conditioned slicing. International Journal on Software Tools for Technology Transfer, 2007, 9, 89-101.	1.9	11
22	Transformer-Coupled Loopback Test for Differential Mixed-Signal Specifications. VLSI Test Symposium (VTS), Proceedings, IEEE, 2007, , .	1.0	10
23	Post-Silicon Timing Validation Method Using Path Delay Measurements. , 2011, , .		10
24	Rethinking error injection for effective resilience. , 2014, , .		10
25	Sequential equivalence checking between system level and RTL descriptions. Design Automation for Embedded Systems, 2008, 12, 377-396.	1.0	9
26	On-Chip Delay Measurement Based Response Analysis for Timing Characterization. Journal of Electronic Testing: Theory and Applications (JETTA), 2010, 26, 599-619.	1.2	9
27	Imbalance-Based Self-Test for High-Speed Mixed-Signal Embedded Systems. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 785-789.	3.0	9
28	Path Criticality Computation in Parameterized Statistical Timing Analysis Using a Novel Operator. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 497-508.	2.7	9
29	Real-time checking of linear control systems using analog checksums. , 2013, , .		9
30	EAGLE: A regression model for fault coverage estimation using a simulation based metric. , 2014, , .		9
31	Training Multi-Bit Quantized and Binarized Networks with a Learnable Symmetric Quantizer. IEEE Access, 2021, 9, 47194-47203.	4.2	9
32	Synthesis of Native Mode Self-Test Programs. Journal of Electronic Testing: Theory and Applications (JETTA), 1998, 13, 137-148.	1.2	8
33	An area efficient on-chip static IR drop detector/evaluator. , 2009, , .		8
34	Delay defect diagnosis methodology using path delay measurements. , 2011, , .		8
35	Functional test generation for hard to detect stuck-at faults using RTL model checking. , 2012, , .		8
36	Concurrent Path Selection Algorithm in Statistical Timing Analysis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1715-1726.	3.1	8

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37	A Built-In Repair Analyzer With Optimal Repair Rate for Word-Oriented Memories. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 281-291.	3.1	8
38	In-depth soft error vulnerability analysis using synthetic benchmarks. , 2015, , .		8
39	Generation and evaluation of current and logic tests for switch-level sequential circuits. Journal of Electronic Testing: Theory and Applications (JETTA), 1992, 3, 359-366.	1.2	7
40	Extraction based verification method for off the shelf integrated circuits. , 2009, , .		7
41	Recursive Path Selection for Delay Fault Testing. , 2009, , .		7
42	At-speed Test of High-Speed DUT Using Built-Off Test Interface. , 2010, , .		7
43	Efficient and product-representative timing model validation. , 2011, , .		7
44	Frequency Response Verification of Analog Circuits Using Global Optimization Techniques. Journal of Electronic Testing: Theory and Applications (JETTA), 2001, 17, 395-408.	1.2	6
45	Functionally valid gate-level peak power estimation for processors. , 2009, , .		6
46	Transformer-Coupled Loopback Test for Differential Mixed-Signal Dynamic Specifications. IEEE Transactions on Instrumentation and Measurement, 2011, 60, 2014-2024.	4.7	6
47	Phase-Aware Multitone Digital Signal Based Test for RF Receivers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 2097-2110.	5.4	6
48	Power prediction of embedded scalar and vector processor: Challenges and solutions. , 2017, , .		6
49	Real-Time Error Detection in Nonlinear Control Systems Using Machine Learning Assisted State-Space Encoding. IEEE Transactions on Dependable and Secure Computing, 2021, 18, 576-592.	5.4	6
50	A low-cost concurrent error detection technique for processor control logic. , 2008, , .		5
51	LFSR-Based Performance Characterization of Nonlinear Analog and Mixed-Signal Circuits. , 2009, , .		5
52	Vector based Analog to Digital Converter sequential testing methodology to minimize ATE memory and analysis requirements. , 2009, , .		5
53	Real-time dynamic hybrid BiST solution for Very-Low-Cost ATE production testing of A/D converters with controlled DPPM. , 2010, , .		5
54	A Built-In Self-Test scheme for DDR memory output timing test and measurement. , 2012, , .		5

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55	Frequency-Independent Parametric Built in Test Solution for PLLs with Low Speed Test Resources. , 2012, , .		5
56	Dynamic Trace Signal Selection for Post-Silicon Validation. , 2013, , .		5
57	Capacitor-Coupled Built-Off Self-Test in Analog and Mixed-Signal Embedded Systems. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 257-261.	3.0	5
58	A Broadband CMOS RF Front End for Direct Sampling Satellite Receivers. IEEE Journal of Solid-State Circuits, 2019, 54, 2140-2148.	5.4	5
59	Cross-Layer Resilience. , 2019, , .		5
60	A Robust Top-Down Dynamic Power Estimation Methodology for Delay Constrained Register Transfer Level Sequential Circuits. , 2008, , .		4
61	Low-cost Test of Timing Mismatch Among Time-Interleaved A/D Converters in High-speed Communication Systems. VLSI Test Symposium (VTS), Proceedings, IEEE, 2008, , .	1.0	4
62	Characterization and testing of microelectromechnical accelerometers. , 2008, , .		4
63	On-Line Calibration and Power Optimization of RF Systems Using a Built-In Detector. , 2009, , .		4
64	Hybrid BiST solution for Analog to Digital Converters with low-cost Automatic Test Equipment compatibility. , 2009, , .		4
65	A Built-In Self-Test scheme for high speed I/O using cycle-by-cycle edge control. , 2010, , .		4
66	Path criticality computation in parameterized statistical timing analysis. , 2011, , .		4
67	Refactoring of Timing Graphs and Its Use in Capturing Topological Correlation in SSTA. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 485-496.	2.7	4
68	Cross-Layer Control Adaptation for Autonomous System Resilience. , 2018, , .		4
69	A Random Jitter RMS Estimation Technique for BIST Applications. , 2009, , .		3
70	Closed-loop Built in Self Test for PLL production testing with minimal tester resources. , 2009, , .		3
71	A novel characterization technique for high speed I/O mixed signal circuit components using random jitter injection. , 2010, , .		3
72	On Computing Criticality in Refactored Timing Graphs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1935-1939.	2.7	3

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73	Cross-Layer Resilience in Low-Voltage Digital Systems: Key Insights. , 2017, , .		3
74	ESIFT: Efficient System for Error Injection. , 2018, , .		3
75	Design of a Safe Convolutional Neural Network Accelerator. , 2019, , .		3
76	A Proactive System for Voltage-Droop Mitigation in a 7-nm Hexagonâ„¢ Processor. IEEE Journal of Solid-State Circuits, 2021, 56, 1166-1175.	5.4	3
77	Conditioned HDL Slicing A way to Speed-up Formal Verification. Midwest Symposium on Circuits and Systems, 2006, , .	1.0	2
78	A 6-bit 300-MS/s 2.7mW ADC based on linear voltage controlled delay line. , 2008, , .		2
79	Dedicated Rewriting: Automatic Verification of Low Power Transformations in RTL. , 2009, , .		2
80	PLL lock time prediction and parametric testing by lock waveform characterization. , 2010, , .		2
81	Off-Chip Skew Measurement and Compensation Module (SMCM) Design for Built-Off Test Chip. Journal of Electronic Testing: Theory and Applications (JETTA), 2011, 27, 429-439.	1.2	2
82	Stream cipher hash based execution monitoring (SCHEM) framework for intrusion detection on embedded processors. , 2012, , .		2
83	Enhanced algorithm of combining trace and scan signals in post-silicon validation. , 2013, , .		2
84	Error Resilient Real-Time State Variable Systems for Signal Processing and Control. , 2014, , .		2
85	Real-time correction of dc servo motor and controller failures using analog checksums. , 2014, , .		2
86	Dynamic Performance Characterization of Embedded Single-Ended Mixed-Signal Circuits. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 329-333.	3.0	2
87	Designing nonlinearity characterization for mixed-signal circuits in system-on-chip. Analog Integrated Circuits and Signal Processing, 2015, 82, 341-348.	1.4	2
88	Checksum based error detection in linearized representations of non linear control systems. , 2016, , .		2
89	A multi-band low noise amplifier with strong immunity to interferers. Analog Integrated Circuits and Signal Processing, 2017, 93, 13-27.	1.4	2
90	Spectral Leakage-Driven Loopback Scheme for Prediction of Mixed-Signal Circuit Specifications. IEEE Transactions on Industrial Electronics, 2019, 66, 586-594.	7.9	2

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91	A Neural Network Decomposition Algorithm for Mapping on Crossbar-Based Computing Systems. Electronics (Switzerland), 2020, 9, 1526.	3.1	2
92	Simulation Study on the Optimization of Photon Energy Delivered to the Prefrontal Cortex in Low-Level-Light Therapy Using Red to Near-Infrared Light. IEEE Journal of Selected Topics in Quantum Electronics, 2021, 27, 1-10.	2.9	2
93	On Design Validation Using Verification Technology. Journal of Electronic Testing: Theory and Applications (JETTA), 1999, 15, 173-189.	1.2	1
94	Efficient Combinational Verification Using Overlapping Local BDDs and a Hash Table. Formal Methods in System Design, 2002, 21, 95-101.	0.8	1
95	Error detection in 2-D Discrete Wavelet lifting transforms. , 2009, , .		1
96	SNR-Aware Error Detection for Low-Power Discrete Wavelet Lifting Transform in JPEG 2000. , 2009, , .		1
97	“Manufacturing test of systems-on-a-chip (SoCs)”. , 2011, , .		1
98	On-chip source synchronous interface timing test scheme with calibration. , 2012, , .		1
99	Testing and Fault Diagnosis of Time-Interleaved S? Modulators Using Checksums. , 2012, , .		1
100	Application of under-approximation techniques to functional test generation targeting hard to detect stuck-at faults. , 2013, , .		1
101	Asynchronous Measurement of Transient Phase-Shift Resulting From RF Receiver State-Change. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 2740-2751.	5.4	1
102	Digital Calibration for 8-Bit Delay Line ADC Using Harmonic Distortion Correction. , 2013, , .		1
103	Harmonic distortion correction for 8-bit delay line ADC using gray code. , 2014, , .		1
104	A novel low power 11-bit hybrid ADC using flash and delay line architectures. , 2014, , .		1
105	A novel low power 11-bit hybrid ADC using flash and delay line architectures. , 2014, , .		1
106	Resiliency Demands on Next Generation Critical Embedded Systems. , 2019, , .		1
107	Single Trojan injection model generation and detection. , 2016, , .		1
108	Performance-Optimized Design for Parametric Reliability. Journal of Electronic Testing: Theory and Applications (JETTA), 2008, 24, 129-141.	1.2	0

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109	High speed recursion-free CORDIC architecture. , 2010, , .		0
110	Calibration-enabled scalable built-in current sensor compatible with very low cost ATE. , 2010, , .		0
111	Arbitrary Waveform Generator Response Shaping Method to Enable ADC Linearity Testing on Very Low Cost Automatic Test Equipment. , 2011, , .		0
112	On-Chip Programmable Dual-Capture for Double Data Rate Interface Timing Test. , 2011, , .		0
113	Robust power gating reactivation by dynamic wakeup sequence throttling. , 2011, , .		0
114	Guest Editorial Special Issue of IEEE Sensors on the 4th IEEE International Workshop on Advances in Sensors and Interfaces 2011 (IWASI 2011). IEEE Sensors Journal, 2012, 12, 3299-3300.	4.7	0
115	A Built-in Self-Test Scheme for Memory Interfaces Timing Test and Measurement. Journal of Electronic Testing: Theory and Applications (JETTA), 2012, 28, 585-597.	1.2	0
116	Calibration Enabled Scalable Current Sensor Module for Quiescent Current Testing. Journal of Electronic Testing: Theory and Applications (JETTA), 2012, 28, 697-704.	1.2	0
117	Indirect method for random jitter measurement on SoCs using critical path characterization. , 2012, , .		0
118	On a rewriting strategy for dynamically managing power constraints and power dissipation in SoCs. , 2013, , .		0
119	A novel algorithm for sparse FFT pruning and its applications to OFDMA technology. , 2014, , .		0
120	Digital Calibration for 8-bit Delay Line ADC Using Harmonic Distortion Correction. Journal of Electronic Testing: Theory and Applications (JETTA), 2015, 31, 127-138.	1.2	0
121	FSNoC: Safe Network-on-Chip Design with Packet Level Lock Stepping. , 2019, , .		0
122	Resilient Reorder Buffer Design for Network-on-Chip. , 2019, , .		0
123	Built-in Harmonic Prediction Scheme for Embedded Segmented-Data-Converters. IEEE Access, 2020, 8, 7851-7860.	4.2	0
124	A Current and Temperature Limiting System in a 7-nm Hexagonâ„¢ Compute Digital Signal Processor. IEEE Journal of Solid-State Circuits, 2021, 56, 814-823.	5.4	0